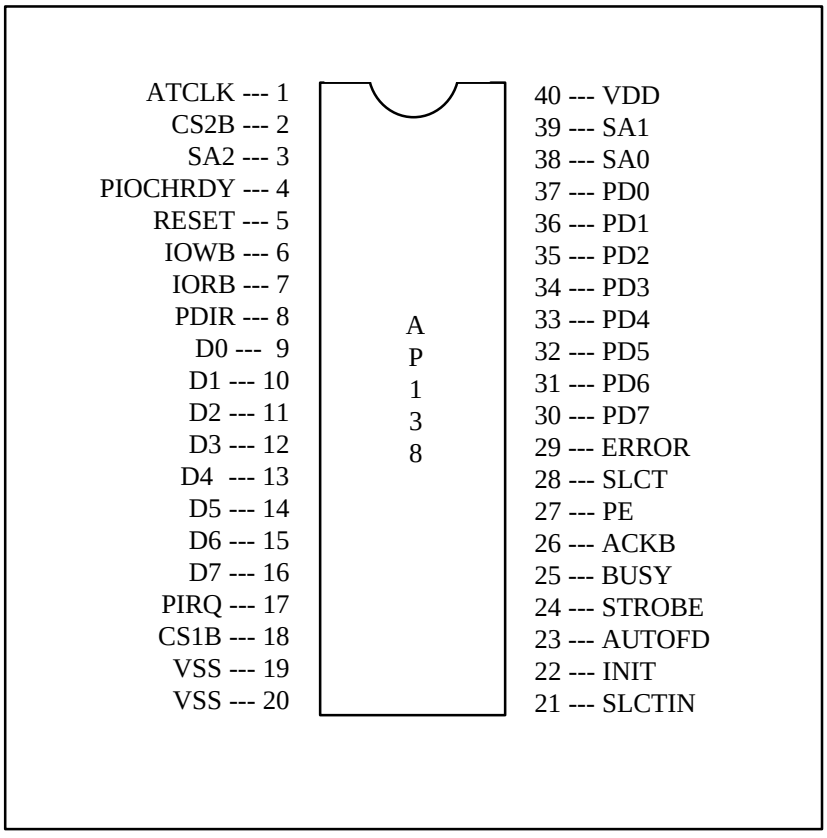
Introduction

AP138 is a parallel port interface between PC and peripherals. This interface can be configured into standard printer mode (SPP), bi-directional mode (BIDI) and enhanced parallel port (EPP) mode. These modes are IEEE P1284 compliant. AP138 is an enhanced version of previous AP138 in which more control bits are added to provide more flexibility such as EPP1.7 support, programmable parallel port I/O characteristics etc. However, AP138 is pin-to-pin compatible to AP138.

Pin Assignment

40 PIN DIP PACKAGE

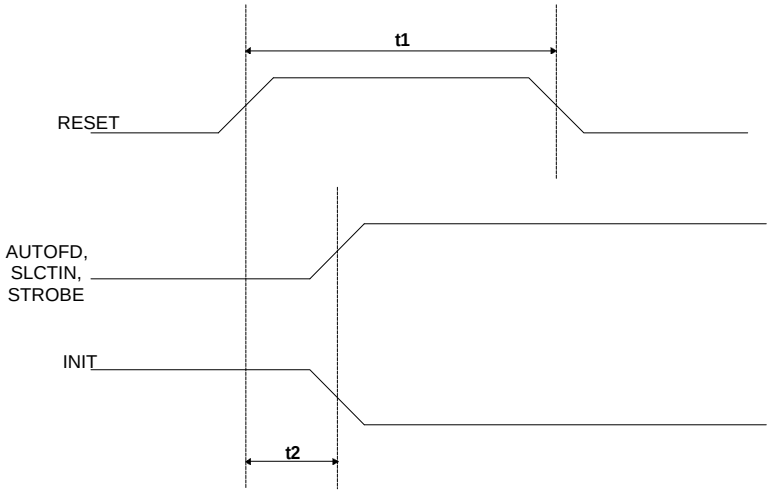


Pin #	Pin Names	Type	Descriptions
1	ATCLK	I	8 Mhz clock input from AT bus
2	CS2B	I	Config. register select
3	SA2	I	A2 from ISA Bus
4	PIOCHRDY	OD (12mA)	I/O channel ready
5	RESET	I (schmitt)	Chip reset
6	IOWB	I	I/O Write
7	IORB	I	I/O Read
8	PDIR	I/O (4mA)	RESET=1; Hardware selection for EPP mode; 1 = EPP mode, 0 = Standard mode RESET=0; Printer data bus direction; 0=output to printer, 1 = input from printer
9-16	D0-D7	I/O (12mA)	ISA data bus
17	PIRQ	O (12mA)	Interrupt request to Host
18	CS1B	I	Parallel port register select
19	VSS		Ground
20	VSS		Ground
21	SLCTIN	I/O (20mA)	Standard Mode : Printer select control to printer EPP Mode : ADDSTRB# signal to printer for data strobing during address read/write operations
22	INIT	I/O (20mA)	Peripheral Reset
23	AUTOFD	I/O (20mA)	Standard Mode : Auto-line feed control to printer EPP Mode : DATASTB# signal to printer for data strobing during data read/write operations
24	STROBE	I/O (20mA)	Standard Mode : Data strobe to printer EPP Mode : WRITE# signal to printer indicating read or write operations
25	BUSY	I (Schmitt)	Standard Mode : Busy status from printer
26	ACKB	I (Schmitt)	Standard Mode : Acknowledge signal from printer EPP Mode : Peripheral interrupt from printer
27	PE	I (Schmitt)	Paper end status from printer
28	SLCT	I (Schmitt)	Printer select status from printer
29	ERROR	I (Schmitt)	Error status line from printer
30-37	PD7-PD0	I/O (20mA)	Printer data bus
38	SA0	I	A0 from ISA Bus
39	SA1	I	A1 from ISA Bus
40	VDD		+5v power

*All inputs are of TTL type if not explicitly specified.
*All outputs have sink and source current specified at 0.4v and 2.4v respectively.
*All outputs have source current equal to half of the sink current.

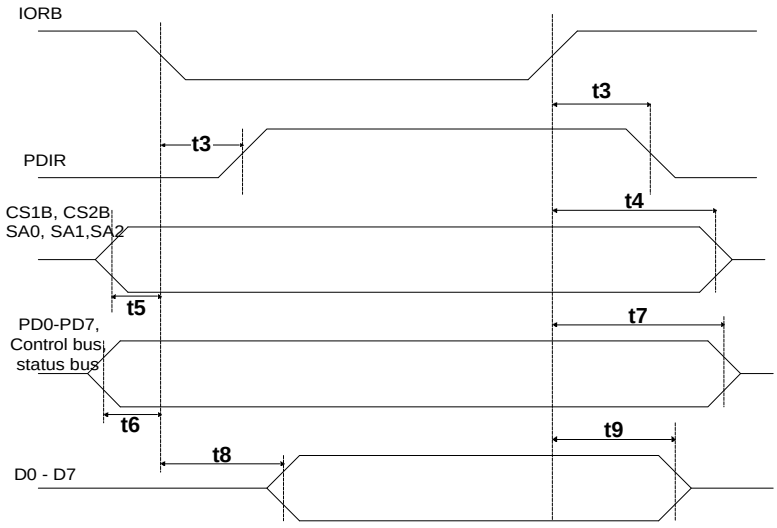
TIMING DIAGRAM

Reset Waveform

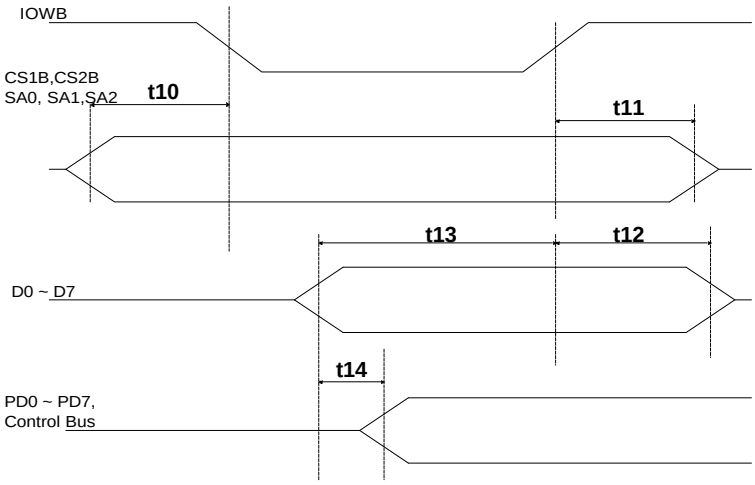


Waveforms in SPP and PS/2 mode

Read cycle



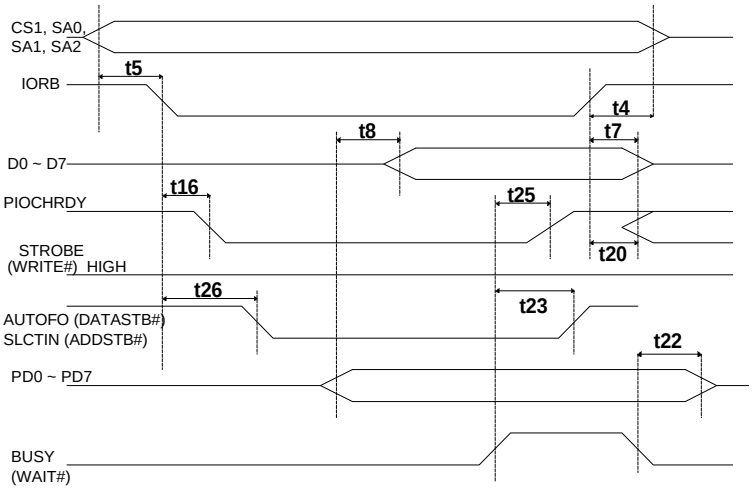
Write Cycle



Note : Control Bus includes AUTOFD, SLCTIN, STROBE and INIT.
Status Bus includes ERROR, SLCT, PE, ACKB and BUSY.

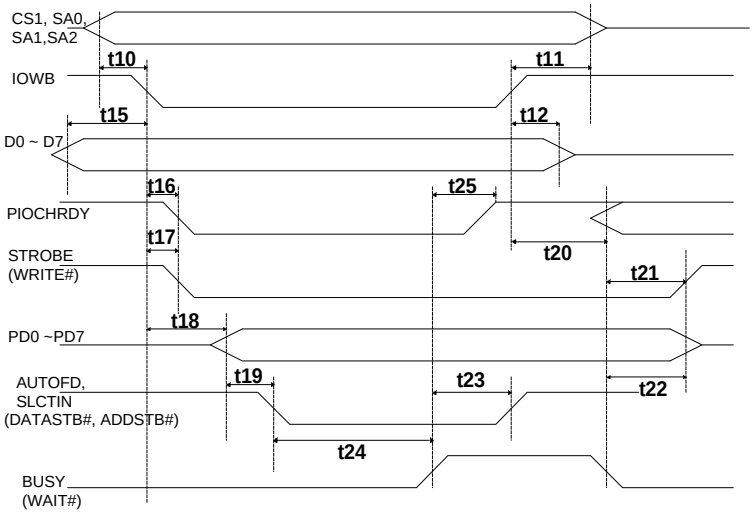
WAVEFORMS IN EPP MODE

Data or Address Read Cycle



Note : Signal names shown in brackets are used in EPP mode.

Data or Address Write Cycle



SYM	DESCRIPTION	MAX	MIN	UNIT
t1	Min. Reset pulse width		300	ns
t2	Printer control signals reset delay	60		ns
t3	DELAY from IORB to PDIR	35		ns
t4	Chip select and address hold time from IORB		20	ns
t5	Chip select and address setup time to IORB		40	ns
t6	Printer data bus, control bus and status bus setup time to IORB		0	ns
t7	Printer data bus, control bus and status bus hold time from IORB		0	ns
t8	Delay from printer data bus, control bus or status bus to system data bus	100		ns
t9	Delay from IORB rising edge to system data bus floating	30		ns
t10	Chip select and address setup time to IOWB		40	ns
t11	Chip select and address hold time to IOWB		20	ns
t12	System data bus hold time from IOWB		30	ns
t13	System data bus setup time to IOWB rising edge		70	ns
t14	Delay from system data bus to printer data bus or control bus during write cycle	10		ns
t15	System data bus setup time in EPP write cycle		0	ns
t16	Delay from IOWB/IORB to PIOCHRDY low	24		ns
t17	Delay from IOWB to STROBE (WRITE#) low	24		ns
t18	Delay from IOWB to printer data valid	50		ns
t19	Delay from printer data valid to AUTOFD(DATASTR#) or SLCTIN (ADDSTRB#) low	10		ns
t20	Delay from IOWB high to PIOCHRDY floating	10		ns
t21	Delay from BUSY (WAIT#) low to STROBE (WRITE#) high	10		ns
t22	Delay from BUSY (WAIT#) low to printer data bus valid	10		ns
t23	Delay from BUSY (WAIT#) to AUTOFD (DATASTB#) or SLCTIN (ADDSTR#) high	10		ns
t24	Max. allowed delay from AUTOFD (DATASTB#) or SLCTIN (ADDSTB#) low to BUSY (WAIT#) high	10	0	ns
t25	Delay from BUSY (WAIT#) to PIOCHRDY high	10		ns
t26	Delay from IORB to AUTOFD (DATASTB#) or SLCTIN (ADDSTB#) low	20		ns

ADDRESS DECODING FOR INTERNAL REGISTERS

AP138 has nine internal registers which can be selected by using CS2B, CS1B, SA0, SA1 and SA2 pins. The following is the decoding map of the registers.

CS2B	CS1B	SA2	SA1	SA0	Registers Selected	Note
1	0	0	0	0	Data Port	1
1	0	0	0	1	Status Port	1,3
1	0	0	1	0	Control Port	1
1	0	0	1	1	EPP Address Port	2
1	0	1	0	0	EPP Data Port 0	2
1	0	1	0	1	EPP Data Port 1	2
1	0	1	1	0	EPP Data Port 2	2
1	0	1	1	1	EPP Data Port 3	2
0	1	0	1	0	Config. Register	1
0	1	0	1	1	Secret Config. Register	4

Note 1: Register is available in all modes.
Note 2: Register is available in EPP modes only.
Note 3: Port is for Read only.
Note 4: Register is available when Config. Register is programmed as `b11100000.

REGISTER BIT MAP

	D0	D1	D2	D3	D4	D5	D6	D7
Data Port	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7
Status Port	TMOUT	0	0	#ERR	SLCT	PE	#ACK	#BUSY
Control Port	STROBE	AUTOFD	#INIT	SLCTIN	IRQEN	PCD	0	0
EPP ADDR. Port	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7
EPP Data Port 0-3	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7
Config. Register	--	--	--	--	--	M0	M1	M2
Secret Config. Reg.	--	--	--	--	--	ETYPE	OD	EPPSEL

REGISTER DESCRIPTIONS

1. Data Port

The data register is cleared at initialization by RESET. During a write operation, the Data Register latches the contents of the data bus with the rising edge of IOWB input. The contents of this register are buffered (non-inverting) and output onto the PD0-PD7 ports. During a READ operation standard parallel port (SPP) mode, PD0-PD7 ports are buffered (not latched) and output to the host CPU.

2. Status Port

The contents of the status port are sent to CPU during a read operation.

Bit 0 -- TMOUT	This bit is valid in EPP mode only and indicates that a 10μs time out has occurred during an EPP cycle. A logic 1 means a time out error has been detected. This bit will be self-cleared during a write operation.
Bit 1,2	Always ZERO
Bit 3 -- #ERR	The level on ERROR input is read by the CPU as bit 3 of the status port.
Bit 4 -- SLCT	The level on SLCT input is read by the CPU as bit 4 of the status port.
Bit 5 -- PE	The level on PE input is read by the CPU as bit 5 of the status port.
Bit 6 -- #ACK	The level on ACKB input is read by the CPU as bit 6 of status port.
Bit 7 -- #BUSY	The complement of the level on the BUSY input is read by the CPU as bit 7 of the status port.

3. Control Port

The control register is initialized by the RESET input, with only bits 0 to 5 affected; bit 6 and 7 are always zero.

Bit 0 -- STROBE	This bit is inverted and output onto the STROBE output.
Bit 1 -- AUTOFD	This bit is inverted and output onto the AUTOFD output.
Bit 2 -- #INIT	This bit is output onto the INIT output without inversion.
Bit 3 -- SLCTIN	This bit is inverted and output onto the SLCTIN output.

Bit 4 -- IRQEN — This is the interrupt request enable bit which enables interrupt requests from the parallel port to the CPU. When it is set to high, interrupt is generated at the rising edge of ACKB input. When it is set to low, interrupt is disabled.

Bit 5 -- PCD — This bit is used to control the data flow direction between the parallel port and the connected device. A logic 0 sets the parallel port in output mode; a logic 1 sets the parallel port in input mode. In EPP mode, a logic '0' must be set in order to function properly.

Bit 6,7 — Always ZERO

4. EPP Address Port

The address register is cleared at initialization by RESET. During a WRITE operation, the contents of D0-D7 are buffered (non-inverting) and output onto the PD0-PD7 bus, the leading of IOWB causes an EPP address write cycle to be performed. The trailing edge of IOWB latches the data for the duration of the EPP write cycle. During a read operation, PD0-PD7 bus is read. The leading edge of IORB causes an EPP address read cycle to be performed and the data output to the host CPU. The deassertion of SLCTIN (ADDSTB#) latches PD0-PD7 for the duration of the IORB cycle. This register is only available in EPP mode.

5. EPP Data Port 0-3

The data registers are cleared at initialization by RESET. During a WRITE operation, the contents of PD0-PD7 are buffered (non-inverting) and output onto the PD0-PD7 bus. The leading edge of IOWB causes an EPP data write cycle to be performed. The trailing edge of IOWB latches the data for the duration of the EPP write cycle. During a READ operation, PD0-PD7 bus is read. The Leading edge of the IORB causes an EPP read cycle to be performed and the data output to the host CPU. The deassertion of AUTOFD (DATASTB#) latches PD0-PD7 for the duration of the IORB cycle. These registers are only available in EPP mode.

6 Config. Register

This register is used to configure the operation mode, and is initialized to standard parallel mode by the RESET input.

M2	M1	M0	Mode
0	0	0	Standard parallel mode
0	0	1	Bi-direction mode
1	0	0	EPP mode
1	1	1	Config. mode

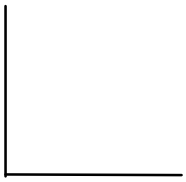
Bit 6 -- OD	Logic ‘1’ sets open-drain control signal outputs while logic ‘0’ sets push-pull control signal outputs. Note that PD7-PD0 are always push-pull output.
Bit 5 -- EPPSEL	Logic ‘1’ would allow M2, M1 and M0 to override EPP mode hardware setting from PDIR pin. Default is ‘0’.

SOFTWARE CONSTRAINTS

Before an EPP cycle is executed, the software must ensure that the control register bit PCD is a logic ‘0’, if the user leaves PCD as a logic “1” and attempts to perform an EPP write, the chip is unable to perform the write and will appear to perform an EPP read on the parallel bus, no error is indicated.

ORDERING INFORMATION

ASP AP138



AP138 = Enhanced Parallel Port Controller
40 PIN P-DIP