1990 BYTE AWARD OF EXCELLENCE

Am286™ZX/Am286LX Integrated Processors

PC-AT Motherboard-on-a-Chip

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Integrates entire IBM PC-AT motherboard logic, plus enhancements**
  - –80C286 Microprocessor Core
  - –Enhanced Bus Controller
  - –Enhanced Clock Generator
  - –DMA Controllers
  - –Interrupt Controllers
  - –Counter/Timer
  - –Real Time Clock and CMOS Static RAM
- **Direct connection to DRAM, AMD 80C287™ math coprocessor, EPROMs, keyboard controller, and AT-bus slots eliminates the need for buffers and other glue logic**
- **Full hardware support for EMS 4.0 memory management with 128 EMS registers allows fast switching for multitasking systems**
- **100% compatible with the IBM PC-AT standard**
- **Low-power operation plus power saving features for battery powered notebook/hand-held systems (Am286LX processor only)**
- **Industry standard I/O port 92H fast reset and GATEA20 features for high-speed switching between real and protected mode**
- **Page mode/interleave DRAM Controller with direct interface to 256-kbit, 1-Mbit, and 4-Mbit DRAMs—supports up to 16 Mb of physical memory**
- **Complete line of support products available including demo boards, ICE, BIOS, and EMS drivers**
- **Flexible clock speeds up to 16 MHz**
- **28mm x 28mm, 216-Pin EIAJ Plastic Quad Flat Pack (PQFP), with socket available**

GENERAL DESCRIPTION

The Am286ZX and Am286LX integrated processors are AMD proprietary PC-AT motherboard-on-a-chip devices for personal computers. They integrate all of the logic functions from the original IBM PC-AT motherboard, plus enhancements, onto one chip. Included are the 80C286 microprocessor, all of the AT standard peripherals, and memory management to provide a high-performance, low-cost, low-power system solution for personal computers. The high level of integration provided by the Am286ZX/LX integrated processor allows designers to reduce the size, power consumption, and cost of a PC-AT compatible system, while increasing functionality and adding features.

The Am286ZX/LX integrated processor is ideal for design of desktop, notebook, handheld, embedded, and other industry standard AT personal computers, where performance, size, power consumption, and cost are critical factors. The Am286LX processor version provides additional power saving features including CPU shutdown mode, system shutdown mode, staggered DRAM refresh, and slow-refresh DRAM support.

Figure 1 shows a system block diagram for an AT motherboard, illustrating the high level of integration achieved by the Am286ZX/LX integrated processor.

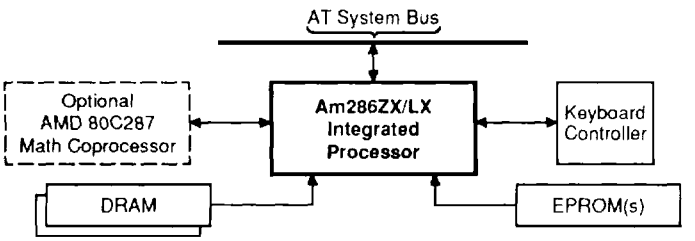

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Figure 1. PC-AT System Block Diagram Using the Am286ZX/LX Integrated Processor

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Issue Date: December 1991

SYSTEM ARCHITECTURE

Figure 2 shows the Am286ZX/LX Integrated Processor Bus Interface. The AT System Bus (S Bus), Memory Bus (M Bus), and the I/O Bus (X Bus) directly interface to the rest of the system components. Optional buffers are shown for applications that require extended S-bus drive capability and/or four DRAM banks. The Am286ZX/LX integrated processor is designed to drive two bus slots and two DRAM banks, without requiring buffers.

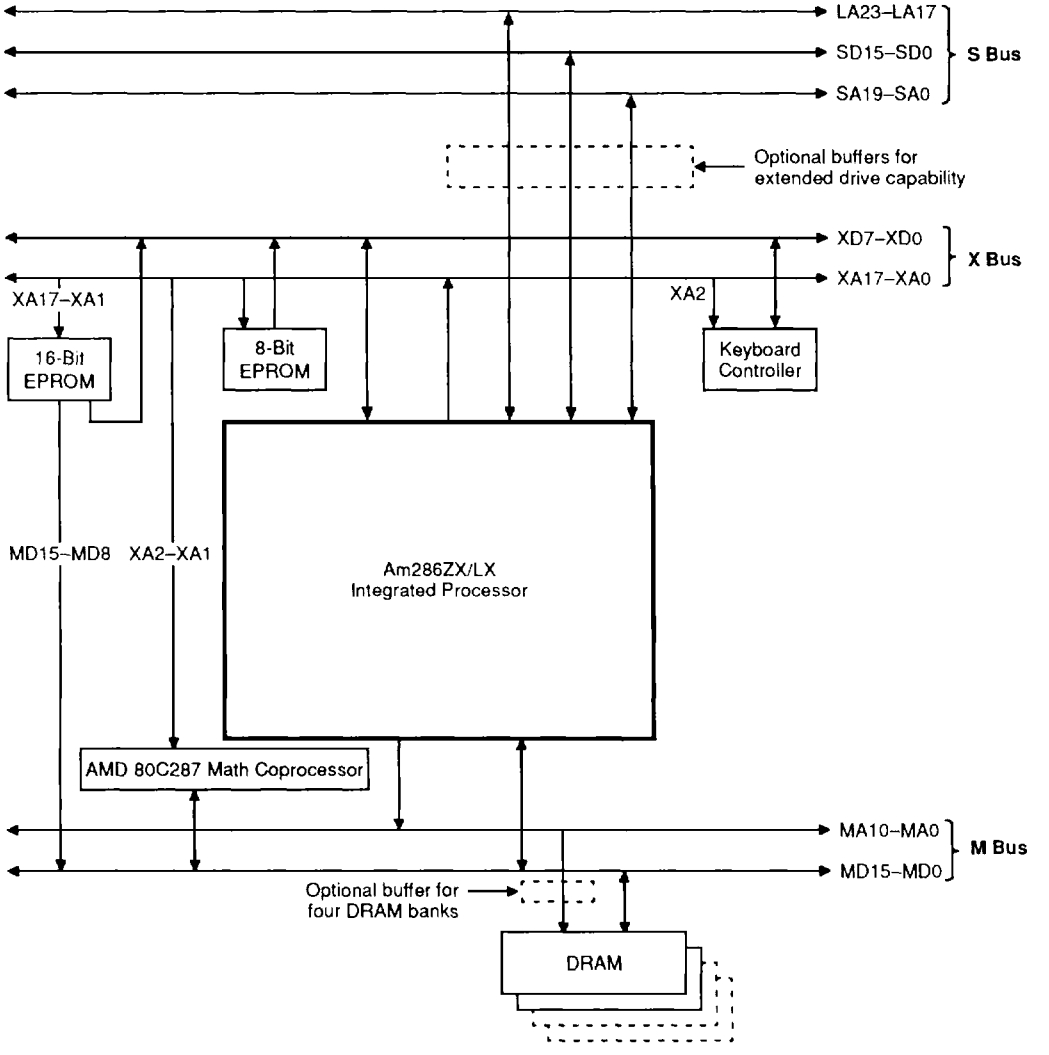

Figure 2. Am286ZX/LX Integrated Processor Bus Interface

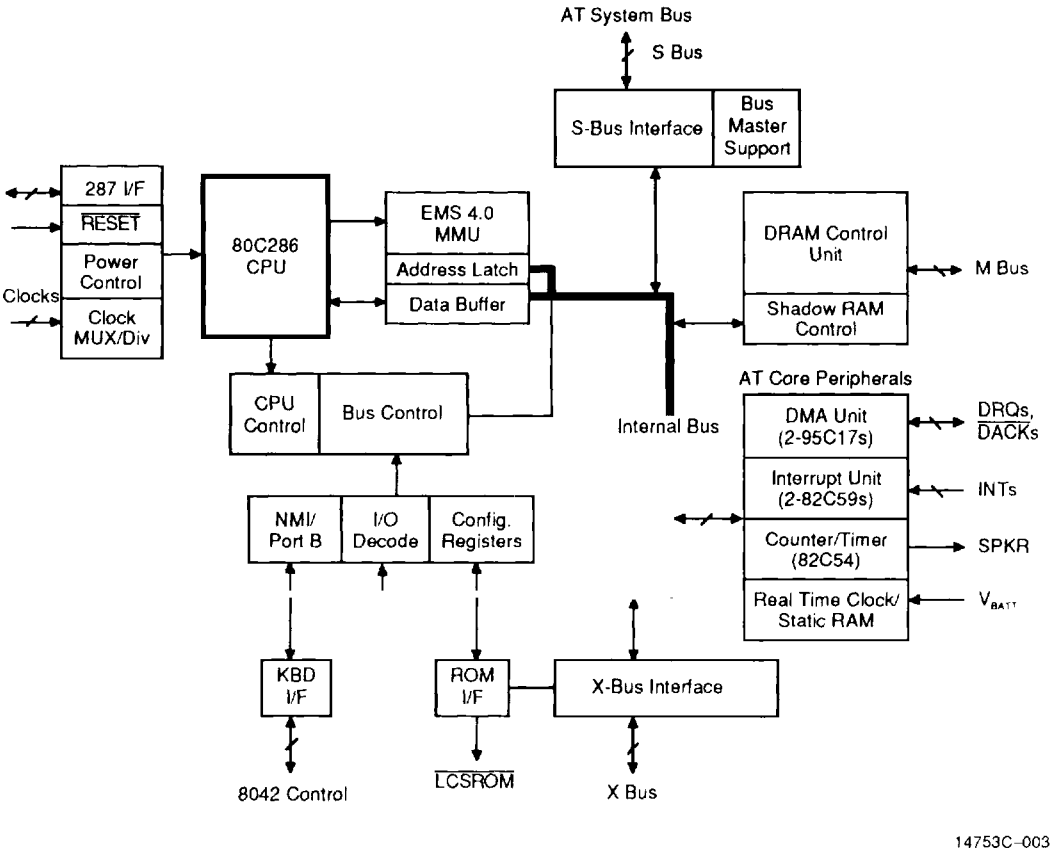

Figure 3. Am286ZX/LX Integrated Processor Internal Block Diagram

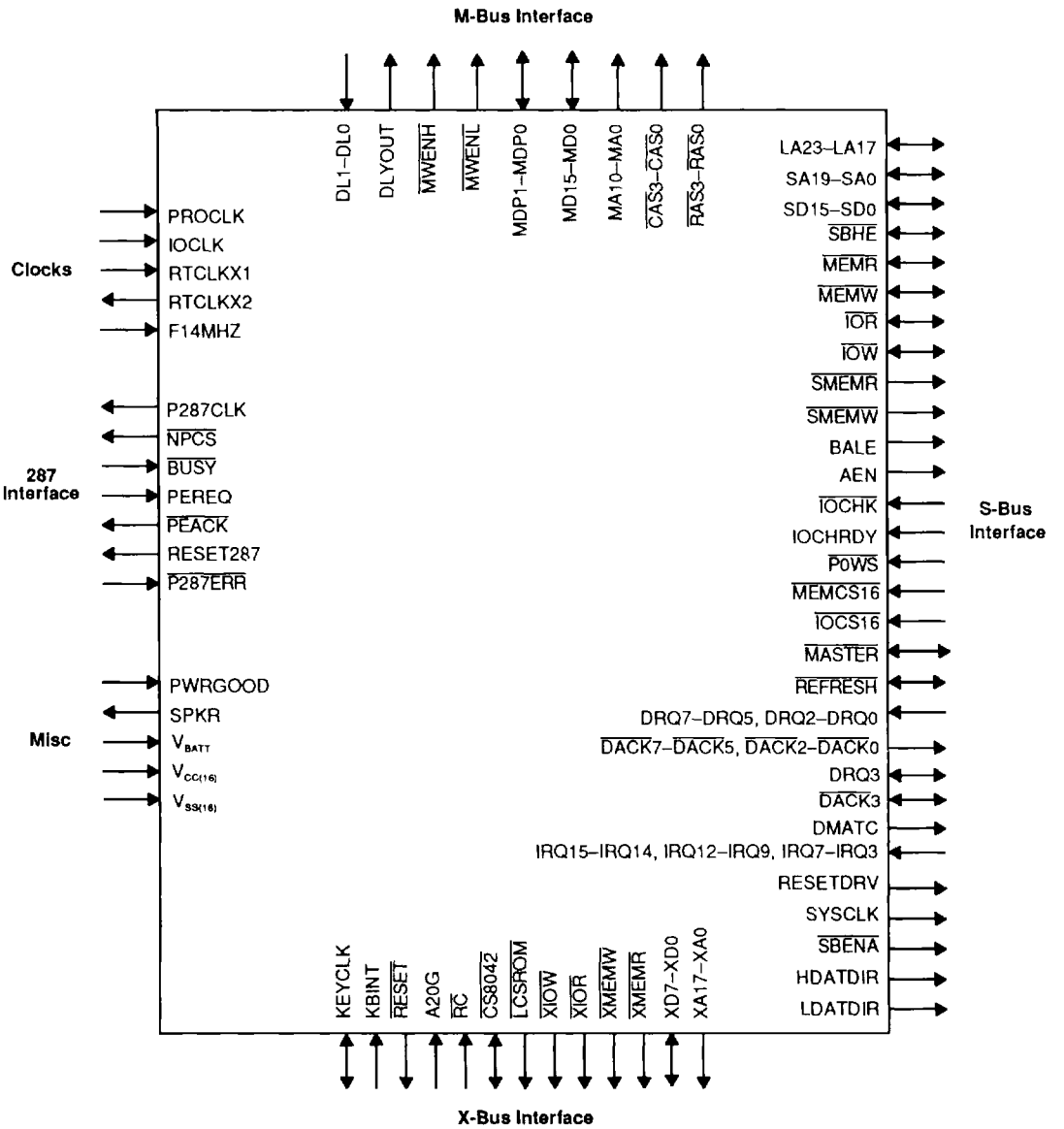

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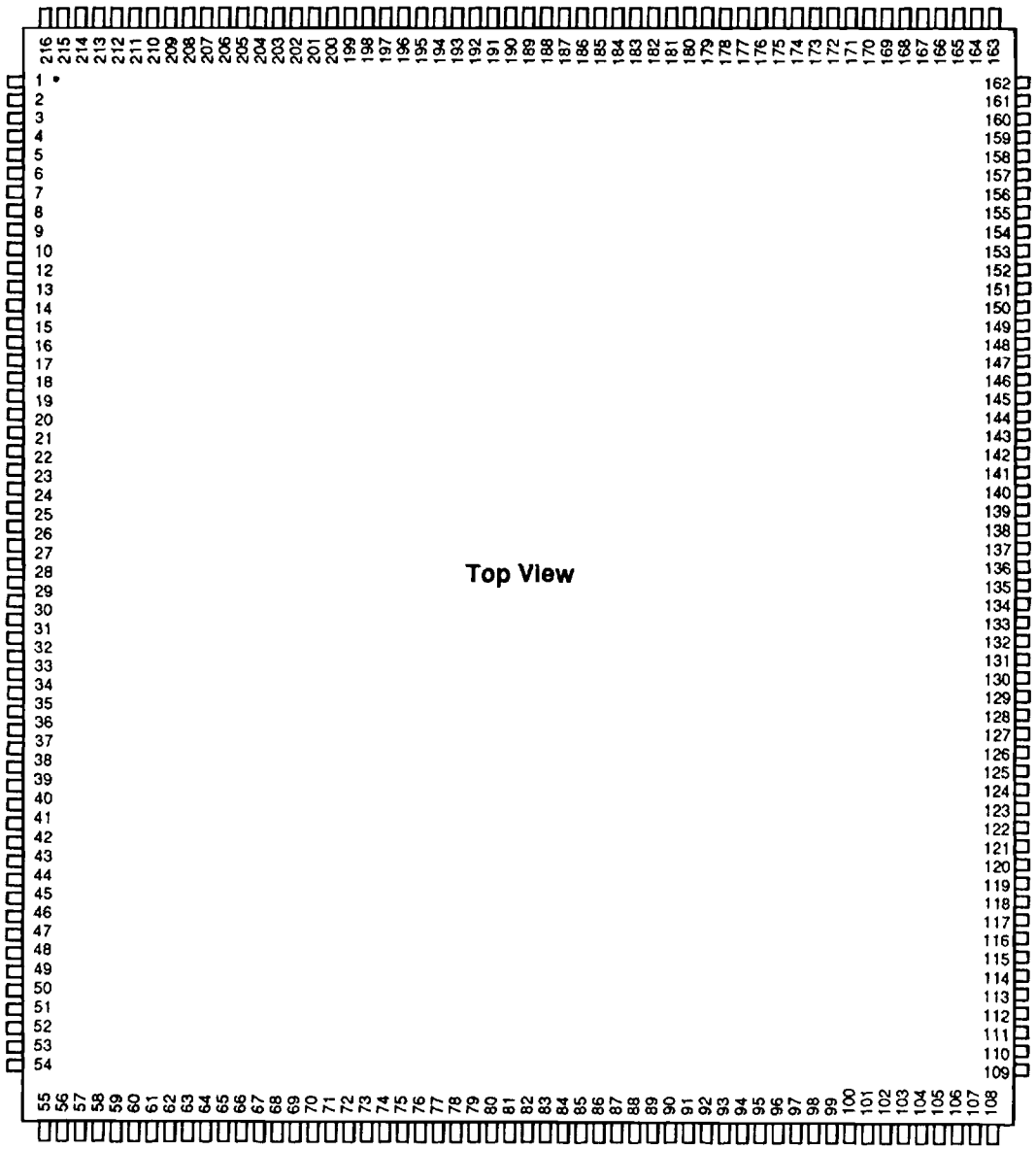
Figure 4. Am286ZX/LX Integrated Processor Logic Symbol



Note: Pin 1 is marked for orientation.

14753C–005

Figure 5. Am286ZX/LX Integrated Processor Connection Diagram

PIN DESIGNATION TABLE (Sorted by Pin Number)

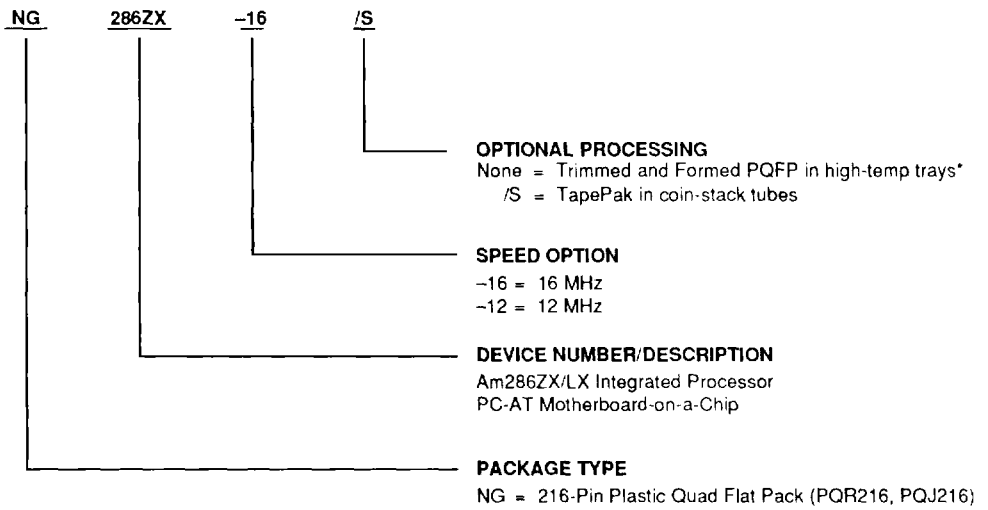
Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	LDATDIR	56	V_{CC}	111	SA18	166	MDP0
2	$\overline{SBENA}$	57	V_{SS}	112	LA18	167	MDP1
3	$\overline{MASTER}$	58	XA12	113	SA19	168	SD0
4	DRQ7	59	XA11	114	LA19	169	SD1
5	$\overline{DACK7}$	60	XA10	115	LA20	170	SD2
6	DRQ6	61	XA9	116	LA21	171	SD3
7	$\overline{DACK6}$	62	XA8	117	LA22	172	SD4
8	DRQ5	63	XA7	118	LA23	173	SD5
9	$\overline{DACK5}$	64	XA6	119	$\overline{RAS0}$	174	SD6
10	DRQ0	65	XA5	120	$\overline{RAS1}$	175	SD7
11	V_{CC}	66	XA4	121	V_{CC}	176	V_{CC}
12	V_{SS}	67	XA3	122	V_{SS}	177	V_{SS}
13	$\overline{DACK0}$	68	XA2	123	$\overline{RAS2}$	178	SD8
14	$\overline{MEMR}$	69	XA1	124	$\overline{RAS3}$	179	SD9
15	$\overline{MEMW}$	70	XA0	125	$\overline{CAS0}$	180	SD10
16	IRQ14	71	V_{CC}	126	$\overline{CAS1}$	181	SD11
17	IRQ15	72	V_{SS}	127	V_{CC}	182	SD12
18	IRQ12	73	MA0	128	V_{SS}	183	SD13
19	IRQ11	74	MA1	129	$\overline{CAS2}$	184	SD14
20	IRQ10	75	MA2	130	$\overline{CAS3}$	185	SD15
21	$\overline{IOCS16}$	76	MA3	131	$\overline{MWENL}$	186	V_{BATT}
22	$\overline{MEMCS16}$	77	MA4	132	$\overline{MWENH}$	187	RTCLKX1
23	$\overline{SBHE}$	78	V_{CC}	133	DLYOUT	188	RTCLKX2
24	BALE	79	V_{SS}	134	DL0	189	V_{CC}
25	DMATC	80	MA5	135	V_{CC}	190	V_{SS}
26	$\overline{DACK2}$	81	V_{CC}	136	V_{SS}	191	$\overline{LCSROM}$
27	V_{CC}	82	V_{SS}	137	DL1	192	$\overline{XMEMW}$
28	V_{SS}	83	MA6	138	XD0	193	$\overline{XMEMR}$
29	IRQ3	84	MA7	139	XD1	194	$\overline{CS8042}$
30	IRQ4	85	MA8	140	XD2	195	$\overline{XIOR}$
31	IRQ5	86	MA9	141	XD3	196	$\overline{XIOW}$
32	IRQ6	87	MA10	142	XD4	197	$\overline{RC}$
33	IRQ7	88	V_{CC}	143	XD5	198	A20G
34	$\overline{REFRESH}$	89	V_{SS}	144	XD6	199	$\overline{RESET}$
35	DRQ1	90	SA0	145	XD7	200	KEYCLK
36	SYSCLK	91	SA1	146	V_{CC}	201	KBINT
37	$\overline{DACK1}$	92	SA2	147	V_{SS}	202	PWRGOOD
38	DRQ3	93	SA3	148	MD0	203	PROCLK
39	$\overline{DACK3}$	94	SA4	149	MD1	204	IOCLK
40	$\overline{IOW}$	95	SA5	150	MD2	205	F14MHZ
41	$\overline{IOR}$	96	SA6	151	MD3	206	V_{CC}
42	$\overline{SMEMW}$	97	SA7	152	MD4	207	V_{SS}
43	$\overline{SMEMR}$	98	SA8	153	MD5	208	SPKR
44	IOCHRDY	99	SA9	154	MD6	209	P287CLK
45	AEN	100	SA10	155	MD7	210	$\overline{NPCS}$
46	$\overline{POWS}$	101	SA11	156	MD8	211	$\overline{BUSY}$
47	DRQ2	102	SA12	157	MD9	212	PEREQ
48	IRQ9	103	SA13	158	MD10	213	$\overline{PEACK}$
49	RESETDRV	104	SA14	159	MD11	214	RESET287
50	$\overline{IOCHK}$	105	SA15	160	V_{CC}	215	$\overline{P287ERR}$
51	XA17	106	SA16	161	V_{SS}	216	HDATDIR
52	XA16	107	SA17	162	MD12		
53	XA15	108	V_{CC}	163	MD13		
54	XA14	109	V_{SS}	164	MD14		
55	XA13	110	LA17	165	MD15		

PIN DESIGNATION TABLE (Sorted by Pin Name)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
A20G	198	LA23	118	RESETDRV	49	V_{CC}	121
AEN	45	$\overline{LCSROM}$	191	RTCLKX1	187	V_{CC}	127
BALE	24	LDATDIR	1	RTCLKX2	188	V_{CC}	135
$\overline{BUSY}$	211	MA0	73	SA0	90	V_{CC}	146
$\overline{CAS0}$	125	MA1	74	SA1	91	V_{CC}	160
$\overline{CAS1}$	126	MA2	75	SA2	92	V_{CC}	176
$\overline{CAS2}$	129	MA3	76	SA3	93	V_{CC}	189
$\overline{CAS3}$	130	MA4	77	SA4	94	V_{CC}	206
$\overline{CS8042}$	194	MA5	80	SA5	95	V_{SS}	12
$\overline{DACK0}$	13	MA6	83	SA6	96	V_{SS}	28
$\overline{DACK1}$	37	MA7	84	SA7	97	V_{SS}	57
$\overline{DACK2}$	26	MA8	85	SA8	98	V_{SS}	72
$\overline{DACK3}$	39	MA9	86	SA9	99	V_{SS}	79
$\overline{DACK5}$	9	MA10	87	SA10	100	V_{SS}	82
$\overline{DACK6}$	7	$\overline{MASTER}$	3	SA11	101	V_{SS}	89
$\overline{DACK7}$	5	MD0	148	SA12	102	V_{SS}	109
DL0	134	MD1	149	SA13	103	V_{SS}	122
DL1	137	MD2	150	SA14	104	V_{SS}	128
DLYOUT	133	MD3	151	SA15	105	V_{SS}	136
DMATC	25	MD4	152	SA16	106	V_{SS}	147
DRQ0	10	MD5	153	SA17	107	V_{SS}	161
DRQ1	35	MD6	154	SA18	111	V_{SS}	177
DRQ2	47	MD7	155	SA19	113	V_{SS}	190
DRQ3	38	MD8	156	$\overline{SBENA}$	2	V_{SS}	207
DRQ5	8	MD9	157	$\overline{SBHE}$	23	XA0	70
DRQ6	6	MD10	158	SD0	168	XA1	69
DRQ7	4	MD11	159	SD1	169	XA2	68
F14MHZ	205	MD12	162	SD2	170	XA3	67
HDATDIR	216	MD13	163	SD3	171	XA4	66
$\overline{IOCHK}$	50	MD14	164	SD4	172	XA5	65
IOCHRDY	44	MD15	165	SD5	173	XA6	64
IOCLK	204	MDP0	166	SD6	174	XA7	63
$\overline{IOCS16}$	21	MDP1	167	SD7	175	XA8	62
$\overline{IOR}$	41	$\overline{MEMCS16}$	22	SD8	178	XA9	61
$\overline{IOW}$	40	$\overline{MEMR}$	14	SD9	179	XA10	60
IRQ3	29	$\overline{MEMW}$	15	SD10	180	XA11	59
IRQ4	30	$\overline{MWENH}$	132	SD11	181	XA12	58
IRQ5	31	$\overline{MWENL}$	131	SD12	182	XA13	55
IRQ6	32	$\overline{NPCS}$	210	SD13	183	XA14	54
IRQ7	33	$\overline{P0WS}$	46	SD14	184	XA15	53
IRQ9	48	P287CLK	209	SD15	185	XA16	52
IRQ10	20	$\overline{P287ERR}$	215	$\overline{SMEMR}$	43	XA17	51
IRQ11	19	$\overline{PEACK}$	213	$\overline{SMEMW}$	42	XD0	138
IRQ12	18	PEREQ	212	SPKR	208	XD1	139
IRQ14	16	PROCLK	203	SYSCLK	36	XD2	140
IRQ15	17	PWRGOOD	202	V_{BATT}	186	XD3	141
KBINT	201	$\overline{RAS0}$	119	V_{CC}	11	XD4	142
KEYCLK	200	$\overline{RAS1}$	120	V_{CC}	27	XD5	143
LA17	110	$\overline{RAS2}$	123	V_{CC}	56	XD6	144
LA18	112	$\overline{RAS3}$	124	V_{CC}	71	XD7	145
LA19	114	$\overline{RC}$	197	V_{CC}	78	$\overline{XIOR}$	195
LA20	115	$\overline{REFRESH}$	34	V_{CC}	81	$\overline{XIOW}$	196
LA21	116	$\overline{RESET}$	199	V_{CC}	88	$\overline{XMEMR}$	193
LA22	117	RESET287	214	V_{CC}	108	$\overline{XMEMW}$	192

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the items below:



Valid Combinations	
NG286LX	–12, –12/S
	–16, –16/S
NG286ZX	–12, –12/S
	–16, –16/S

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released valid combinations.

*Note: Order Trimmed and Formed PQFP in multiples of 24 units/tray, 4 trays/dry pack.

PIN DESCRIPTION

Clocks

PROCLK
Processor Clock (Input)

Processor clock supplies a clock to the clock divider and multiplexer logic.

IOCLK
I/O Clock (Input)

I/O clock supplies a clock to the clock divider and multiplexer logic.

F14MHZ
14.318-MHz Frequency (Input)

14.318-MHz Frequency input to a divider that generates the clock for the internal 82C54 counter/timer.

RTCLKX1
RTC X1 Crystal Connection (Input)

Input to the crystal oscillator that supplies the internal real-time clock's 32-kHz frequency.

RTCLKX2
RTC X2 Crystal Connection (Output)

Output of the crystal oscillator that supplies the internal real-time clock's 32-kHz frequency.

AT System Bus (S Bus) Interface

SYSCLK
System Clock (Output)

System Clock is the S-bus synchronous clock. It is always half the frequency of the AT state machine clock.

LA23–LA17
Extended Address (Inputs/Outputs)

Extended Address lines are used to address up to 16 Mb of memory on the S Bus. These signals are not latched internally with BALE and are valid earlier in the cycle than the SA lines. These pins can be driven by the internal CPU or DMA controller or by an external bus master.

SA19–SA0
S-Bus Address (Inputs/Outputs)

S-Bus Address lines are used to address memory and I/O devices on the S Bus and are valid for the entire bus cycle. These pins can be driven by the internal CPU or DMA controller or by an external bus master.

$\overline{\text{SBHE}}$
S-Bus Byte High Enable (Input/Output; Active Low)

S-Bus Byte High Enable signal indicates a transfer of data on the upper byte of the data bus, SD15–SD8, to a 16-bit, S-bus peripheral. This signal can be driven by the internal CPU or DMA controller or by an external bus master.

SD15–SD0
S-Bus Data (Inputs/Outputs)

S-Bus Data lines are used to transfer data on the S Bus. All 8-bit devices use SD7–SD0. All 16-bit devices use SD15–SD0. Transfers may be initiated by the internal CPU or DMA controller or by an external bus master.

BALE
Buffered Address Latch Enable (Output; Active High)

Buffered Address Latch Enable is an active High output used to latch valid addresses and memory decodes during CPU transfer cycles. BALE is forced High during DMA and external bus master cycles.

$\overline{\text{IOW}}$
I/O Write (Input/Output; Active Low)

I/O Write is an active Low control signal for I/O write cycles on the S Bus. This signal can be driven by the internal CPU or DMA controller or by an external bus master.

$\overline{\text{IOR}}$
I/O Read (Input/Output; Active Low)

I/O Read is an active Low control signal for I/O read cycles on the S Bus. This signal can be driven by the internal CPU or DMA controller or by an external bus master.

$\overline{\text{MEMW}}$
Memory Write (Input/Output; Active Low)

Memory Write is an active Low control signal for all memory write cycles on the S Bus. This signal can be driven by the internal CPU or DMA controller or by an external bus master.

$\overline{\text{MEMR}}$
Memory Read (Input/Output; Active Low)

Memory Read is an active Low control signal for all memory read cycles on the S Bus. This signal can be driven by the internal CPU or DMA controller or by an external bus master.

$\overline{\text{SMEMW}}$
S-Memory Write (Output; Active Low)

S-Memory Write is an active Low control signal for write cycles to S-bus memory with addresses less than 1Mb.

$\overline{\text{SMEMR}}$
S-Memory Read (Output; Active Low)

S-Memory Read is an active Low control signal for read cycles to S-bus memory with addresses less than 1Mb.

$\overline{\text{MEMCS16}}$
Memory 16-Bit Chip Select (Input; Active Low)

Memory 16-Bit Chip Select is an active Low input signal indicating that the present S-bus transfer cycle is a 16-bit memory cycle. This pin should be driven by open collector or three-state buffers. There is an internal pull-up on the pin which can be disabled.

$\overline{\text{IOCS16}}$
I/O 16-Bit Chip Select (Input; Active Low)

I/O 16-Bit Chip Select is an active Low input signal indicating that the present S-bus transfer cycle is a 16-bit I/O cycle. This pin is also sampled at reset time to determine ROM size. This pin should be driven by open collector or three-state buffers. There is an internal pull-up on the pin which can be disabled.

$\overline{\text{P0WS}}$
Zero Wait State (Input; Active Low)

Zero Wait State is an active Low input signal indicating to the bus controller that it can complete the present bus cycle without inserting any additional wait states. This pin should be driven by open collector or three-state buffers. There is an internal pull-up on the pin which can be disabled.

$\overline{\text{IOCHK}}$
I/O Channel Check (Input; Active Low)

I/O Channel Check is an active Low input from the S Bus which can cause a NMI to be generated to the internal CPU, indicating a I/O error condition on the S Bus. This pin should be driven by open collector or three-state buffers. There is an internal pull-up on the pin which can be disabled.

IOCHRDY
I/O Channel Ready (Input; Active High)

I/O Channel Ready is an active High signal from the S Bus. When Low it indicates a "not ready" condition and inserts wait states in AT I/O or memory cycles. When High, it allows the current S-bus cycle to complete. This pin should be driven by open collector or three-state buffers. There is an internal pull-up on the pin which can be disabled.

AEN
Address Enable (Output; Active High)

Address Enable is an active High output signal used to indicate to S-bus I/O device address decoders that a DMA cycle is in progress. When active, the internal DMA controller has control of the S-bus address, data, and control pins.

$\overline{\text{MASTER}}$
Master (Input/Output; Active Low)

$\overline{\text{MASTER}}$ is usually an active Low input signal asserted by an external device on the S Bus to allow S-bus peripherals to access system resources as a bus master. In Bus Master Mode, this pin is an output asserted when a mastering cycle is in progress. This pin should be driven by open collector or three-state buffers. There is an internal pull-up on the pin which can be disabled.

DRQ7–DRQ5, DRQ2–DRQ0
DMA Request (Inputs; Active High)

DMA Request signals 7–5 and 2–0 are asynchronous DMA channel request inputs used by peripheral devices to gain access to a DMA service. These pins can also be used by bus masters to gain S-bus control. DRQ2–DRQ0 perform 8-bit DMA transfers and DRQ7–DRQ5 perform 16-bit DMA transfers. There are weak pull-downs on these pins.

DRQ3
DMA Request (Input/Output)

DMA Request 3 is usually defined the same as the other DRQ inputs. In Bus Master Mode, this pin is an output asserted to request bus access on a host system's bus. There is a weak pull-down on this pin.

$\overline{\text{DACK7}}$–$\overline{\text{DACK5}}$, $\overline{\text{DACK2}}$–$\overline{\text{DACK0}}$
DMA Acknowledge (Outputs; Active Low)

DMA Acknowledge signals 7–5 and 2–0 are active Low output pins which acknowledge their corresponding DMA requests.

$\overline{\text{DACK3}}$
DMA Acknowledge 3 (Input/Output; Active Low)

DMA Acknowledge 3 is usually defined the same as the other $\overline{\text{DACK}}$ outputs. In Bus Master Mode, this pin is an input which senses the status of a bus request to the host system.

DMATC
DMA Terminal Count (Output; Active High)

DMA Terminal Count is an active High output signal indicating that terminal count for a DMA channel has been reached.

$\overline{\text{REFRESH}}$
Refresh (Input/Output; Active Low)

$\overline{\text{REFRESH}}$ is an active Low signal to indicate a memory refresh cycle. This signal can be driven by an external bus master. There is an internal pull-up on the pin which can be disabled.

IRQ15–IRQ14, IRQ12–IRQ9, IRQ7–IRQ3
Interrupt Request (Inputs; Active Low)

Interrupt Request input pins signal the internal 82C59 interrupt controllers that an I/O device needs attention. There are weak pull-ups on these pins.

RESETDRV
Reset Drive (Output; Active High)

Reset Drive is an active High signal used to reset or initialize system logic at power-up time. It is synchronous to SYSCLK.

$\overline{\text{SBENA}}$
S-Bus Buffer Enable (Output; Active Low)

S-Bus Buffer Enable is an active Low enable for the S-bus address and data expansion buffers.

HDATDIR
High Data Direction (Output; Active High)

High Data Direction is an active High direction control pin for the high byte of the S-bus data buffer. A logic High on this pin indicates a drive direction out from the chip.

LDATDIR
Low Data Direction (Output; Active High)

Low Data Direction is an active High direction control pin for the low byte of the S-bus data buffer. A logic High on this pin indicates a drive direction out from the chip.

DRAM Interface

$\overline{\text{RAS3}}$–$\overline{\text{RAS0}}$
Row Address Strobe (Outputs; Active Low)

Row Address Strobes are active Low outputs used by the DRAMs as RAS signals to clock in row addresses for each of the 4 possible DRAM banks.

$\overline{\text{CAS3}}$–$\overline{\text{CAS0}}$
Column Address Strobe (Outputs; Active Low)

Column Address Strobes are active Low outputs used by the DRAMs as CAS signals to clock in column addresses for each of the 4 possible DRAM banks.

MA10–MA0
Memory Address (Outputs)

Memory Address lines are multiplexed outputs and convey the following information: row addresses during RAS signals, column addresses during CAS signals, and refresh addresses during refresh cycles. 256-kbit DRAMs use MA8–MA0; 1-Mbit DRAMs use MA9–MA0; and, 4-Mbit DRAMs use MA10–MA0.

MD15–MD0
Memory Data (Inputs/Outputs)

Memory Data bus transfers data to/from the DRAMs and the AMD 80C287 math coprocessor. The high byte of the bus, MD15–MD8, is also used for transfers involving 16-bit ROM and 16-bit X-bus I/O devices.

MDP1–MDP0
Memory Data Parity (Inputs/Outputs)

Memory Data Parity bits 1 and 0 transfer parity bit information to/from the optional parity DRAM. Parity is generated and verified internally. MDP0 is the parity for the low byte and MDP1 is the parity for the high byte.

$\overline{\text{MWENH}}$
Memory Write Enable High (Output; Active Low)

Memory Write Enable High is an active Low output for the high byte DRAM write enable.

$\overline{\text{MWENL}}$
Memory Write Enable Low (Output; Active Low)

Memory Write Enable Low is an active Low output for the low byte DRAM write enable.

DLYOUT
Delay Line Out (Output; Active High)

Delay Line Out is an active High output to the delay line for generating DRAM control signals.

DL1–DL0
Delay Line (Inputs; Active High)

Delay Line inputs 1 and 0 are active High inputs from two taps of a delay line that generate DRAM control signals.

X-Bus Interface

XA17–XA0
X-Bus Address (Outputs)

X-Bus Address lines provide addressing for the BIOS ROM, keyboard controller, AMD 80C287 math coprocessor, and other X-bus peripherals.

XD7–XD0
X-Bus Data (Inputs/Outputs)

X-Bus Data lines are used to transfer the low 8 bits of data to/from X-bus devices such as the keyboard controller, BIOS ROM, and other X-bus peripherals.

$\overline{\text{XIOW}}$
X-Bus I/O Write (Output; Active Low)

X-Bus I/O Write is an active Low control signal directing an I/O port to accept data from the XD Bus.

$\overline{\text{XIOR}}$
X-Bus I/O Read (Output; Active Low)

X-Bus I/O Read is an active Low control signal directing an I/O port to place data on the XD Bus.

$\overline{\text{XMEMW}}$
X-Bus Memory (Output; Active Low)

X-Bus Memory Write is an active Low control signal for memory write cycles on the X Bus.

$\overline{\text{XMEMR}}$
X-Bus Memory Read (Output; Active Low)

X-Bus Memory Read is an active Low control signal for memory read cycles on the X Bus, such as BIOS ROM reads.

Coprocessor Interface

P287CLK
287 Clock (Output)

287 Clock provides the output clock to the math coprocessor (AMD 80C287 math coprocessor). The clock is generated by the clock divider and multiplexer logic, and is derived from PROCLK or IOCLK.

$\overline{\text{NPCS}}$
Numeric Processor Chip Select (Output; Active Low)

Numeric Processor Chip Select is an active Low output which indicates a data transfer involving the AMD 80C287 math coprocessor.

$\overline{\text{BUSY}}$
Busy (Input; Active Low)

$\overline{\text{BUSY}}$ is an active Low input from the AMD 80C287 math coprocessor indicating it is executing an instruction. There is a weak internal pull-up resistor on this pin.

PEREQ
Processor Extension Request (Input; Active High)

Processor Extension Request is an active High input pin which indicates that the AMD 80C287 math coprocessor is ready to transfer data to/from the CPU. There is a weak pull-down on this pin.

$\overline{\text{PEACK}}$
Processor Extension Acknowledge (Output; Active Low)

Processor Extension Acknowledge is an active Low output which indicates that the requested transfer due to an active PEREQ has been completed.

RESET287
287 Reset (Output; Active High)

287 Reset is an active High output signal which resets the AMD 80C287 math coprocessor.

$\overline{\text{P287ERR}}$
287 Error (Input; Active Low)

287 Error is an active Low input which indicates an AMD 80C287 math coprocessor error condition and can trigger the coprocessor interrupt to the interrupt controller. There is a weak pull-up on this pin.

Keyboard Controller Interface

$\overline{\text{CS8042}}$
8042 Chip Select (Input/Output; Active Low)

8042 Chip Select is an active Low signal used for selecting the external keyboard controller. If the XT keyboard interface is enabled, the pin definition changes to XTKBDATA, a bi-directional serial data transfer line with an internal pull-up.

$\overline{\text{RC}}$
Reset CPU (Input; Active Low)

Reset CPU is an active Low input signal which will activate the internal CPU's reset when active. This is generated from the 8042 keyboard controller.

A20G
Address 20 Gate (Input)

Address 20 Gate input for CPU address line 20. A logic High on this input will enable A20 pass-through from the CPU. A logic Low will force the internal A20 inactive. This signal is generated by the 8042 keyboard controller.

$\overline{\text{RESET}}$
Reset (Output; Active Low)

$\overline{\text{RESET}}$ is an active Low output, CPU clock synchronized reset signal derived from PWRGOOD. It is usually used to reset the keyboard controller. If the XT keyboard interface is enabled, the pin definition changes to XTKBRST, an I/O controlled reset output for an XT keyboard.

KEYCLK
Keyboard Clock (Input/Output)

Keyboard Clock provides the output clock to the keyboard controller. The clock is generated by the clock divider and multiplexer logic and can be derived from several clock sources. If the XT keyboard interface is enabled, the pin definition changes to XTKBCLK, an I/O controlled clock line with an internal pull-up.

KBINT
Keyboard Interrupt (Input)

Keyboard Interrupt is a direct connection to the IRQ1 input on the master 82C59A.

Miscellaneous Signals

$\overline{\text{LCSROM}}$
ROM Chip Select (Output; Active Low)

ROM Chip Select is an active Low output which provides the chip select for the BIOS ROM/EPROM.

PWRGOOD
Power Good (Input; Active High)

Power Good is an active High input signal which indicates a stable system power condition. This is normally driven by the power supply. A logic Low on this input resets the device. There is a schmitt trigger input on this pin.

SPKR
Speaker (Output)

Speaker output signal is the output of the internal tone generation logic which includes one channel of the internal 82C54 timer. This is a standard TTL level output.

V_{BATT}

Negative Battery Voltage input to power the internal Real Time Clock and CMOS memory.

V_{CC}

Power.

V_{SS}

Ground.

FUNCTIONAL DESCRIPTION

80C286 and Standard Peripherals

80C286 Microprocessor Core

The Am286ZX/LX integrated processor integrates AMD's CMOS 80C286 microprocessor as the core of the internal system. The 80C286 core maintains the complete functional features of a standard 80C286. This includes full 80286 instruction set, registers, status information, internal memory organization, 16 Mb of physical and 1 Gb of virtual address space, all addressing modes, address and data segmentation, pipelining schemes, real and protected mode environments with four levels of memory protection, interrupt priorities, and halt and shut down cycles. See the 80C286 data sheet (*order #11625*) *for more information.*

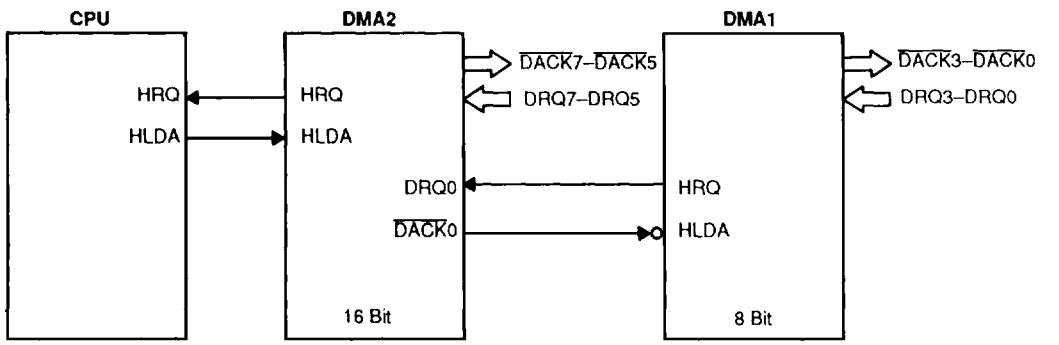
In the Am286ZX/LX integrated processor, the core is designed to be fully static. This means that the Am286ZX/LX integrated processor can operate anywhere from its maximum speed down to 0 MHz. Power consumption is significantly reduced by lowering the clock speed. For maximum power saving, the clock may be shut off completely. The Am286ZX/LX integrated processor retains its state while the processor and peripheral clocks are stopped, and then continues to operate from its original state when these clocks are resumed.

DMA Controllers

Two identical 9517/8237-compatible DMA controllers and a page register are integrated into the Am286ZX/LX integrated processor. DMA1 occupies addresses 000H–00FH and DMA2 occupies addresses 0C0H –0DFH. Each controller is a four channel DMA device which generates the memory addresses and control signals necessary to directly transfer information between a peripheral device and memory. This allows transfer of information at higher speeds with little CPU intervention. The two DMA controllers are internally cascaded to provide four DMA channels for 8-bit transfers (DMA1) and three DMA channels for 16-bit transfers (DMA2). DMA2 Channel 0 is internally cascaded.

The programmable registers in the Am286ZX/LX integrated processor allow independent control for both 8-bit and 16-bit transfers by inserting wait states. Each DMA channel has a pair of 16-bit counters and a pair of reload registers for each counter. This allows up to 64-kb block transfers with DMA1 and up to 128-kb block transfers with DMA2. Several modes of operations are possible using programmable features in the registers.

The page registers are used to generate the high order addresses during DMA cycles. Only eight of these registers are used, but all 16 are included to maintain PC-AT compatibility. Each DMA channel has a register associated with it, with the exception of Channel 0 of DMA2. The Am286ZX/LX integrated processor includes weak pull-downs on the DRQ input pins.



14753C–006

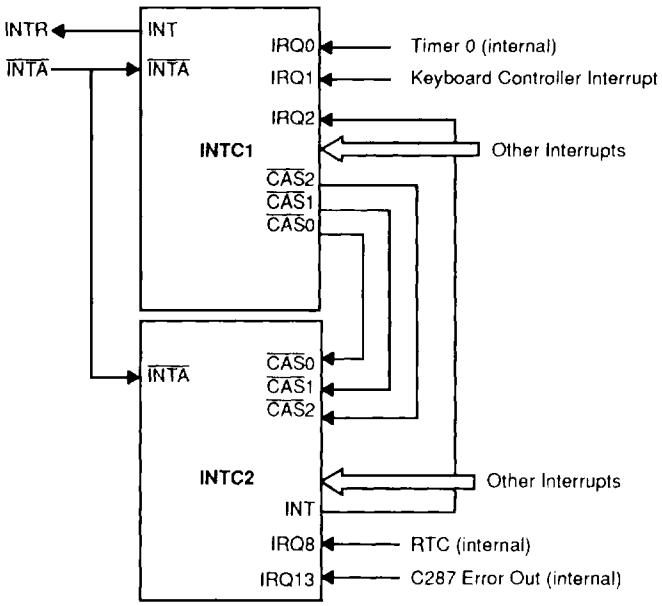
Figure 6. DMA Block Diagram

Interrupt Controllers

Two identical, 8259-compatible interrupt controllers, INTC1 and INTC2, are integrated into the Am286ZX/LX integrated processor. They accept requests from peripherals, resolve priority on pending interrupts and interrupts in service, issue an interrupt request to the processor, and provide interrupt vectors for interrupt service routines.

The two devices are internally connected and must be programmed to operate in cascade mode for operation of all 15 interrupt channels. INTC1 occupies addresses 020H-021H and is configured for master operation in cascade mode. INTC2 occupies addresses 0A0H–0A1H and is configured for slave operation. The interrupt request output signal from INTC2 (INT) is internally connected to the interrupt request input Channel 2 (IRQ2) of INTC1. This configuration is compatible with the IBM PC-AT.

The output of Timer 0 in the counter/timer section is connected to Channel 0 (IRQ0) of INTC1. The interrupt request from the Real Time Clock is connected to Channel 0 (IRQ8) of INTC2. The other interrupts are also available to external peripherals, as in the AT architecture. The Am286ZX/LX integrated processor includes weak pull-ups on the interrupt input pins.



14753C-007

Figure 7. Interrupt Controller Block Diagram

Counter/Timer

A three-channel, general purpose, 82C54-compatible, 16-bit counter/timer is integrated into the Am286ZX/LX integrated processor. It provides critical timing parameters for the PC system under software control. It can be programmed to count in binary or in BCD. Each counter operates independently of the other two and can be programmed for operation as a timer or a counter. All three are controlled from a common set of control logic, which provides controls to load, read, configure, and control each counter. This counter occupies I/O addresses 040H–043H. There are six modes of operation:

Mode 0	Interrupt on terminal count
Mode 1	Hardware re-triggerable one-shot
Mode 2	Rate generator
Mode 3	Square wave generator
Mode 4	Software triggered strobe
Mode 5	Hardware re-triggered strobe

All three counters are driven from a common clock, which is internally generated as a divide by 12 of the F14MHZ pin. The output of Counter 0 is connected to IRQ0 interrupt input of INTC1, and may be used as a software "timer tick" for time-keeping and task-switching activities. The output of Counter 1 is internally connected as a refresh request. The output of Counter 2 is internally connected to speaker logic.

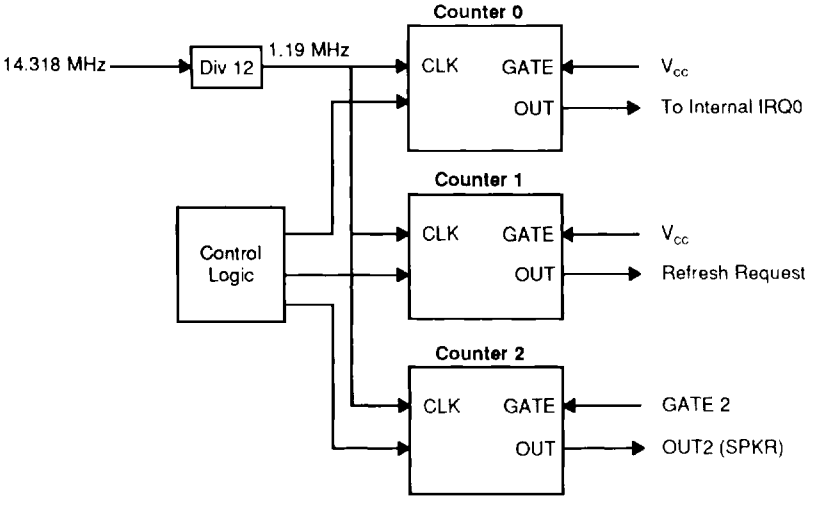
Real Time Clock and CMOS Static RAM

A Real Time Clock (RTC) function is implemented in the Am286ZX/LX integrated processor at I/O address space 070H and 071H. It combines a complete time-of-day clock with alarm, a one hundred year calendar, a programmable periodic interrupt, and 114 bytes of CMOS static RAM. The static RAM is battery backed-up to save its contents in the absence of main system power. Also, since it is battery backed-up, the clock counting continues to maintain the date and time when power is shut off .

The Am286ZX/LX integrated processor includes a low-power CMOS crystal oscillator to handle the 32-kHz clock signal to the RTC. This feature saves board space by integrating the oscillator on-chip, and it extends the life of the system's battery.

An indexed addressing scheme is implemented to write to the 128 locations of the RTC. The index register is written with the address of the memory location, which acts as an address pointer. Data is then transferred to the location. The RTC contains 128 addressable locations which include: 10 locations for time, calendar and alarm data, 4 general purpose registers, and 114 static RAM locations.

The alarm bytes are programmed to generate an interrupt at a specific time, or can be programmed to generate a periodic interrupt. The static RAM from index addresses 0EH to 7FH are not affected by the RTC. This area can be used to store configuration and calibration information. Since this section is battery powered, it will not lose data when the system is turned off.



14753C-008

Figure 8. Counter/Timer Block Diagram

System Control Logic

Enhanced Clock Generator

The Am286ZX/LX integrated processor provides very flexible clock selections for the CPU clock, AT-bus clock, keyboard clock, and AMD 80C287 math coprocessor clock. Configuration registers are provided to select these clocks to suit system applications. An 82284-compatible logic block is used to generate the READY signal for the internal CPU.

PROCLK and IOCLK are the main input clock pins for the clock generator. Depending on the system design, the Am286ZX/LX integrated processor can be configured to select internal CPU clock, AMD 80C287 math coprocessor clock, AT state machine clock, and keyboard clock from either PROCLK or IOCLK. Flexible divisors are provided to select desired operational speeds. SYSCLK is always half the frequency of the AT-state machine clock (ATSMCLK).

The dividers are at the divide by four setting at power up. The default selections for clock source and divider can be modified by writing to configuration registers. The Am286ZX/LX integrated processor contains logic to prevent clock pulse width violations when changing any clock.

In order to achieve maximum system performance, it is desirable to run the processor at the maximum rated speed. Internal state machines maintain asynchronous protocols for high-speed operation of the CPU while allowing slower S-bus cycles.

Enhanced Bus Controller

The Am286ZX/LX integrated processor's Enhanced Bus Controller provides the control logic for routing addresses and data through the Am286ZX/LX integrated processor for every type of data transaction. At its core, it provides analogous functions to the 82284 and 82288. The rest of the logic transforms the Am286ZX/LX integrated processor into advanced high-speed, AT-compatible products. These advanced functions include the following:

1. Dual state machine design—A high-speed CPU synchronous state machine for DRAM and internal register access, and an S-bus state machine which can operate asynchronously to the CPU.
2. AT-compatible, high-byte routing, and word-to-byte transaction conversion for bus transfers to 8-bit peripherals.
3. Address/data routing and buffer control for all possible data transfers, including CPU, DMA, Refresh, and bus mastering.

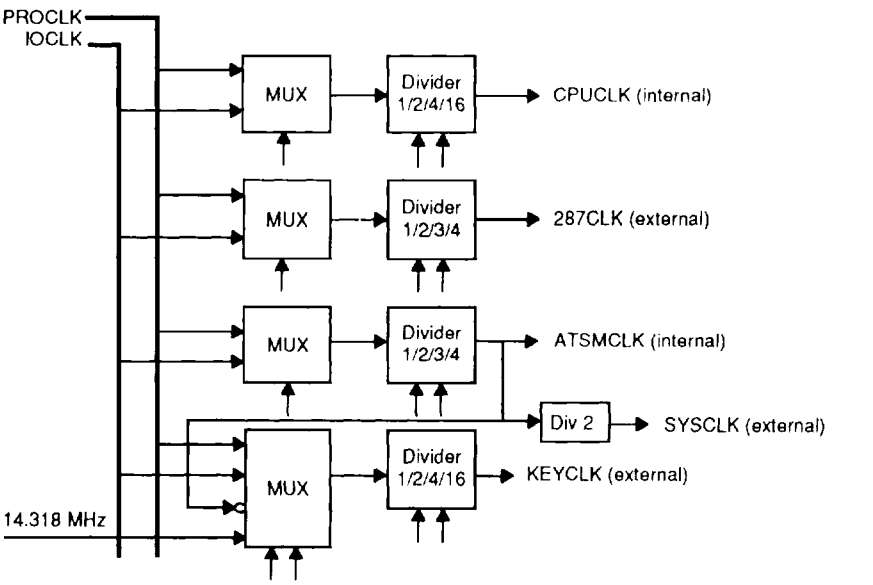


Figure 9. Clock Generator Block Diagram

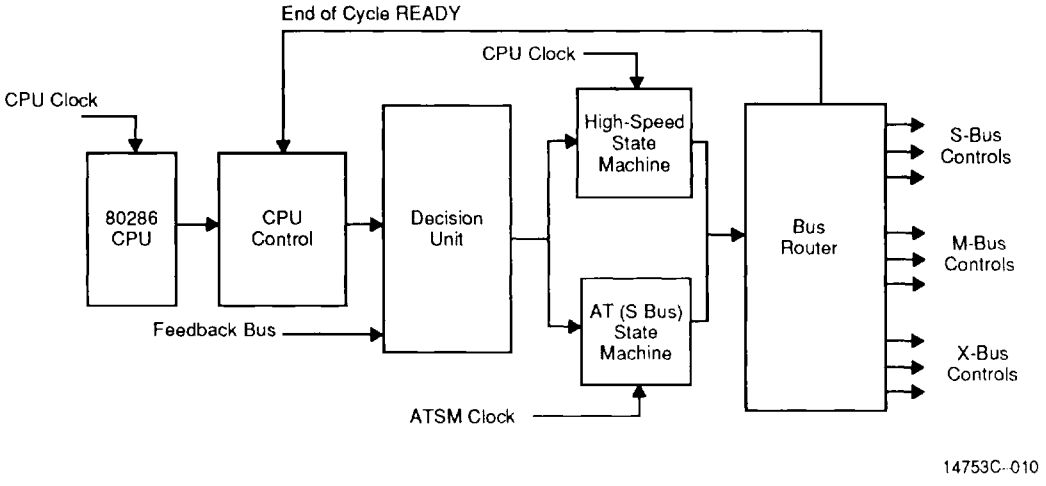


Figure 10. Bus Controller Block Diagram

DRAM Interface

The Am286ZX/LX integrated processor supports a robust and easily implemented memory system providing zero or near zero wait state performance, while maintaining low system cost with inexpensive DRAMs. Its memory array is configured to directly support two banks of 16/18 bits (four 8/9 bit SIMMs). Two additional banks can be added by adding buffers on the memory address lines. Each bank consists of 16-bit data and two optional parity bits, one for each byte. They can be implemented with 256-kbit, 1-Mbit, or 4-Mbit DRAMs for a maximum of 8 Mb per bank, up to a total of 16 Mb in multiple banks.

The array supports page mode accesses to decrease memory speed requirements. If adjacent arrays are populated with the same DRAM size, two or four way interleaving may be selected to increase the page mode hit ratio. The Am286ZX/LX integrated processor can handle memory size mixing. If interleaving is enabled, only the same size banks are interleaved.

In page mode operation, consecutive accesses within DRAM page boundaries are reduced to zero wait states. Wait states occur only when changing pages or crossing page boundaries. In the case of identical banks, interleaving may be enabled to double (2 way) or quadruple (4 way) the page size. This increases the page mode hit ratio. The following table shows the average number of wait states, plus the recommended memory speeds.

CPU Speed	Mode	Average Wait States	DRAM Speed
12 MHz	Normal	0	80 ns
12 MHz	Page/Interleave	0.6	120 ns
12 MHz	Normal	1	100 ns
16 MHz	Normal	1	80 ns
16 MHz	Page/Interleave	0.6	100 ns

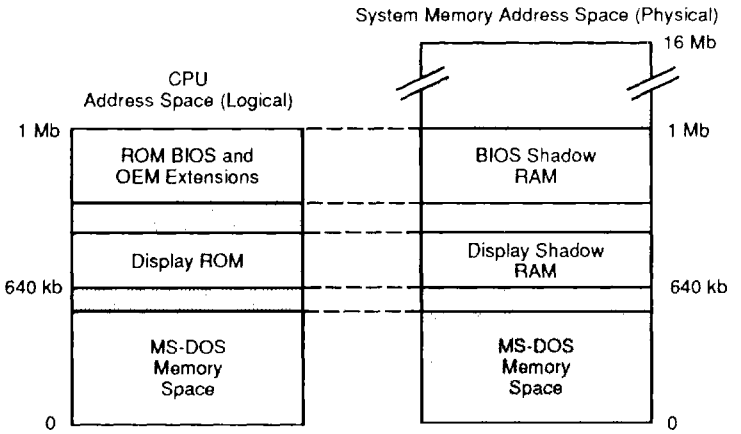
The Am286ZX/LX integrated processor can also interface to SRAM via the S Bus or the high-speed memory bus that normally connects to DRAM.

Shadow RAM/384-kb Relocation

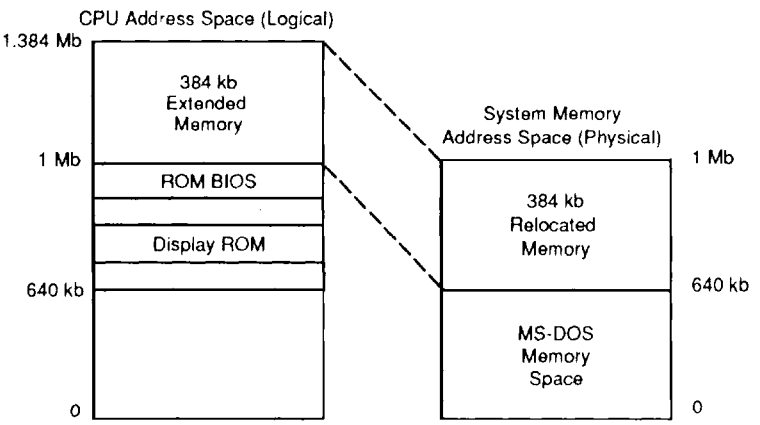
Typically, system ROM BIOS and other ROM extensions require multiple wait states for access, presenting a significant system performance bottleneck. Shadow RAM is a method to eliminate this slow speed path. Using the ROM chip-select control facilities, slow access ROMs can be disabled and replaced with fast access write protected RAM in the 384 kb of unused RAM area. Three 8-bit registers provide Shadow RAM mapping control of 384-kb shadow memory. This area is divided into 24 blocks of 16 kb.

Upon system initialization, the BIOS copies itself and any ROM extensions into a temporary location in system memory. The ROMs are then disabled with the appropriate bits in the ROM control register, while at the same time the shadow RAM is enabled. The ROM contents are then copied into the RAM at original locations, and the appropriate 16-kb pages are write protected. Other sections of RAM can be moved and write protected for other system functions, such as consolidating ROM extensions and write protecting system scratch-pad RAM.

However, if only 1 Mb of RAM is present, the 384 kb between 640 kb and 1 Mb can be relocated to above the 1-Mb boundary, providing 384 kb of extended memory to the user. This feature is enabled by the REL bit in the DRAM Control Register (DRC). The Am286ZX/LX integrated processor provides the flexibility of offering either Shadow RAM or 384-kb relocation by setting the appropriate configuration registers. These two features are mutually exclusive.



a. Shadowing the ROM into RAM



b. 384-kb Relocation

14753C-011

Figure 11. Shadow ROM/384-kb Relocation

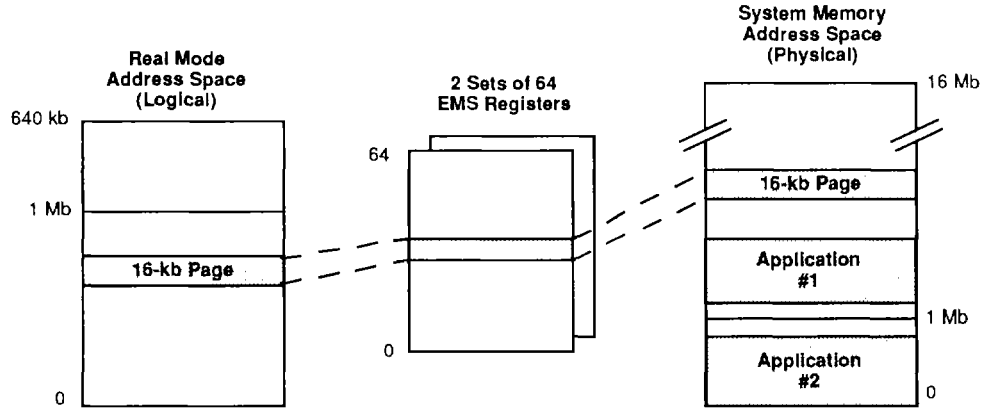
EMS 4.0 Memory Management

The principle behind EMS 4.0 is that any 16-kb page within a large protected memory area can be mapped to a location within the IBM-PC address space (0–1 Mb). This provides a method to implement extremely large data sets and multi-tasking within the memory limitations of MS-DOS. The Am286ZX/LX Address Translation Unit (ATU) provides all the basic hardware functionality to completely map the entire PC address space. The DRAM controller can be programmed to reserve up to 15.5 Mb of local memory for use with EMS. Using the ATU, any 16-kb page in the lower 1 Mb of memory can be mapped to any page in the reserved EMS address space.

The PC logical memory space of 1 Mb is considered as 64 pages, with each page 16 kb (64 x 16 kb = 1 Mb). The EMS memory mapping involves allocating one or more of these pages as a page frame. Accesses to this page frame are translated to addresses in the reserved memory area via a set of pointers in hardware. These pointers are stored in 2 sets of 64 Address Translation Registers (Main and Alternate sets), which are read and written by means of an address translation control register and four address translation register I/O address locations.

MS-DOS application software takes advantage of EMS 4.0 by writing code that conforms to the LIM EMS 4.0 specification.

The Am286ZX/LX integrated processor has two sets of 64 EMS registers. Each set of 64 registers forms a translation set which can map the entire 0–1 Mb address space. By having two sets, EMS software can perform high-speed switching between the two translation sets of EMS memory. When performing this type of multitasking, the addresses (pointers) of EMS memory for each task are loaded into both the primary and alternate EMS registers. This allows for a task switch to occur without reloading the pointers to each task. This greatly improves performance of task switching which is utilized by multitasking EMS software.



14753C-012

Figure 12. EMS Address Translation

Power Saving (Am286LX Processor Only)

Power saving modes are included in the Am286LX processor to allow the system BIOS to control power consumption. Power consumption is controlled by selectively turning off on-chip clocks. The Am286LX processor has two power saving modes—CPU stop clock and system standby. CPU stop clock mode shuts down the CPU clock until the next interrupt. By stopping CPU activity the system draws less current. In this way the system can stop the CPU when CPU interaction is not required. For example, in a keyboard polling loop, the system can stop the CPU between keyboard interrupts.

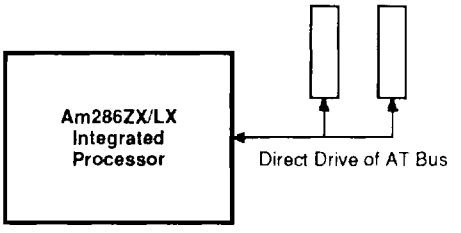
System standby mode goes even further by stopping all clocks that are not essential for DRAM refresh. This mode could be used in conjunction with slow-refresh DRAMs to basically turn the system off, except for maintaining data in the RAMs. The system can be switched into system standby mode during long periods of inactivity to substantially improve battery life. Normal implementation of the Am286LX processor's power saving modes requires no external circuitry. Instead, the modes are enabled by software.

The Am286LX processor also incorporates staggered DRAM refresh. By staggering the refresh of the DRAMs, instantaneous current demands are greatly reduced, providing a lower current surge on the system's power source. The Am286LX processor also has support for slow-refresh DRAMs. With slow-refresh memory, data does not have to be refreshed as often, which reduces power consumption.

External Interfaces

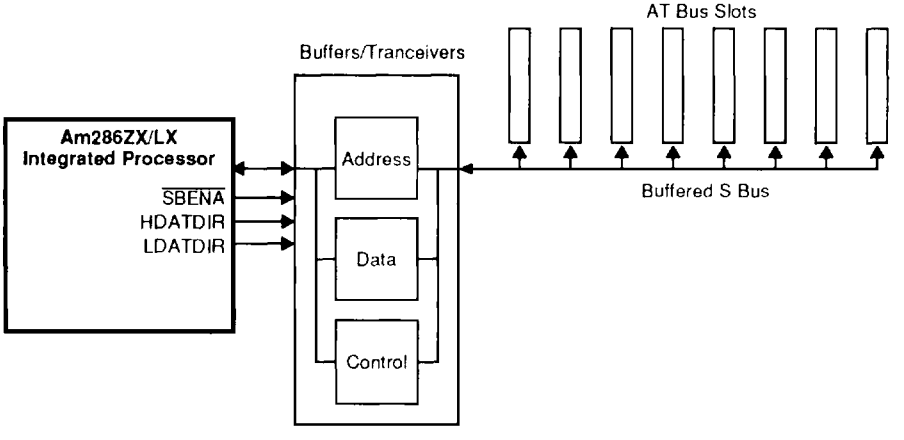
AT System Bus

The Am286ZX/LX integrated processor can directly drive the AT Bus within the limits of the DC current drive specification. For a fully buffered AT Bus, the Am286ZX/LX integrated processor provides three buffer control output pins. They are $\overline{\text{SBENA}}$, HDATDIR, and LDATDIR.



14753C-013

Figure 13. Direct S-Bus Connection



14753C-014

Figure 14. Buffered S-Bus Connection

Keyboard Controller

The Am286ZX/LX integrated processor provides a direct interface for an AT-type keyboard controller (8042), or an XT-type keyboard. The type of keyboard interface is selected with a configuration register. The KEYCLK output is driven by the clock generation logic, with four selectable clock inputs (see Enhanced Clock Generation). The keyboard controller is attached as an X-bus device.

AMD 80C287 Math Coprocessor

The Am286ZX/LX integrated processor provides a direct interface to the AMD 80C287 math coprocessor. The clock generation for the AMD 80C287 math coprocessor is driven by the clock generation logic, with two selectable clock inputs (see Enhanced Clock Generator). The AMD 80C287 math coprocessor is attached with the X-bus address lines and the M-bus data lines. The Am286ZX/LX integrated processor provides AT-standard I/O command decodes for "clear busy" (port 0F0h) and AMD 80C287 math coprocessor reset (port 0F1h). Standard coprocessor interconnect is shown in the following diagram.

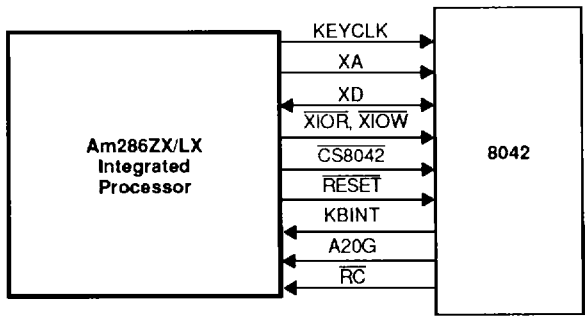
ROM/EPROM

The Am286ZX/LX integrated processor provides support for 8- or 16-bit EPROM configurations. The EPROM(s) are attached as an X-bus device, with high-byte data off the M Bus for 16-bit configurations.

Expansion Bus (X Bus)

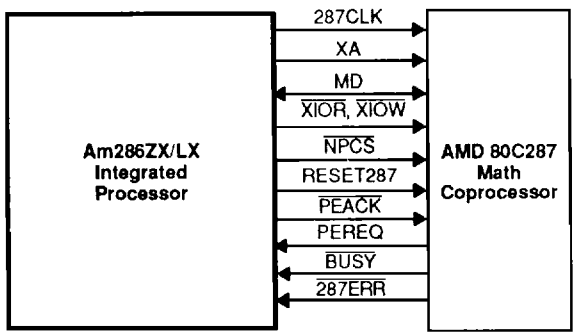
In addition to the EPROM, keyboard controller, and AMD 80C287 math coprocessor peripherals, the Am286ZX/LX integrated processor's X Bus can be used to attach other I/O devices. Eight configuration registers are available to map any 8-byte I/O address range onto the X Bus. 16-bit I/O is also supported.

Any I/O device such as serial ports, parallel ports, and floppy disk controllers may be attached to the Am286ZX/LX integrated processor's X Bus. Any of the four 8-byte DMA channels (0–3) can be mapped to the X Bus as well. For example, a floppy disk controller would use DMA Channel 2.



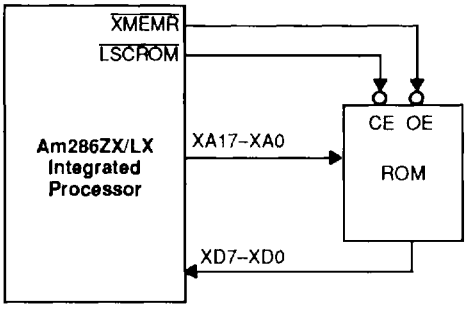
14753C-015

Figure 15. Keyboard Controller Interface



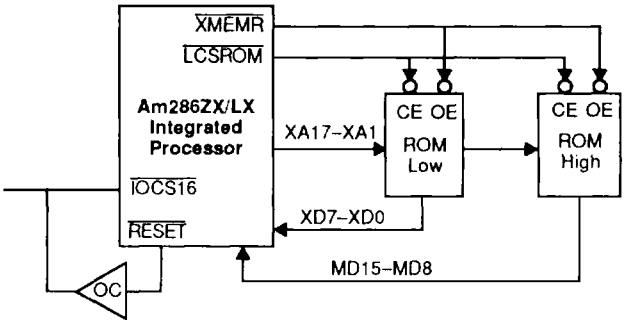
14753C-016

Figure 16. AMD 80C287 Math Coprocessor Interface



Note: This is the default configuration. 14753C–017

Figure 17. 8-Bit EPROM Configuration



Note: Open-collector buffer between RESET and IOCS16. 14753C–018

Figure 18. 16-Bit EPROM Configuration

Additional Features

Fast RESET and Fast GATEA20

The Am286ZX/LX integrated processor provides two features which enhance the system's performance—fast RESET and fast GATEA20. Normally, system software calls for a BIOS routine which issues two commands to switch the processor from protected mode to real mode. First, a RESET command is written to the 8042-keyboard controller; then the GATEA20 command is written to the 8042 controller. This imposes a performance limitation due to the slow 8042. The Am286ZX/LX integrated processor provides the fast RESET and fast GATEA20 features to bypass the keyboard controller and reduce the mode switch time. The Am286ZX/LX integrated processor conforms to the industry standard port 92h location to perform a reset to real mode.

These features greatly improve performance in operating environments like OS/2 and DOS extenders that frequently switch between real and protected mode during execution.

Bus Master Mode

The Am286ZX/LX integrated processor is normally the main CPU of an AT-architecture motherboard. However, the Am286ZX/LX integrated processor's Bus Master Mode allows it to act as a Bus Master peripheral connected to the expansion bus of a host system. This allows the Am286ZX/LX integrated processor to be the main CPU on a high-performance bus-master add-in card. The Am286ZX/LX integrated processor directly supports industry standard architecture (ISA) bus mastering and, with extended logic, MCA and EISA systems. Selecting bus master mode changes the operating mode of some of the S-bus pins to allow direct connection of the Am286ZX/LX integrated processor to the system expansion bus of another system.

NMI and Port B Logic

Industry standard non-maskable interrupt (NMI) logic is provided. This includes the AT-standard port B register at I/O address 061h, and the NMI enable register at I/O address 070h.

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Junction Temperature . . . . . +175°C
Lead Temperature (10 seconds) . . . . . +275°C
Supply Voltage to Ground Potential
Continuous . . . . . −0.5 V to +7.0 V
DC Voltage Applied to Outputs . . . . −0.5 to V_{CC} Max
DC Input Voltage . . . . . −0.5 to V_{CC} Max
DC Output Current . . . . . ±30 mA
DC Input Current . . . . . −10 mA to +10 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Ambient Temperature (T_A) . . . . . 0°C to +70°C
Supply Voltage (V_{CC}) . . . . . +4.75 V to +5.25 V
Battery Voltage (V_{BATT}) . . . . . −3.0 V to −4.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges

V_{CC} = +5 V ±5%, T_A = 0°C to +70°C.

Parameter Symbol	Parameter Descriptions	Notes and Conditions	Min	Max	Unit
V_{IL}	Input Low Voltage		−0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{ILC}	CLK Input Low Voltage (Note 11)		−0.5	0.8	V
V_{IHC}	CLK Input High Voltage (Note 11)		3.6	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = See Note 10	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = See Note 10	3.0	–	V
I_I	Input Leakage Current	V_{IN} = GND or V_{CC}	−10	10	µA
I_{OZ}	Output Leakage Current	V_O = GND or V_{CC}	−10	10	µA
I_{CCSC}	Supply Current (Notes 1, 13)	16 MHz CPU 12.5 MHz CPU		30 28	mA
I_{CCSS}	Supply Current (Notes 2, 13)	16 MHz CPU 12.5 MHz CPU		24 22	mA
I_{CCFS}	Supply Current (Notes 3, 13)	16 MHz CPU 12.5 MHz CPU		5 5	mA
I_{CC}	Supply Current (Note 14)	16 MHz CPU 12.5 MHz CPU		240 190	mA
I_{CCBATT}	RTC Battery Backup Supply Current	V_{BATT} = −3.0 V (Note 12)		20	µA
IL_{LOAD1}	Pull Up Loading Current (Note 4)	V_{IN} = 0.4 V, V_{CC} = 5.25 V	−0.40	−0.10	mA
IL_{LOAD2}	Pull Up Loading Current (Note 5)	V_{IN} = 0.4 V, V_{CC} = 5.25 V	−4.50	−1.50	mA
IL_{LOAD3}	Pull Up Loading Current (Note 6)	V_{IN} = 0.4 V, V_{CC} = 5.25 V	−9.0	−3.0	mA
IL_{LOAD4}	Pull Up Loading Current (Note 7)	V_{IN} = 3.0 V, V_{CC} = 5.25 V	−0.30	−0.05	mA
IL_{LOAD5}	Pull Up Loading Current (Note 8)	V_{IN} = 0.4 V, V_{CC} = 5.25 V	−14.0	−5.0	mA
IH_{LOAD}	Pull Down Loading Current (Note 9)	V_{IN} = 3.0 V, V_{CC} = 5.25 V	0.05	0.40	µA

Notes:
1. Stop Clock Mode (Am286LX processor only): CTSC bit set, input clocks running, CPU clock stopped, peripheral clocks and refresh running.
2. System Standby Mode (Am286LX processor only): SSBY bit set, input clocks running, CPU and Peripheral clocks stopped, refresh running.
3. Full Standby Mode: All input clocks stopped, including 32KHz and F14MHz. This is traditional CMOS standby current.
4. Pull up current for the SA, SD, IRQ, $\overline{MEMR}$, $\overline{MEMW}$, $\overline{IOR}$, $\overline{IOW}$, $\overline{SBHE}$, BUSY, and $\overline{P287ERR}$ pins.
5. Pull up current for the $\overline{MASTER}$, IOCHRDY, $\overline{IOCHK}$ pins.
6. Pull up current for the $\overline{REFRESH}$, $\overline{IOCS16}$, $\overline{MEMCS16}$, and $\overline{POWS}$ pins.
7. Pull up current for the XA pin.
8. Pull up current for the KEYCLK and $\overline{CS8042}$ pins.
9. Pull down current for the DRQ and PEREQ pins.
10. The Am286ZX/LX integrated processors have several output buffer types, each with different I_{OL}/I_{OH} characteristics. They are characterized by the following table.
11. Includes pins PROCLK, IOCLK, KEYCLK (XT keyboard mode), $\overline{CS8042}$ (XT keyboard mode), and PWRGOOD, IOCHK.
12. See Battery Backup Test diagram.
13. V_{IN} = Vcc or GND, Vcc = 5.25 V, outputs loaded with 50 pF.
14. V_{IN} = 0 V or 4 V, Vcc = 5.25 V, outputs loaded with 50 pF.

Pin Group	I_{OL}, I_{OH}	C_L
SA, SD, $\overline{MEMR}$, $\overline{MEMW}$, $\overline{IOR}$, $\overline{IOW}$, RESETDRV	6 mA	100 pF
LA, $\overline{SMEMR}$, $\overline{SMEMW}$, SYSCLK, $\overline{MASTER}$, $\overline{REFRESH}$, $\overline{SBHE}$, DMATC, BALE, AEN, $\overline{SBENA}$, XD, XA, $\overline{XIOR}$, $\overline{XIOW}$, $\overline{RESET}$, $\overline{DACK}$	4 mA	100 pF
$\overline{XMEMR}$, $\overline{XMEMW}$, LCSROM	4 mA	50 pF
SPKR	4 mA	150 pF
MA	2 mA	260 pF
MD, MDP	2 mA	100 pF
$\overline{MWENH}$, $\overline{MWENL}$	2 mA	260 pF
$\overline{RAS}$, $\overline{CAS}$	2 mA	200 pF
DLYOUT, P287CLK, $\overline{NPCS}$, RESET287, $\overline{PEACK}$, HDATDIR, LDATDIR	2 mA	50 pF

CAPACITANCE

T_A = +25°C; all measurements referenced to device GND.

Parameter Symbol	Parameter Descriptions	Typ	Unit
C_{IN}	Input Pin Capacitance	10	pf
C_{IO}	Bi-directional Pin Capacitance	10	pf
C_{OUT}	Output Pin Capacitance	10	pf

Note: Pin capacitance is characterized at a frequency of 1 MHz, and is tested on a sample basis only.

SWITCHING CHARACTERISTICS over operating range

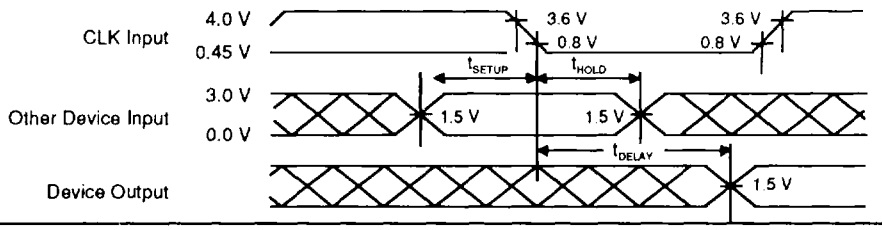
Method of Specification

The Am286ZX/LX integrated processor has several modes of operation. Given the number of options available and the internal generation of clocks, some explanation of the specification method is in order. The following points must be noted:

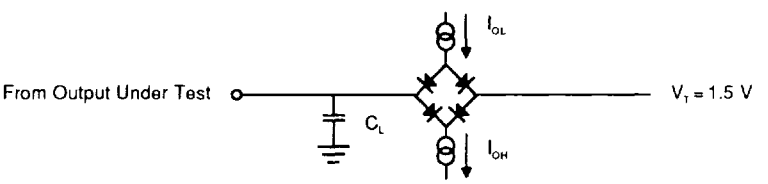
1. In order to test and verify the timing parameters, the specifications are from external input to output definitions.
2. The designator "srcCLK" refers to the input clocks PROCLK or IOCLK. Internal and external clocks are generated from these input clock signals. KEYCLK may use the 14.318 MHz input clock as its source. It is assumed for all diagrams that all PROCLK and IOCLK related dividers are set for divide by 1.
3. Output invalid delay times (Min and Max) not specified track the corresponding valid delay time (Min and Max) within ±5 ns. There are two exception on the M bus for non-paged mode accesses. The $\overline{RAS}$ invalid delay timing tracks the valid delay timing by +10 ns. The MA10–MA0 invalid timing tracks the valid delay timing by ±8 ns.
4. The AT-bus timing diagrams assume a programmed configuration of no command delays for 16-bit memory accesses, one command delay for 8-bit memory accesses, and one command delay for I/O commands. The timing parameters are referenced to clocks and are independent of command delays.

Note: Switching characteristics are targeted numbers and are subject to change without notice.

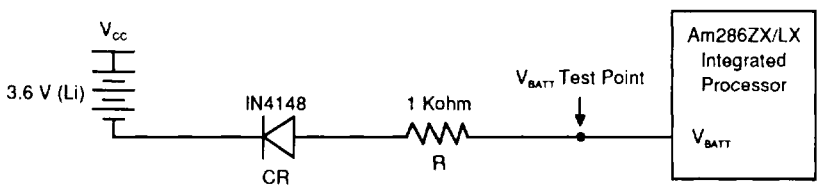
SWITCHING TEST WAVEFORM



SWITCHING TEST CIRCUIT



BATTERY BACKUP TEST DIAGRAM



Input Clocks

Parameter Symbol	Parameter Descriptions	Notes and Conditions	Min	Max	Unit
t1	PROCLK, IOCLK Period	16 MHz CPU 12.5 MHz CPU	31 40		ns
t2	PROCLK, IOCLK Low Time	16 MHz CPU 12.5 MHz CPU	14 16		ns
t3	PROCLK, IOCLK High Time	16 MHz CPU 12.5 MHz CPU	13 16		ns
t4	RTCCLK Period (Note 1)		30.518		µs
t5	F14 MHz Period		69.8		ns
t6	F14 MHz High, Low Time		25		ns

Note 1. 32.768 kHz ±100 ppm crystal input across RTCLKX1 and RTCLKX2 for AT compatibility.

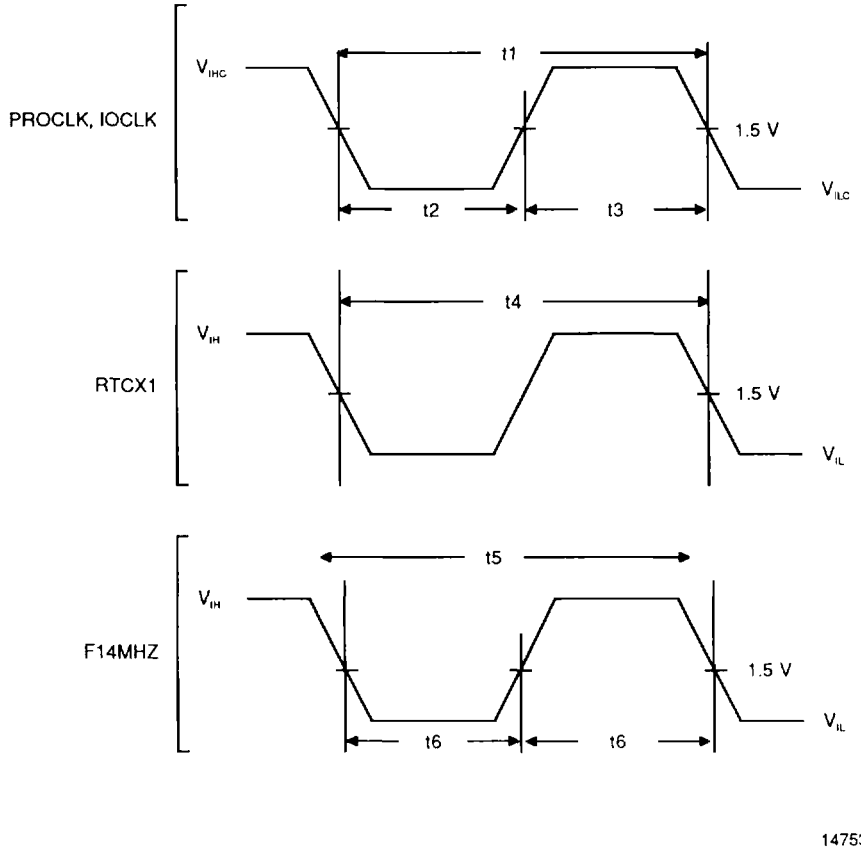
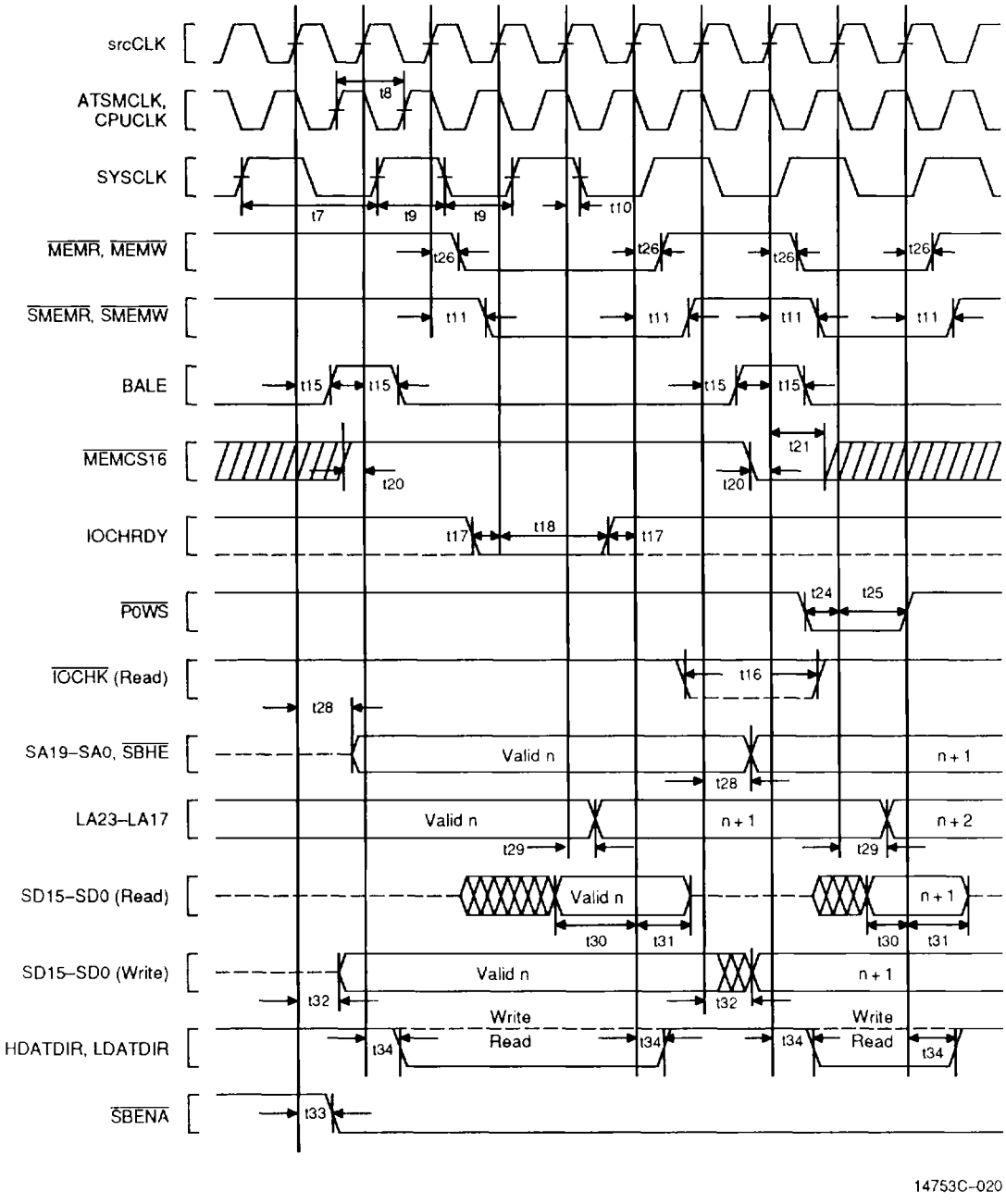


Figure 19. Input Clocks

AT System Bus Interface: Referenced to srcCLK

Parameter Symbol	Parameter Descriptions	Notes and Conditions	Min	Max	Unit
t7	SYSCLK Period	Note 2	125		ns
t8	ATSMCLK Period		62.5		ns
t9	SYSCLK High/Low Time		50		ns
t10	SYSCLK Delay from srcCLK	Note 1	9	31	ns
t11	$\overline{\text{SMEMR}}$/$\overline{\text{SMEMW}}$ from srcCLK	Note 1		70	ns
t12	$\overline{\text{IOR}}$/$\overline{\text{IOW}}$ from srcCLK	Note 1		50	ns
t13	$\overline{\text{REFRESH}}$ Active from srcCLK	Note 1		90	ns
t14	$\overline{\text{REFRESH}}$ Inactive from srcCLK	Note 1		90	ns
t15	BALE from srcCLK	Note 1		45	ns
t16	$\overline{\text{IOCHK}}$ Active Pulse Width	Note 3	10		ns
t17	IOCHRDY Setup to srcCLK	Notes 1, 3	5		ns
t18	IOCHRDY Hold from srcCLK	Notes 1, 3	17		ns
t19	RESETDRV from srcCLK	Note 4		65	ns
t20	$\overline{\text{MEMCS16}}$ Setup to srcCLK	Note 1	5		ns
t21	$\overline{\text{MEMCS16}}$ Hold to srcCLK	Note 1	30		ns
t22	$\overline{\text{IOCS16}}$ Setup to srcCLK	Note 1	10		ns
t23	$\overline{\text{IOCS16}}$ Hold to srcCLK	Note 1	25		ns
t24	$\overline{\text{PoWS}}$ Setup to srcCLK	Note 1	11		ns
t25	$\overline{\text{PoWS}}$ Hold to srcCLK	Note 1	15		ns
t26	$\overline{\text{MEMR}}$/$\overline{\text{MEMW}}$ from srcCLK	Note 1		47	ns
t27	IRQ Inactive Pulse Width	Notes 3, 5, 6	100		ns
t28	SA, $\overline{\text{SBHE}}$ Valid from srcCLK	Note 1		60	ns
t29	LA Valid from srcCLK	Note 1		52	ns
t30	SD Read Setup to srcCLK	Note 1	13		ns
t31	SD Read Hold to srcCLK	Note 1	35		ns
t32	SD Write Valid from srcCLK	Note 1		60	ns
t33	$\overline{\text{SBENA}}$ from srcCLK	Note 1		52	ns
t34	(H,L)DATDIR from srcCLK	Note 1		54	ns

Notes: 1. ATSMCLK reference.
2. The maximum frequency for SYSCLK is 8 MHz.
3. Asynchronous inputs not requiring setup or hold times. This specification given for testing purposes.
4. Duration of RESETDRV active is dependent on PWRGOOD and can be software controlled
5. Low time required to clear the input latch of the interrupt controller.
6. IRQs must remain High until after the first interrupt acknowledge cycle to prevent spurious interrupts.



14753C-020

Figure 20. AT System Bus Interface (Processor) Memory 8-Bit-1WS, 16-Bit-0WS

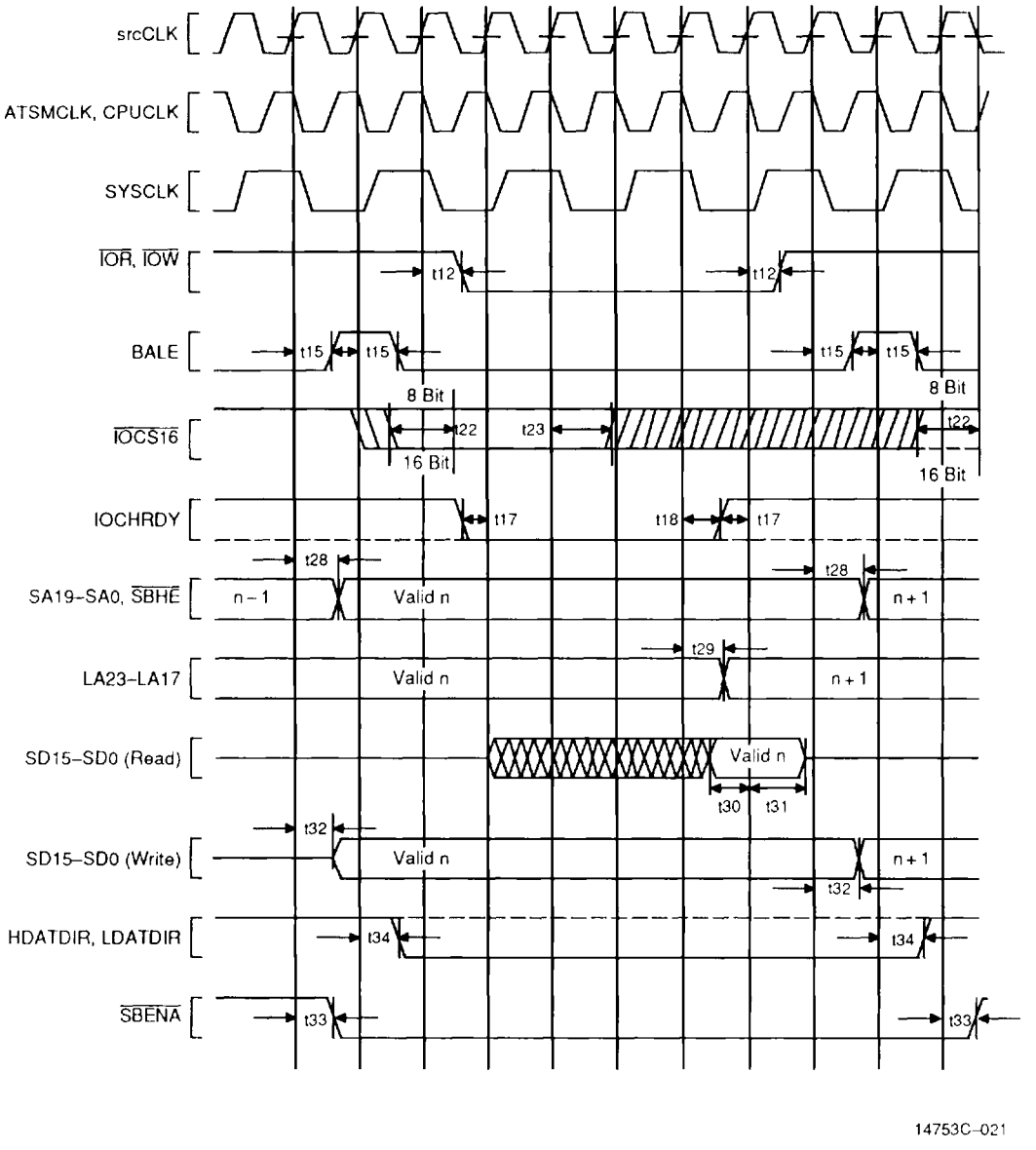


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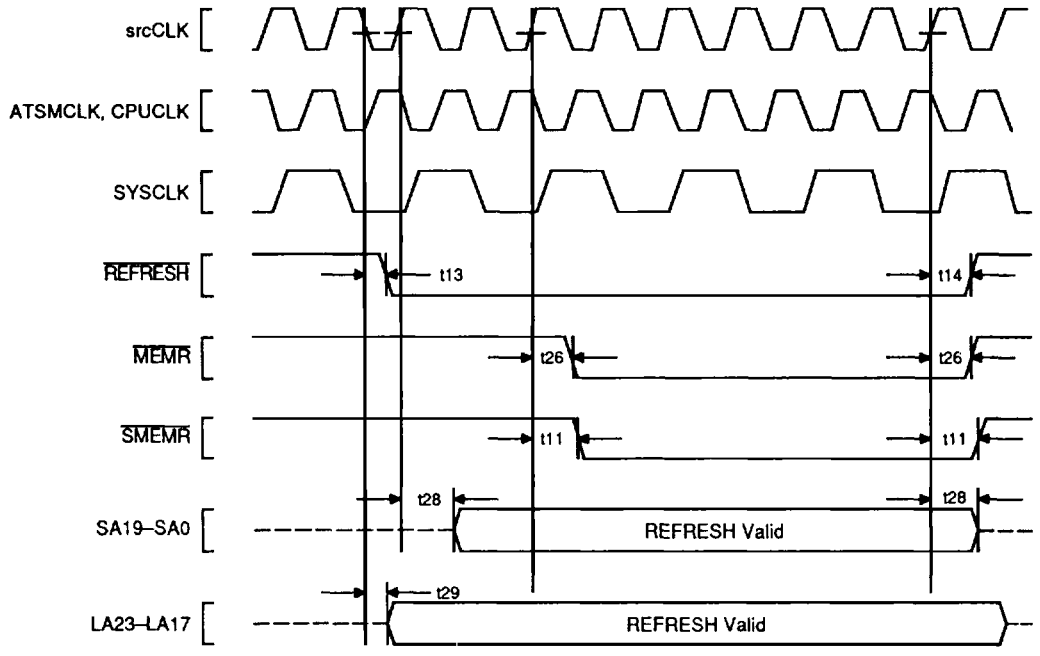
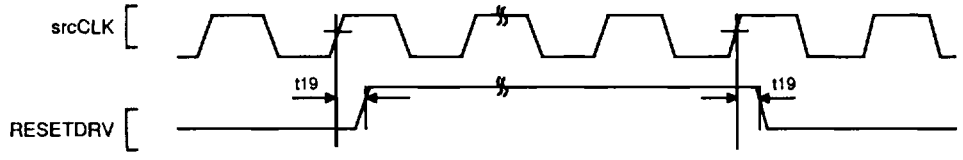
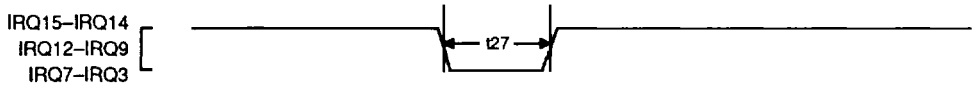
Figure 21. AT System Bus Interface (Processor) I/O 16- and 8-Bit-2WS



a. REFRESH



b. RESETDRV



c. IRQ

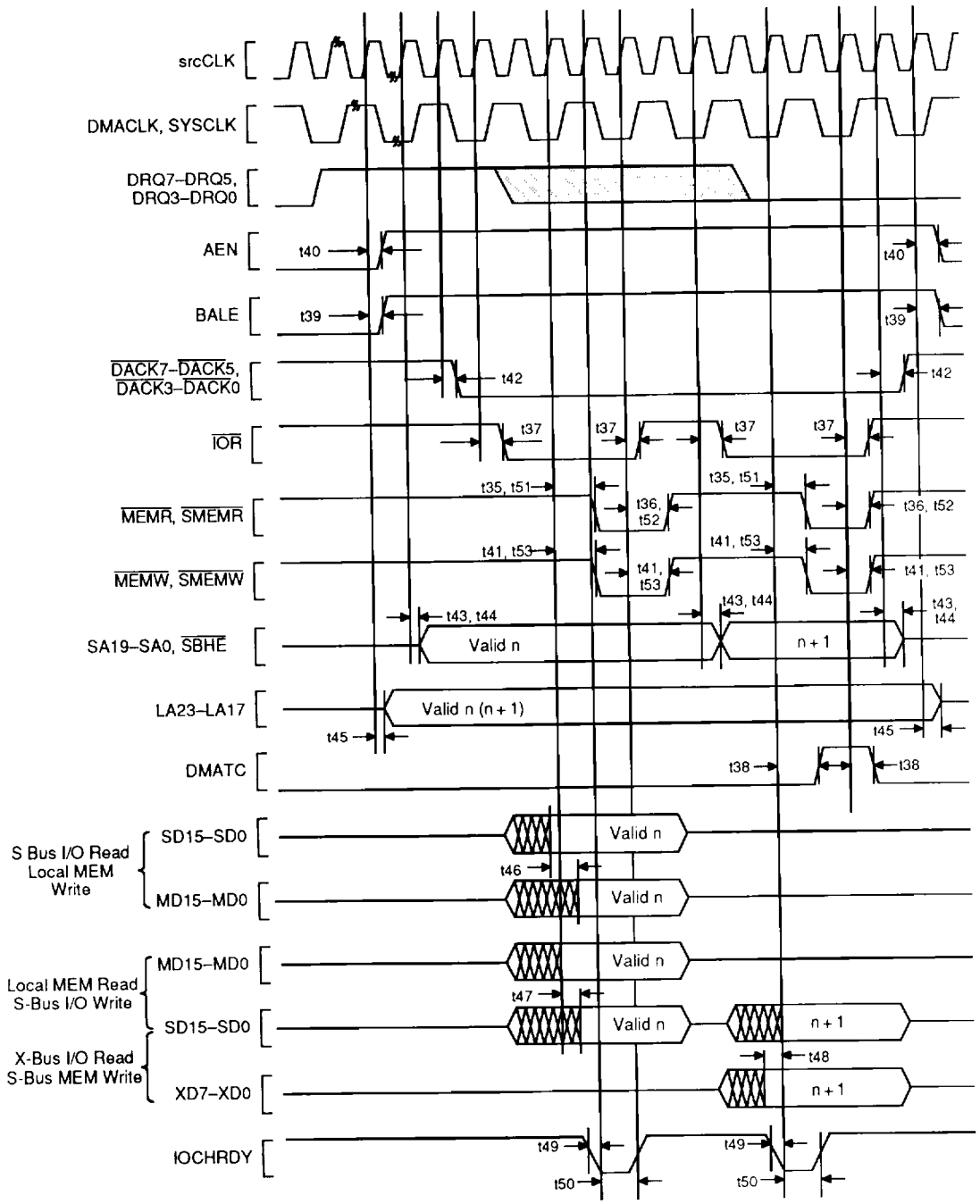
14753C–022

Figure 22. AT System Bus Interface (Processor)

AT System Bus Interface (DMA): Referenced to srcCLK

Parameter Symbol	Parameter Descriptions	Notes and Conditons	Min	Max	Unit
t35	$\overline{\text{MEMR}}$ Active from srcCLK	Note 2		50	ns
t36	$\overline{\text{MEMR}}$ Inactive from srcCLK	Note 2		75	ns
t37	$\overline{\text{IOR}}$ from srcCLK	Note 2		60	ns
t38	DMATC from srcCLK	Note 2		75	ns
t39	BALE from srcCLK	Note 1		55	ns
t40	AEN from srcCLK	Note 1		60	ns
t41	$\overline{\text{MEMW}}$, $\overline{\text{IOW}}$ from srcCLK	Note 2		60	ns
t42	$\overline{\text{DACK}}$ from srcCLK	Note 2		65	ns
t43	SA Valid from srcCLK	Note 2		120	ns
t44	$\overline{\text{SBHE}}$ from srcCLK	Note 2		80	ns
t45	LA Valid from srcCLK	Note 2		105	ns
t46	MD Valid from SD Valid ($\overline{\text{IOR}}$)			25	ns
t47	SD Valid from MD Valid ($\overline{\text{MEMR}}$)			27	ns
t48	SD Valid from XD Valid ($\overline{\text{IOR}}$)			27	ns
t49	IOCHRDY Setup to srcCLK	Notes 2, 3	5		
t50	IOCHRDY Hold from srcCLK	Notes 2, 3	25		
t51	$\overline{\text{SMEMR}}$ Active from srcCLK	Note 2		50	
t52	$\overline{\text{SMEMR}}$ Inactive from srcCLK	Note 2		80	
t53	$\overline{\text{SMEMW}}$ from srcCLK	Note 2		65	

Notes 1. CPUCLK reference.
2. DMACLK reference.
3. Asynchronous inputs not requiring setup or hold times. This specification given for testing purposes.



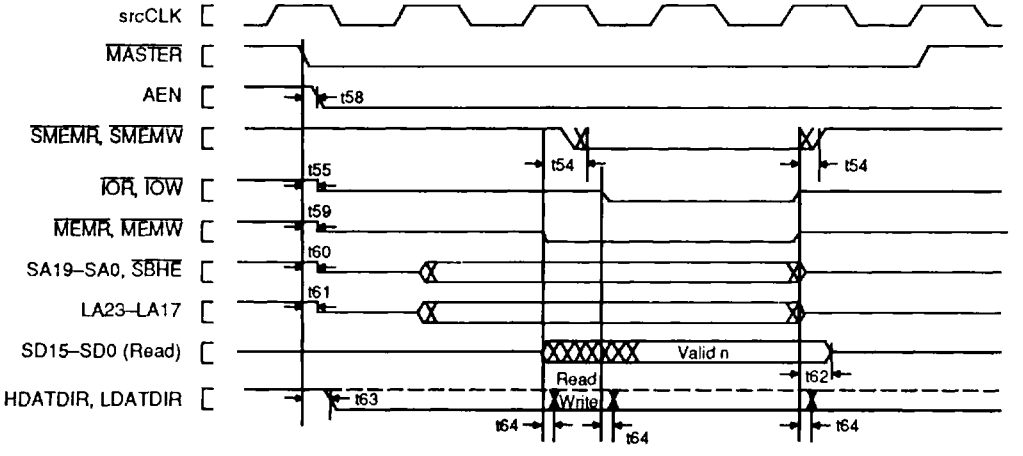
14753C-023

Figure 23. AT System Bus Interface (DMA) Local I/O Write/Memory Read, X Bus I/O Read/Memory Write

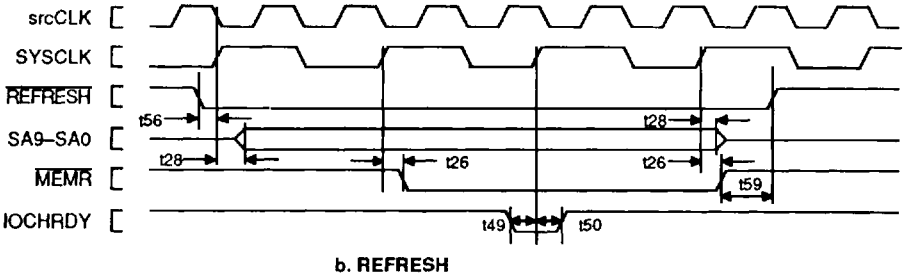
AT System Bus Interface (External Master): Referenced to srcCLK

Parameter Symbol	Parameter Descriptions	Notes and Conditions	Min	Max	Unit
t54	$\overline{\text{SMEMR}}$/$\overline{\text{SMEMW}}$ from $\overline{\text{MEMR}}$/$\overline{\text{MEMW}}$			50	ns
t55	$\overline{\text{IOR}}$/$\overline{\text{IOW}}$ Float from $\overline{\text{MASTER}}$ Active	Note 3		40	ns
t56	$\overline{\text{REFRESH}}$ Setup to srcCLK	Note 1, 2	5		ns
t57	$\overline{\text{REFRESH}}$ Hold from srcCLK	Note 1, 2	20		ns
t58	AEN from $\overline{\text{MASTER}}$			40	ns
t59	$\overline{\text{MEMR}}$/$\overline{\text{MEMW}}$ Float from $\overline{\text{MASTER}}$ Active	Note 3		40	ns
t60	SA, $\overline{\text{SBHE}}$ Float from $\overline{\text{MASTER}}$ Active	Note 3		55	ns
t61	LA Float from $\overline{\text{MASTER}}$ Active	Note 3		30	ns
t62	SD Hold from $\overline{\text{MEMR}}$		12		ns
t63	(H,L)DATDIR from $\overline{\text{MASTER}}$ Active			44	ns
t64	(H,L)DATDIR from $\overline{\text{IOR}}$/$\overline{\text{MEMR}}$ Active			44	ns
t65	SA Setup to Command		40		ns
t66	SA Hold from Command		10		ns

Notes: 1. ATSMCLK reference.
2. Asynchronous inputs not requiring setup or hold times. This specification given for testing purposes.
3. Not 100% tested.



a. Master Read/Write



b. REFRESH

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Figure 24. AT System Bus Interface (External Bus Master)

Coprocessor Interface

Parameter Symbol	Parameter Descriptions	Notes and Conditions	Min	Max	Unit
t68	P287CLK Period	Note 2	30		ns
t69	P287CLK Low Time		12		ns
t70	P287CLK Delay from srcCLK			20	ns
t71	$\overline{NPCS}$ from srcCLK	Notes 1, 3		47	ns
t72	$\overline{BUSY}$ Setup to srcCLK	Notes 1, 3	5		ns
t73	$\overline{BUSY}$ Hold from srcCLK	Notes 1, 3	5		ns
t74	PEREQ Setup to srcCLK	Notes 1, 3	5		ns
t75	PEREQ Hold from srcCLK	Notes 1, 3	20		ns
t76	$\overline{PEACK}$ Active from srcCLK	Note 1		35	ns
t77	$\overline{PEACK}$ Inactive from srcCLK	Note 1		247	ns
t78	RESET287 from srcCLK	Note 1		40	ns
t79	$\overline{BUSY}$ to $\overline{P287ERR}$ Active Overlap		5		ns

Notes: 1. CPUCLK reference.
2. This 50% duty cycle is internally divided by 3 within the AMD 80C287 math coprocessor.
3. Asynchronous inputs not requiring setup or hold times. This specification given for testing purposes.

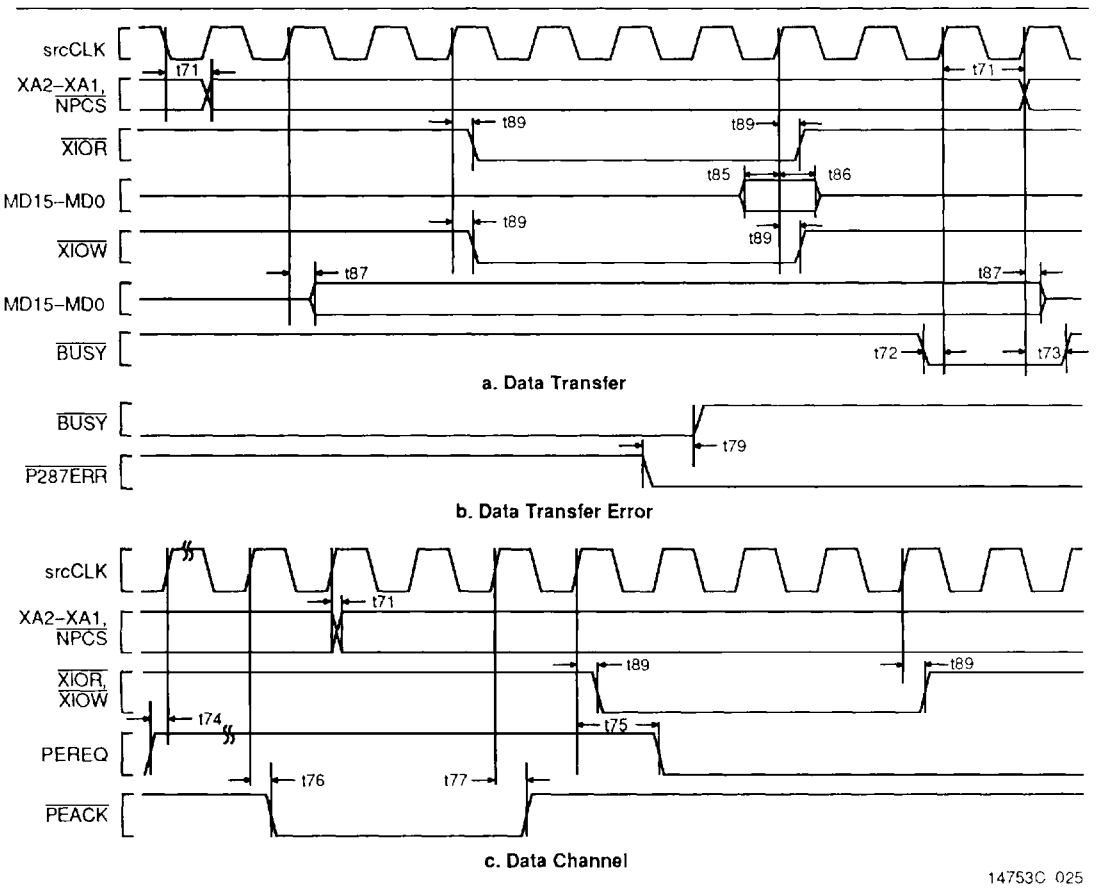
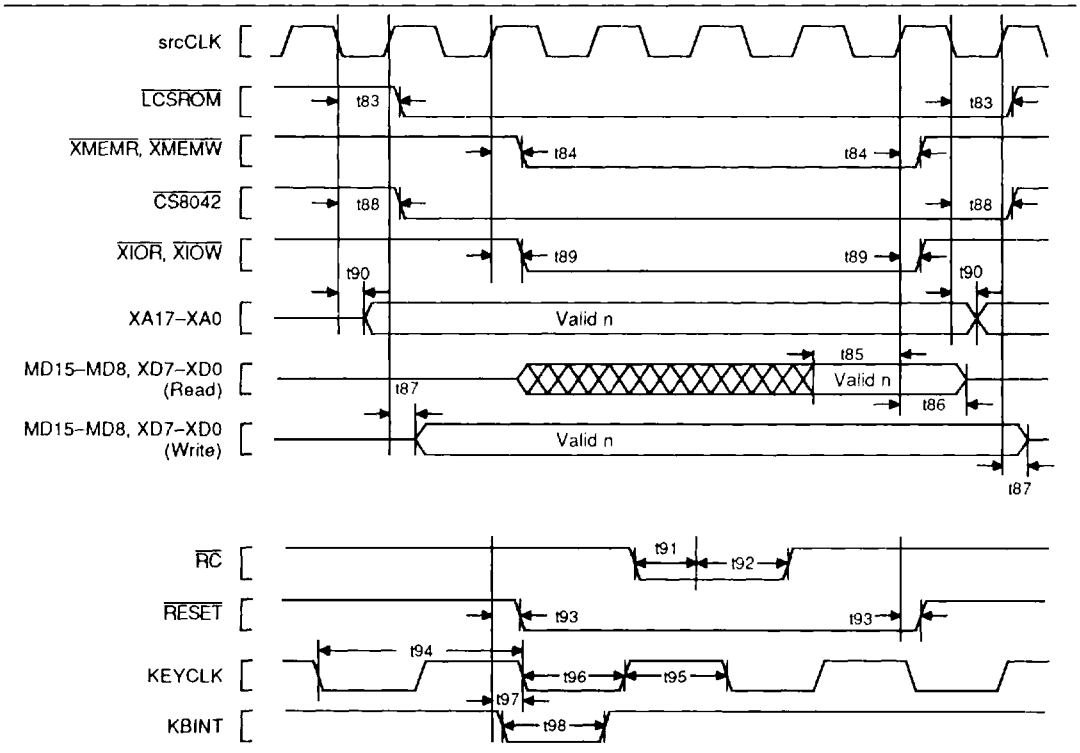


Figure 25. Coprocessor Interface

XBUS—ROM, RAM, KBD, I/O, MEM

Parameter Symbol	Parameter Descriptions	Notes and Conditions	Min	Max	Unit
t83	$\overline{LCSROM}$ from srcCLK	Note 1		60	ns
t84	$\overline{XMEMR}$/$\overline{XMEMW}$ from srcCLK Non-DMA cycles	Note 1		45	ns
t85	MD, XD Read Setup to srcCLK	Note 1	15		ns
t86	MD, XD Read Hold from srcCLK	Note 1	30		ns
t87	MD, XD Write from srcCLK	Note 1		60	ns
t88	$\overline{CS8042}$ from srcCLK	Note 1		47	ns
t89	$\overline{XIOR}$/$\overline{XIOW}$ from srcCLK	Note 1		60	ns
t90	XA from srcCLK	Note 1		40	ns
t91	$\overline{RC}$ Setup to srcCLK	Notes 1, 2	5		ns
t92	$\overline{RC}$ Hold to srcCLK	Notes 1, 2	5		ns
t93	$\overline{RESET}$ from srcCLK	Note 1		25	ns
t94	KEYCLK Period		32		ns
t95	KEYCLK High Time		12		ns
t96	KEYCLK Low Time		8		ns
t97	KEYCLK Delay from srcCLK	Note 1		31	ns
t98	KBINT Inactive Pulse Width	Notes 2, 3, 4		100	ns

Notes: 1. CPUCLK reference.
2. Asynchronous inputs not requiring setup or hold times. This specification given for testing purposes.
3. This Low time is required to clear the input latch in edge triggered mode.
4. In all modes KBINT must remain High until the first Interrupt Acknowledge.



14753C-026

Figure 26. X Bus—ROM, RAM, Keyboard, I/O Device (Processor) Read, Write, 1WS

XBUS—I/O (DMA/External Master)

Parameter Symbol	Parameter Descriptions	Notes and Conditions	Min	Max	Unit
t99	XD Valid from SD Valid			30	ns
t100	XD Valid from MD Valid			30	ns
t101	MD Valid from XD Valid			30	ns
t102	$\overline{XIOR}$/$\overline{XIOW}$ Valid from srcCLK	Note 1		60	ns
t103	$\overline{XMEMR}$/$\overline{XMEMW}$ Valid from $\overline{MEMR}$/$\overline{MEMW}$ Valid			40	ns
t104	$\overline{XIOR}$/$\overline{XIOW}$ Valid from $\overline{IOR}$/$\overline{IOW}$ Valid			30	ns
t105	XA Valid from SA Valid			20	ns

Notes: 1. DMACLK reference.

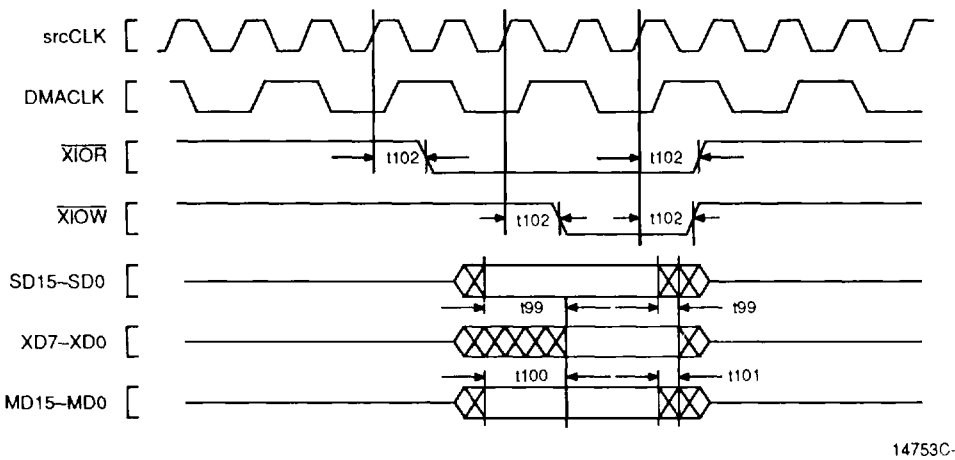


Figure 27. X Bus—I/O Device (DMA)

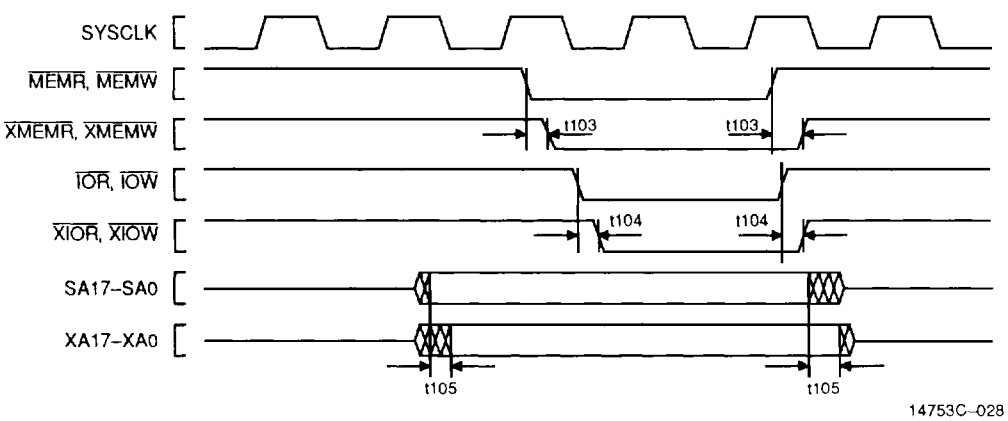


Figure 28. X Bus—RAM, Keyboard, I/O Device (External Bus Master)

Miscellaneous Signals

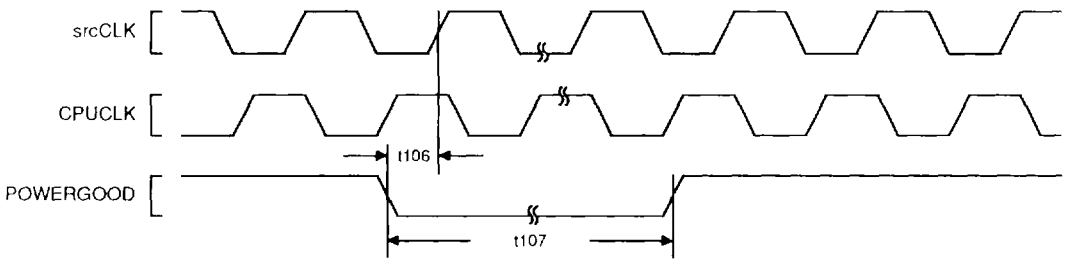
Parameter Symbol	Parameter Descriptions	Notes and Conditions	Min	Max	Unit
t106	PWRGOOD Setup to srcCLK	Notes 1, 2	15		ns
t107	PWRGOOD Pulse Width	Notes 1, 2, 3	65 · TPCLK		ns

Notes 1. CPUCLK reference.
2. Asynchronous inputs not requiring setup or hold times. This specification given for testing purposes.
3. TPCLK is the period of PROCLK.

Am286ZX/LX Integrated Processor as a Bus Master

New Parameter Symbol	Parameter Descriptions	Notes and Conditions	Min	Max	Unit
t108	$\overline{\text{MASTER}}$ Active from $\overline{\text{DACK}}$ Active			25	ns
t109	$\overline{\text{MASTER}}$ Inactive from srcCLK			40	ns
t111	$\overline{\text{IOR}}$/$\overline{\text{IOW}}$ from srcCLK	Note 1		50	ns
t113	$\overline{\text{MEMR}}$/$\overline{\text{MEMW}}$ from srcCLK	Note 1		50	ns
t115	SA, $\overline{\text{SBHE}}$ from srcCLK	Note 1		60	ns
t117	LA Valid from srcCLK	Note 1		45	ns
t119	SD Write from srcCLK	Note 1		63	ns
t120	SD Write Setup to $\overline{\text{MEMW}}$ Active		12		ns

Notes: 1. ATSMCLK reference.



14753C-029

Figure 29. Miscellaneous Signals

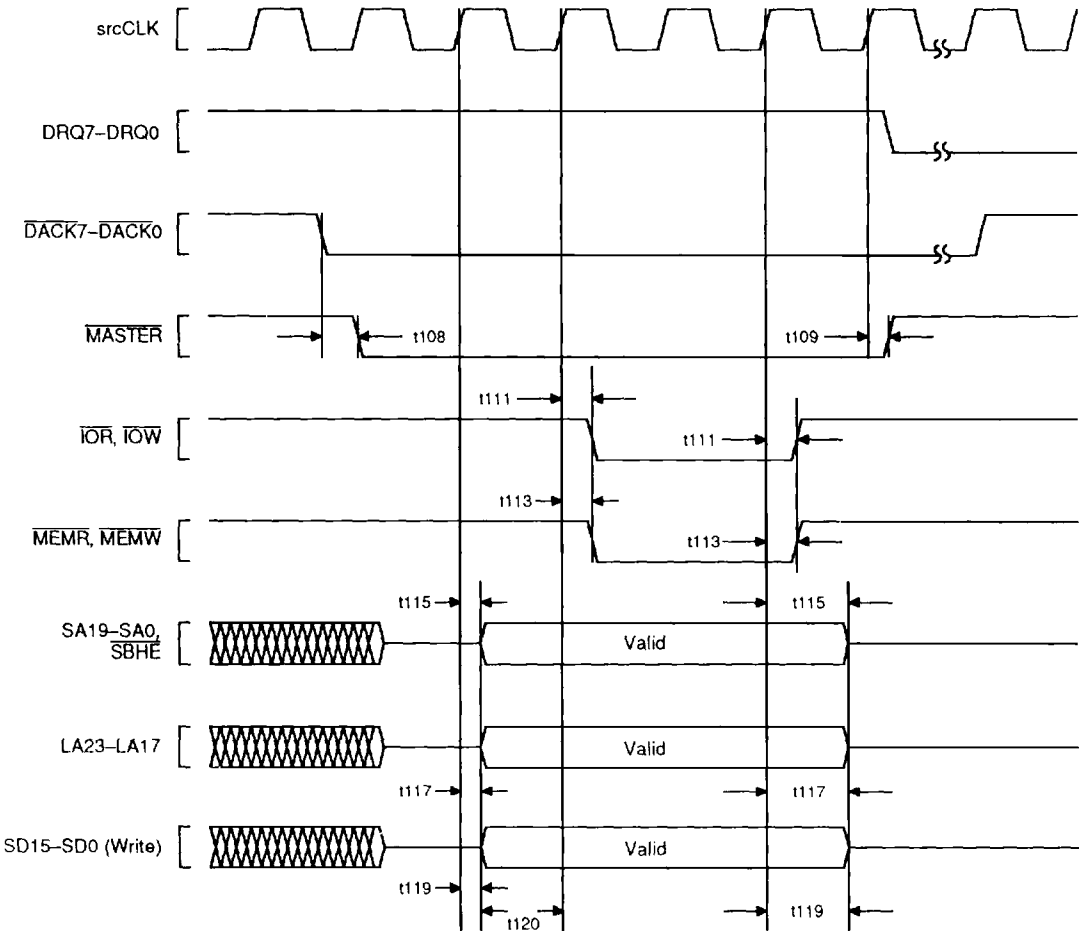


Figure 30. Am286ZX/LX Integrated Processor as a Bus Master

Memory Bus

Parameter Symbol	Parameter Descriptions	Notes and Conditions	Min	Max	Unit
t121	srcCLK to $\overline{RAS}$ Active			36	ns
t122	srcCLK to $\overline{RAS}$ Inactive			43	ns
t123	srcCLK to $\overline{CAS}$ Active			35	ns
t124	srcCLK to $\overline{CAS}$ Inactive			35	ns
t125	srcCLK to MA Valid			50	ns
t126	srcCLK to MA Invalid		9		ns
t127	$\overline{MWENL}$, $\overline{MWENH}$ Active Delay			40	ns
t128	$\overline{MWENL}$, $\overline{MWENH}$ Inactive Delay			40	ns
t129	srcCLK to MD Valid			47	ns
t130	srcCLK to MD FLOAT	Note 1		40	ns
t131	MD Read Setup to srcCLK		6		ns
t132	MD Hold from srcCLK		20		ns
t133	srcCLK to MDP Valid			47	ns
t134	MDP Setup to srcCLK		6		ns
t135	MDP Hold from srcCLK		20		ns
t136	srcCLK to MDP FLOAT	Note 1		40	ns
t137	SA to MA Valid Delay			73	ns
t139	SBUS cmd to DLYOUT Delay		5	35	ns
t140	DL0 to MA Valid Delay			25	ns
t141	SBUS cmd to $\overline{RAS}$ Delay			50	ns
t142	SBUS cmd to $\overline{MWENL}$, $\overline{MWENH}$ Delay			49	ns
t143	DL1 to $\overline{CAS}$ Delay		4	22	ns

Notes: 1 Not 100% tested

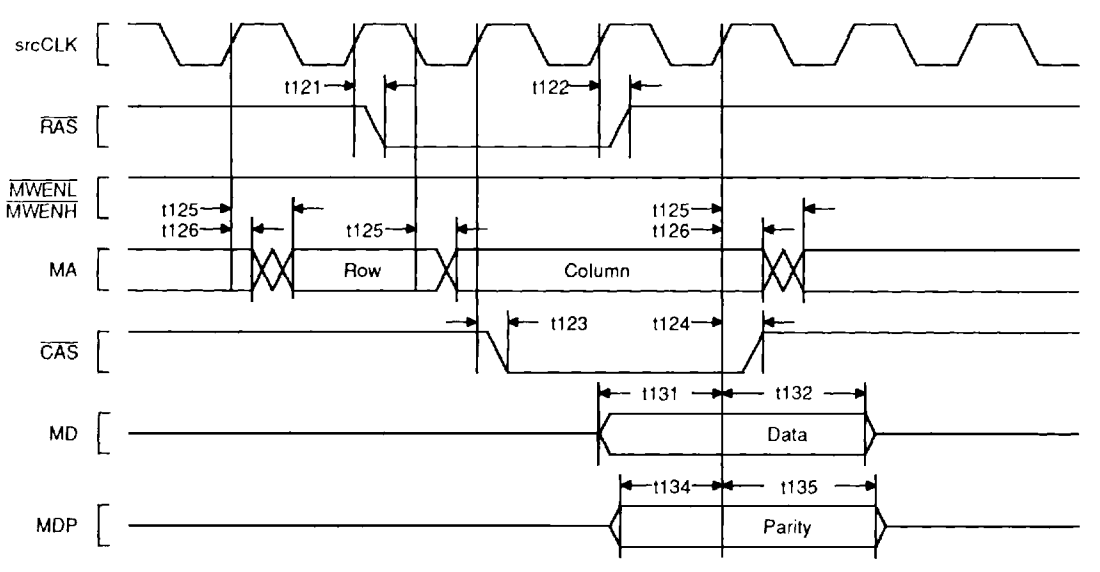


Figure 31. M Bus: Non-Paged Mode—Read/0WS

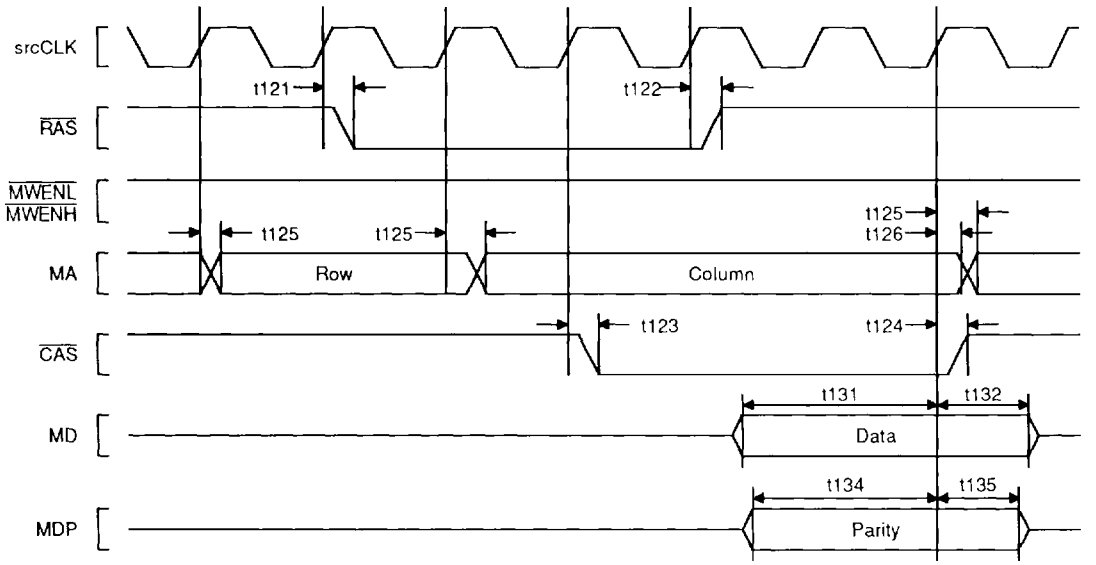


Figure 32. M Bus: Non-Paged Mode—Read/1WS

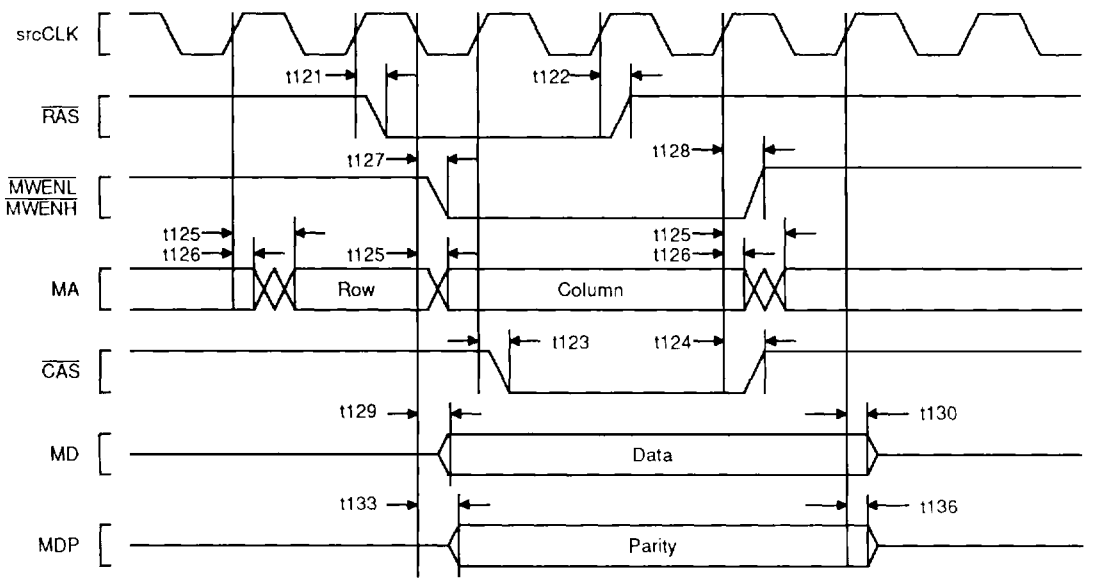


Figure 33. M Bus: Non-Paged Mode—Write/0WS

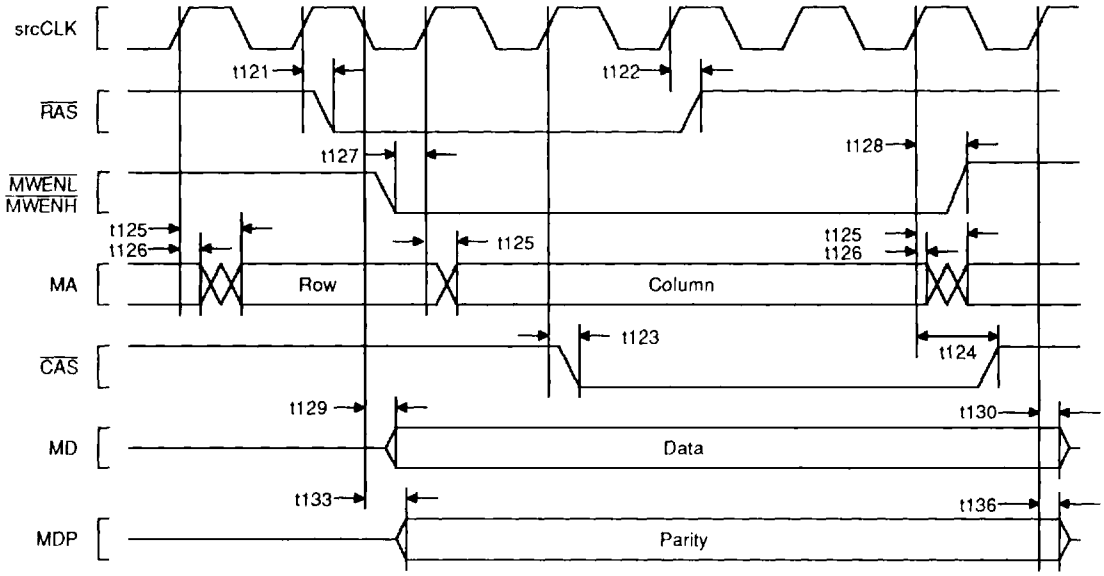


Figure 34. M Bus: Non-Paged Mode—Write/1WS

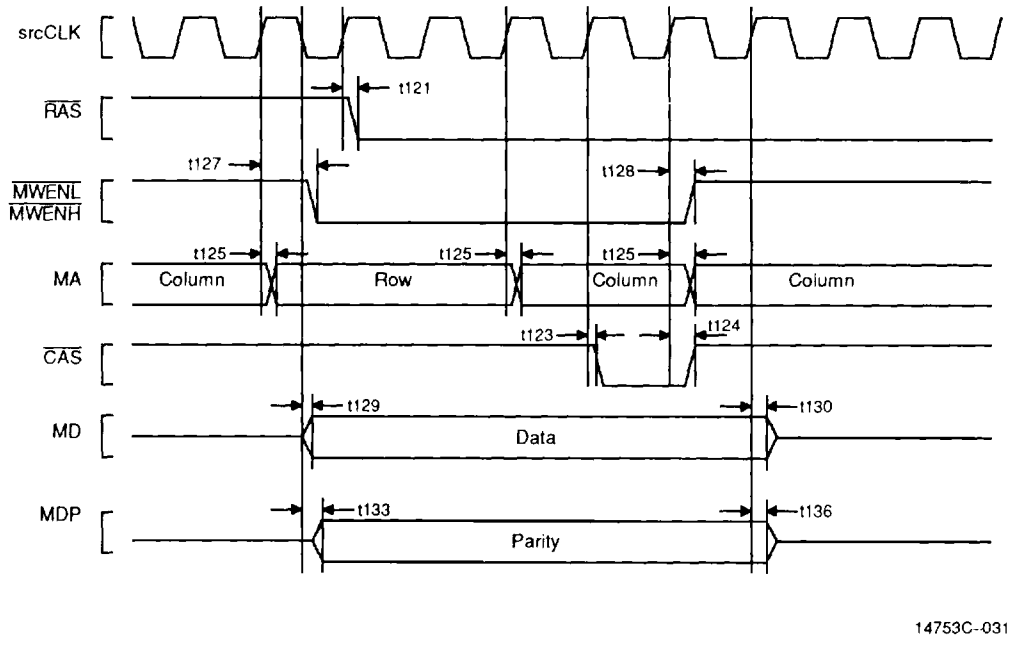


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Figure 35. M Bus: Page Mode, Page—Hit RAS Inactive/Write/0WS

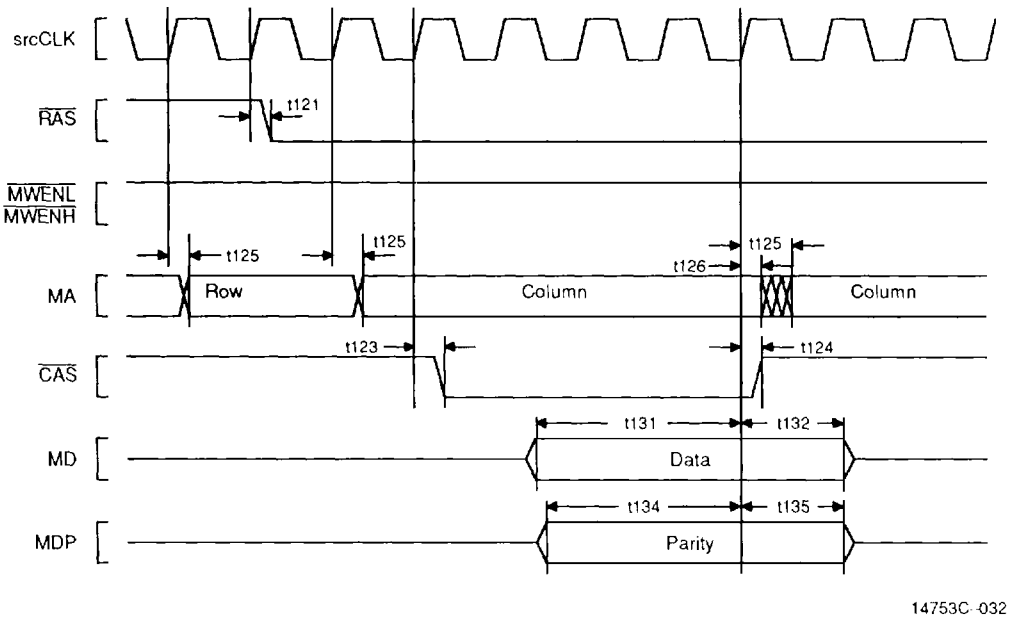


Figure 36. M Bus: Page Mode, Page—Hit RAS Inactive/Read/0WS

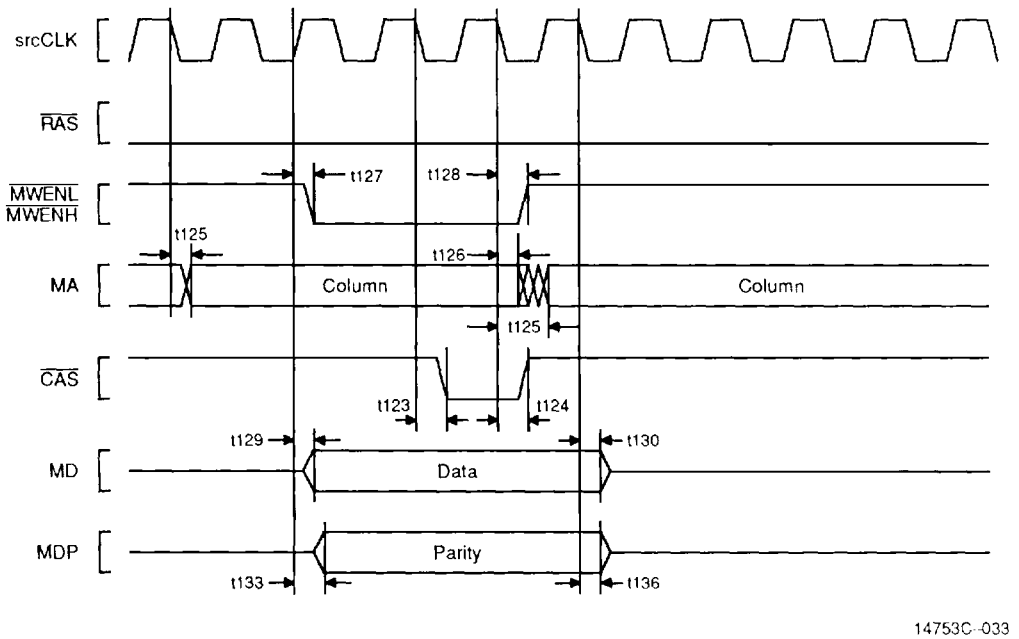


Figure 37. M Bus: Page Mode, Page—Hit/Write/0WS

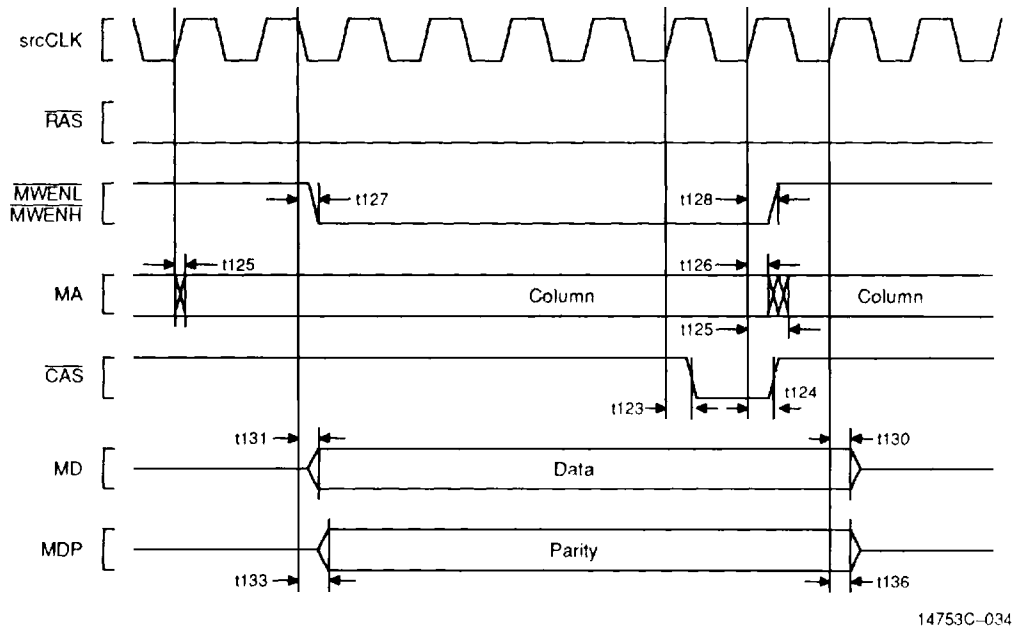


Figure 38. M Bus: Page Mode, Page—Hit RAS Active/Write/1WS

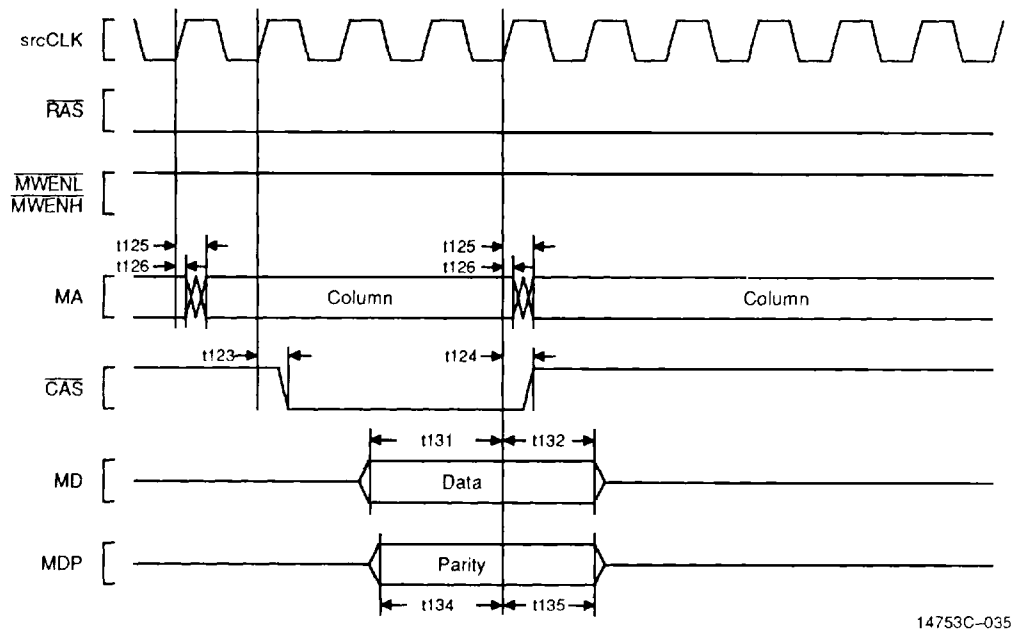


Figure 39. M Bus: Page Mode, Page—Hit RAS Active/0WS/Read

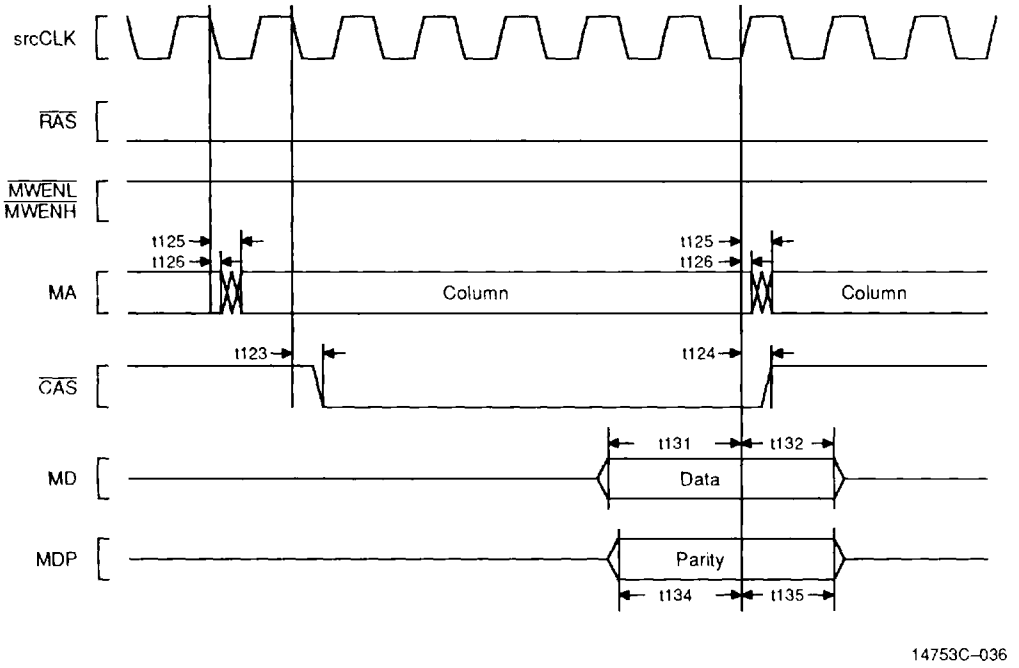


Figure 40. M Bus: Page Mode, Page—Hit $\overline{RAS}$ Active/1WS/Read

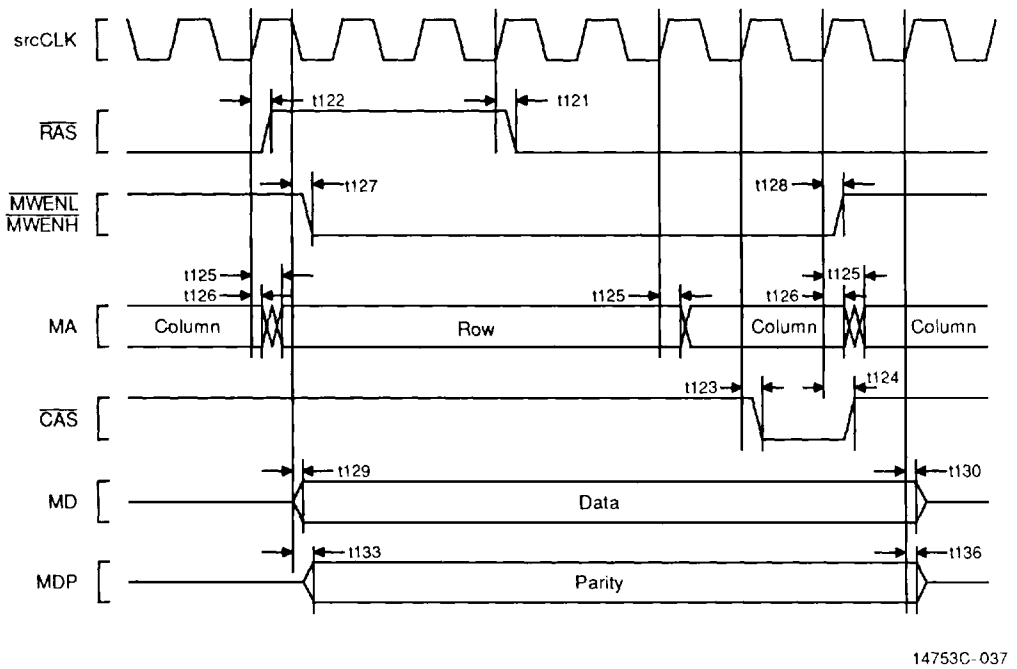


Figure 41. M Bus: Page Mode, Page—Miss/Write/0WS

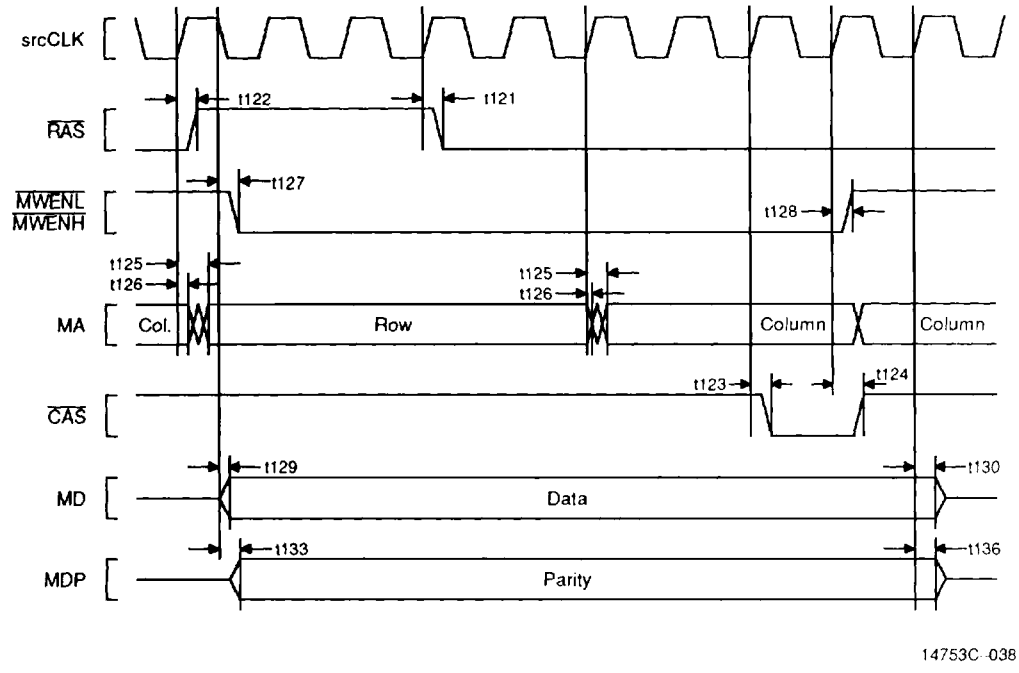


Figure 42. M Bus: Page Mode, Page—Miss/Write/1WS

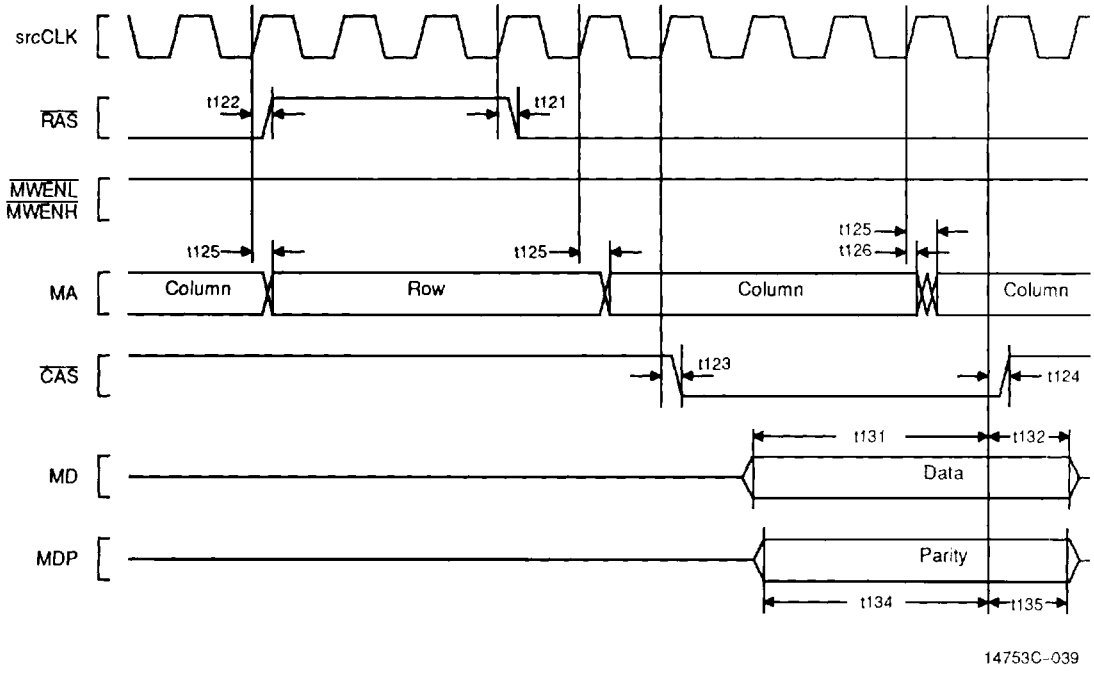
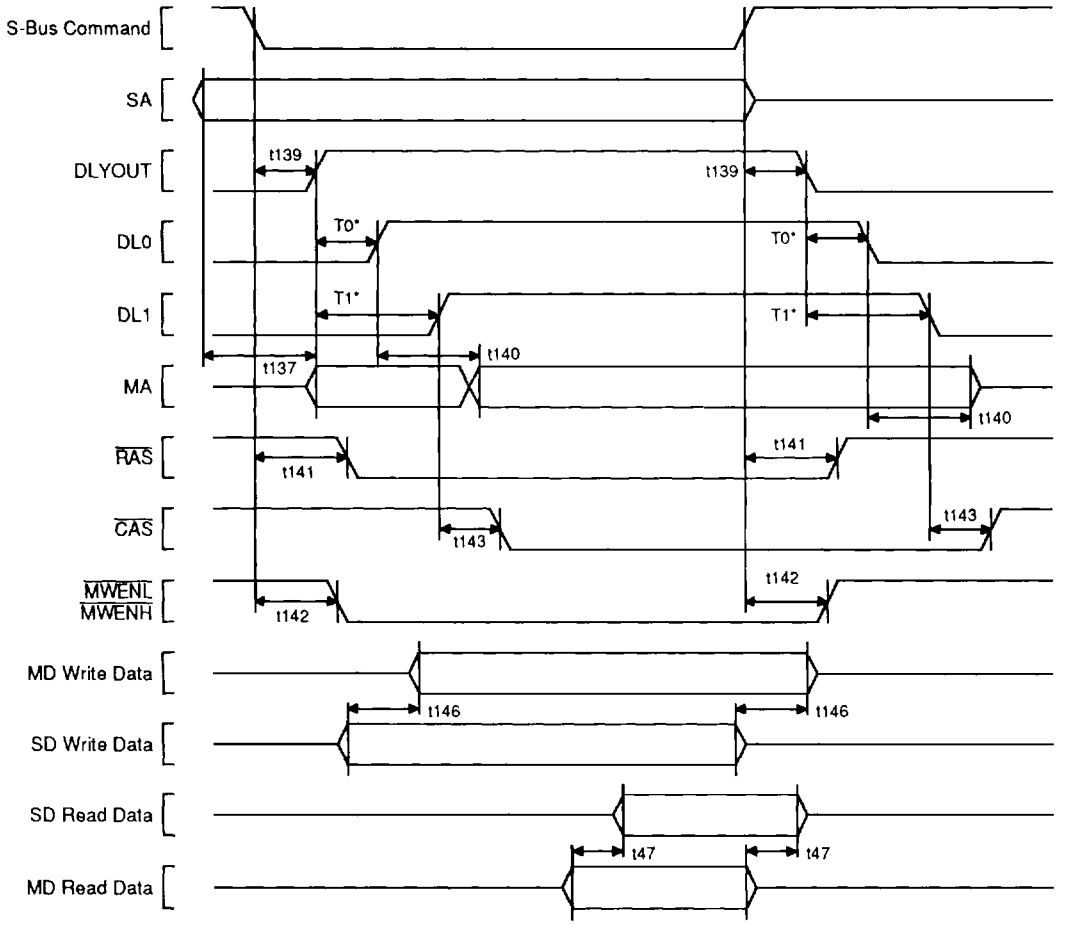


Figure 43. M Bus: Page Mode, Page—Hit $\overline{RAS}$ Inactive/Read/0WS



*T0 and T1 are user selectable via an external delay circuit.

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Figure 44. M Bus: S-Bus Master/DMA Access to Local Memory