M1651T

ALi Super Tualatin Northbridge
AGP 4X, PCI and SDR/DDR Memory Controller

Product Brief

INTRODUCTION

M1651T is ALi's new generation of PCI Northbridge chip supporting the latest Slot-1, Socket-370 Celeron™, Pentium II™, Pentium III™, and Tualatin Processors. It interfaces with the 100/133 front side bus (FSB). It is a single chip solution which provides high performace memory interface for both 66/100/133 SDR and 133/200/266 DDR. The feasible PC-266 DDR enables 2.1 GB/s peak bandwidth between the system memory and Northbridge to boost system performance to the next level.

With AGP 1x/2x/4x support, M1651T prepares system designers with enough head room to interface with different graphics solutions to fulfill various market requirements. ALi also manufactures a series of feature-rich, highly integrated southbridge devices (M1543C, M1535(D), M1535(D)+) which seamlessly work with
M1651T as a complete, flexible and cost-effective solution for notebook designers. M1651T also incorporate ALi's proven power management support which is particularly crucial to mobile applications

Processor Support

- Supports the Celeron™, Pentium II™, Pentium III™, and Tualatin processors. Host bus frequency can be either 100,133MHz.
- 64-bit data bus and 32-bit addressing
- Optimum buffering architecture design for CPU to memory, AGP and PCI read/write
- Flexible configured to support back to back read transfer in 1QW or 2QW
- Supports back to back write transfer
- Optimized processor command scheduling and reordering
- Supports synchronous / asynchronous clock mode between processor and memory interface with optimized latency

Memory Support

- Supports SDRAM / DDR w/ 66, 100, 133MHz
- Supports symmetrical and asymmetrical SDRAM / DDR addressing
- Supports 4, 16, 64, 128, 256, 512Mbit SDRAM / DDR
- Maximum memory size : 3GB
- Supports 6 memory rows with per byte access on each row
- Supports memory shadowing
- x-1-1-1-1-1-1-1 back-to-back page hit
- CAS before RAS and self refresh for SDRAM
- Pipelined SDRAM / DDR cycle control with hidden pre-charge
- Dynamic switching CKE algorithm
- Supports LVTTL / SSTL2 signal level

Accelerated Graphics Port (AGP) Interface

- Supports AGP specification V2.0
- Supports up to 128 entries table look aside buffer for Graphic Address Remapping Table (GART)
- AGP 66MHz protocol
- AGP 1X/2X/4X sideband function
- 28 entries Request queue
- 64 QWORDs Read buffer
- 32 QWORDs Write buffer

PCI Bus Support

- Supports synchronous / asynchronous clock mode between the processor bus and the PCI bus
- 32-bit Address / Data PCI bus using PCI bus driver technology
- Supports up to 6 PCI masters excluding the M1651T and PCI-to-ISA bridge
- Parity protection on all PCI bus signals
- Fully supports PCI Configuration Space Enable (CSE) protocol
- Fully compliant with PCI Rev. 2.2
- Supports delayed transaction
- Dynamic memory prefetch algorithm and programmable post write flush algorithm
- Data Collection/Write assembly of line bursts
- Supports concurrent PCI bus burst transfer at zero wait-states
- 133 MB/sec data streaming for PCI bus to SDRAM / DDR access with minimum latency

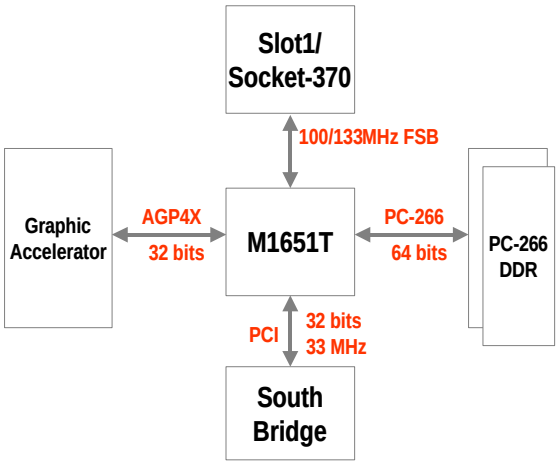
Power Management

- Supports ACPI 1.0b and Legacy green
- Supports PCI Mobile CLKRUN#
- Supports AGP Mobile BUSY# / STOP#
- Internally dynamic clock stop

Packaging

- 528 balls 35x35mm BGA package

M1651T PC-266 SDRAM Architecture



M1651T PC-133 SDRAM Architecture