REALTEK/AVANCE LOGIC, INC.
TWO CHANNEL
AC'97 AUDIO CODEC
ALC201

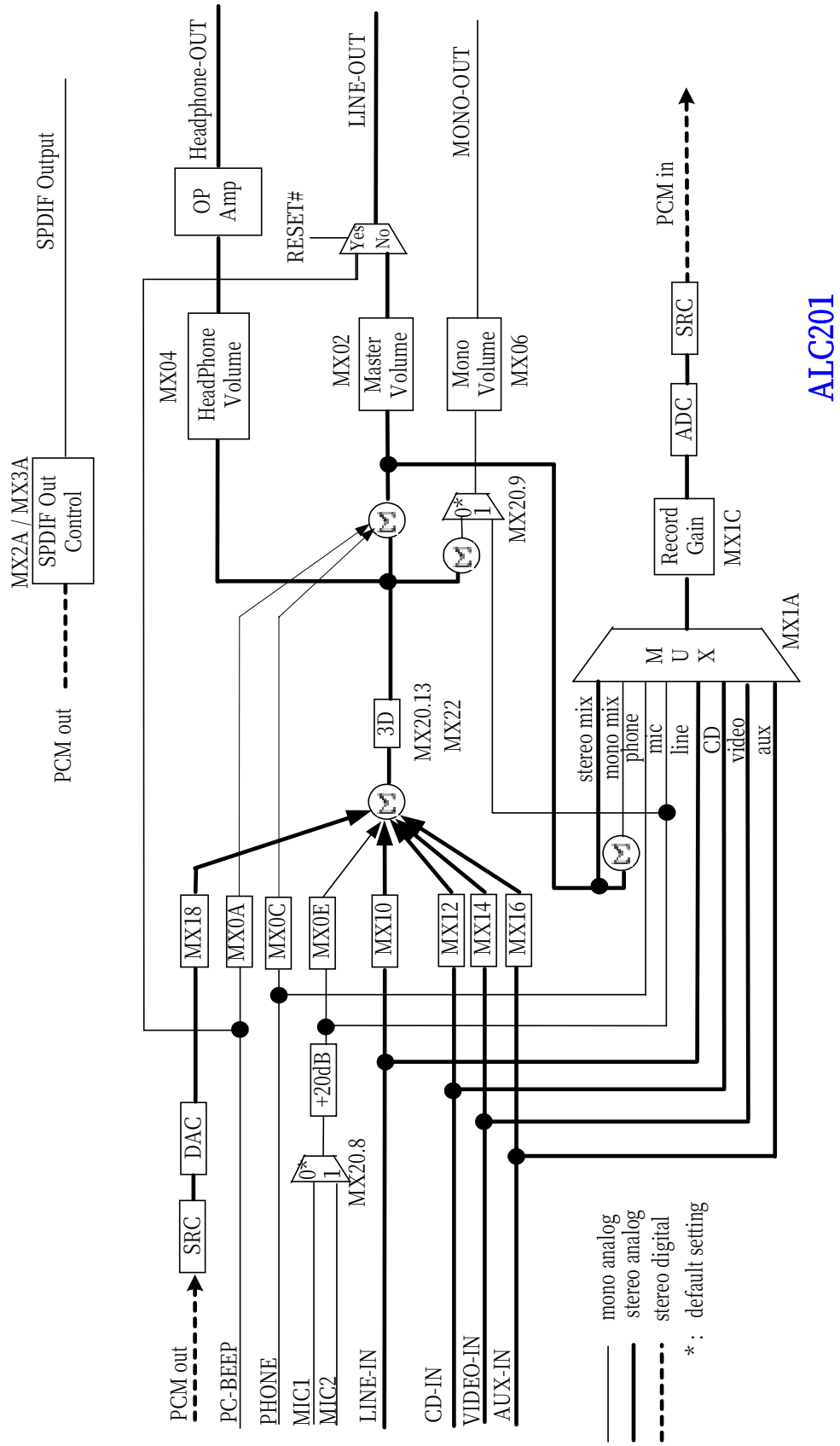
1. Features

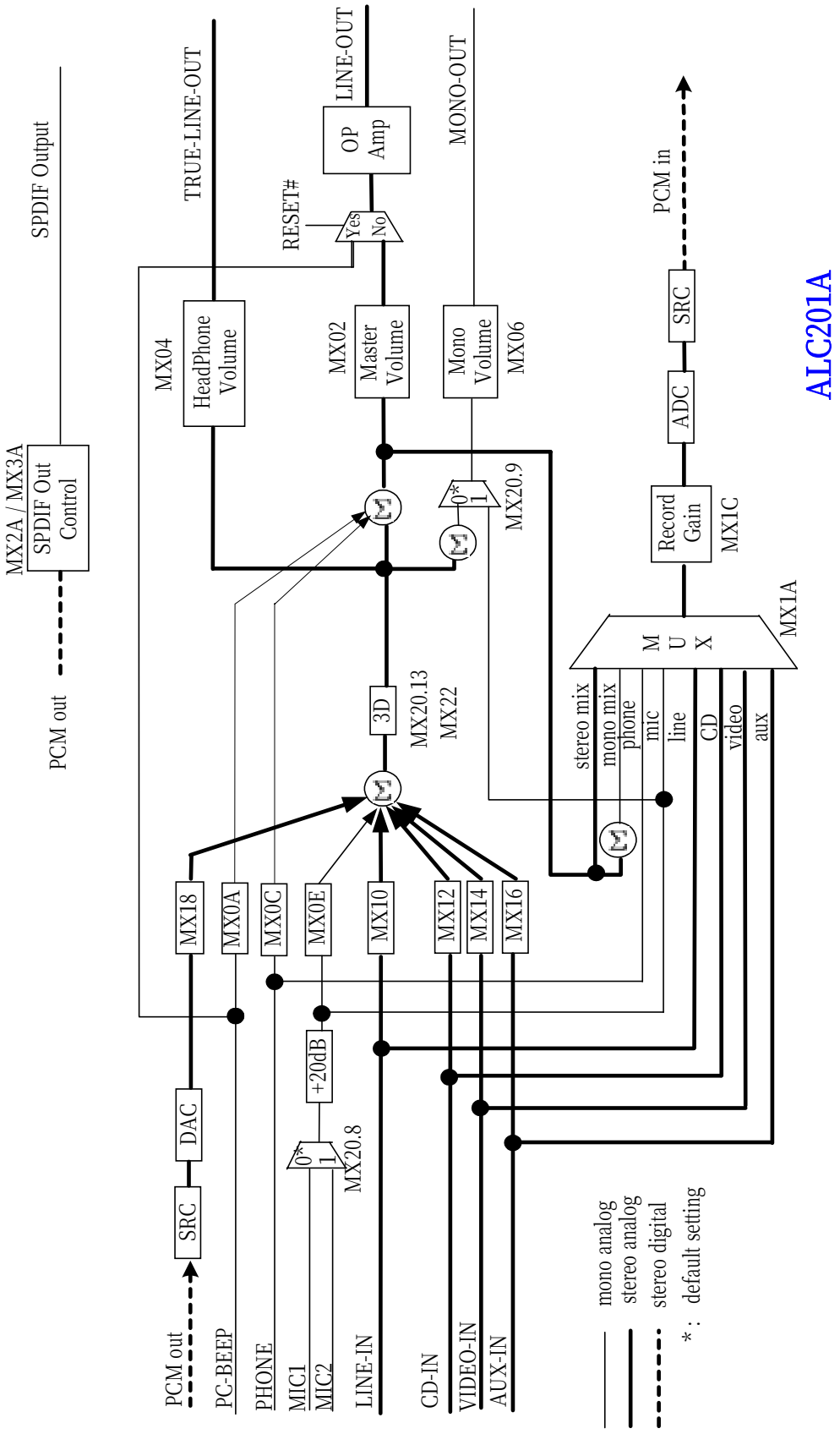
- Single chip audio CODEC with high S/N ratio (>90 dB)
- Compliant with AC'97 2.2 & WHQL specifications
- Support of S/PDIF out is fully compliant with AC'97 rev. 2.2 specifications
- Meets performance requirements for audio on PC2001 systems
- Meets Microsoft PC99 & WLP 2.0 audio requirements
- 18-bit Stereo full-duplex CODEC with independent and variable sampling rate
- 18-bit ADC and DAC resolution
- Four analog line-level stereo inputs with 5-bit volume control: LINE_IN, CD, VIDEO, AUX
- High quality differential CD input
- Two analog line-level mono inputs: PC_BEEP, PHONE_IN
- Two software selectable MIC inputs
- True stereo line level outputs
- Stereo output with 5-bit volume control
- Mono output with 5-bit volume control
- Headphone output with 50mW/20ohm driving capability (ALC201)
- Line output with 50mW/20ohm driving capability (ALC201A)
- Headphone jack-detect function to mute LINE output
- 3D Stereo enhancement
- Multiple CODEC extension capability
- MC'97 Chained in allowing for multi-channel applications
- External Amplifier Power Down (EAPD) capability
- High performance converter technology
- Power management support features
- DC Offset cancellation
- Power support: Digital: 3.3V; Analog: 5V
- Standard 48-Pin LQFP Package

2. General Description

The ALC201A is an 18-bit, full duplex AC'97 2.2 compatible stereo audio CODEC designed for PC multimedia systems, including host/soft audio and AMR/CNR based designs. The ALC201A incorporates proprietary converter technology to achieve a high SNR, greater than 90 dB. The ALC201A AC'97 CODEC supports multiple CODEC extensions with independent variable sampling rates and built-in 3D effects. The ALC201A CODEC provides two pairs of stereo outputs with independent volume controls, a mono output, and multiple stereo and mono inputs, along with flexible mixing, gain and mute functions to provide a complete integrated audio solution for PCs. The digital interface circuitry of the ALC201A CODEC operates from a 5V/3.3V power supply with EAPD (External Amplifier Power Down) control for use in notebook and PC applications. The ALC201A integrates a 50mW/20ohm headset audio amplifier into the CODEC, saving BOM costs. The ALC201A also supports the SPDIF out function, which is compliant to AC'97 2.2, which can offer easy connection of PCs to consumer electronic products, such as AC3 decoder/speaker and mini disk devices. The ALC201A CODEC supports host/soft audio from Intel 810/815/820/845 chipsets as well as audio controller based VIA/SIS/ALI chipsets. Bundled Windows series drivers (Win95/98/ME/2000/XP/NT) and sound effect utilities (supporting Karaoke, 26-kind of environment sound emulation, 5-band equalizer) provide an excellent entertainment package for PC users.

3. Block Diagram

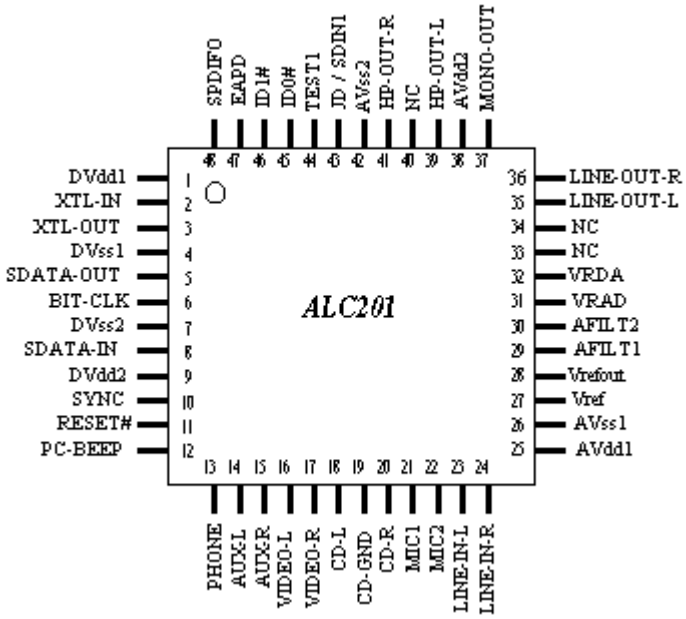



ALC201A
SPDIF Output
TRUE-LINE-OUT
LINE-OUT
MONO-OUT
PCM in
RESET#
Yes
No
OP Amp
MX04
HeadPhone Volume
MX02
Master Volume
Mono Volume
MX06
MX2A / MX3A
SPDIF Out Control
PCM out
MX20.9
0*
1
ADC
SRC
Record Gain
MX1C
MX1A
M U X
3D
MX20.13
MX22
stereo mix
mono mix
phone
mic
line
CD
video
aux
MX18
MX0A
MX0C
MX0E
MX10
MX12
MX14
MX16
+20dB
DAC
SRC
MX20.8
PCM out
PC-BEEP
PHONE
MIC1
MIC2
LINE-IN
CD-IN
VIDEO-IN
AUX-IN
mono analog
stereo analog
stereo digital
*: default setting

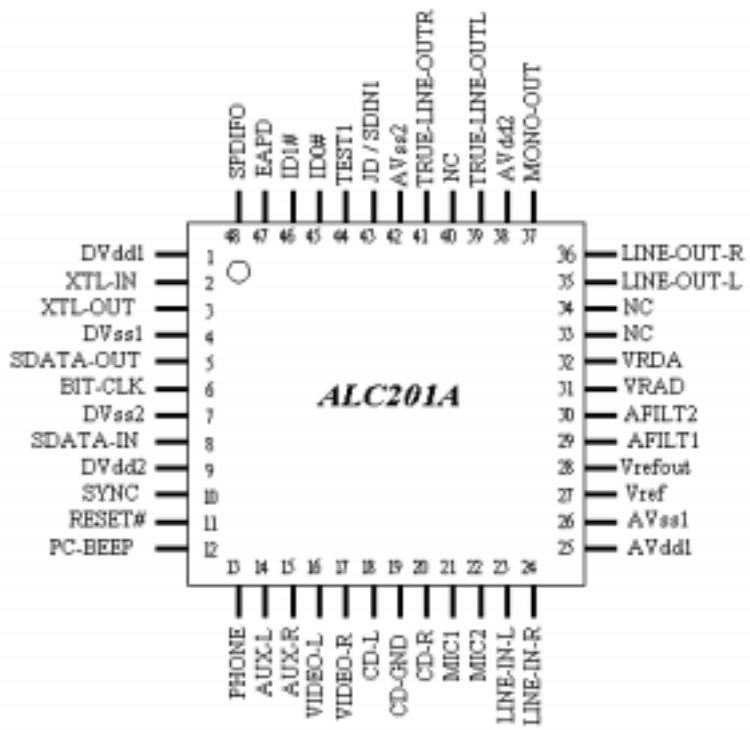
4. Pin Assignments

The ALC201A includes an imbedded op-amp at LINE_OUT (pins 35 & 36). It also supports the standard LINE_OUT function, without an op-amp, at TRUE_LINE_OUT (pins 39 & 41).

ALC201:



ALC201A:



5. Pin Description

5.1 Digital I/O Pins

Name	Type	Pin No	Description	Characteristic Definition
RESET#	I	11	AC'97 master H/W reset	Schmitt trigger input
XTL-IN	I	2	Crystal input pad (24.576Mhz)	Crystal input pad
XTL-OUT	O	3	Crystal output pad	Crystal output pad
SYNC	I	10	Sample Sync (48Khz)	Schmitt trigger input
BIT-CLK	IO	6	Bit clock output (12.288Mhz)	CMOS input/output Vt=0.35Vdd
SDATA-OUT	I	5	Serial TDM AC97 output	Schmitt trigger input
SDATA-IN	O	8	Serial TDM AC97 input	CMOS output
JD / SDIN1	I	43	Jack –Detect sense a low to high edge / SDATA-IN from chained CODEC	Digital input
ID0#	I	45	ID strap 0	CMOS input Vt=0.35Vdd
ID1#	I	46	ID strap 1	CMOS input Vt=0.35Vdd
EAPD	O	47	External Amplifier power down control	2mA CMOS output
SPDIFO	O	48	S/PDIF output	Digital output
				TOTAL: 11 Pins

5.2 Analog I/O Pins

Name	Type	Pin No	Description	Characteristic Definition
PC-BEEP	I	12	PC speaker input	Analog input (1Vrms)
PHONE	I	13	Speakerphone input	Analog input (1Vrms)
AUX-L	I	14	AUX Left channel	Analog input (1Vrms)
AUX-R	I	15	AUX Right channel	Analog input (1Vrms)
VIDEO-L	I	16	Video audio Left channel	Analog input (1Vrms)
VIDEO-R	I	17	Video audio Right channel	Analog input (1Vrms)
CD-L	I	18	CD audio Left channel	Analog input (1Vrms)
CD-GND	I	19	CD audio analog GND	Analog input (1Vrms)
CD-R	I	20	CD audio Right channel	Analog input (1Vrms)
MIC1	I	21	First Mic input	Analog input (1Vrms)
MIC2	I	22	Second Mic input	Analog input (1Vrms)
LINE-L	I	23	Line input Left channel	Analog input (1Vrms)
LINE-R	I	24	Line input Right channel	Analog input (1Vrms)
LINE-OUTL	O	35	Line-Out Left channel	Analog output (ALC201: 1.1Vrms) Analog output (ALC201A: 1.7Vrms)
LINE-OUTR	O	36	Line-Out Right channel	Analog output (ALC201: 1.1Vrms) Analog output (ALC201A: 1.7Vrms)
HP-OUT-L	O	39 (ALC201)	Headphone Out – Left	Analog output (1.7Vrms)
HP-OUT-R	O	41 (ALC201)	Headphone Out – Right	Analog output (1.7Vrms)
TRUE-LINE-OUTL	O	39 (ALC201A)	True Line Out – Left	Analog output (1.1Vrms)
TRUE-LINE-OUTR	O	41 (ALC201A)	True Line Out – Right	Analog output (1.1Vrms)
MONO-OUT	O	37	Speaker Phone output	Analog output (1.1Vrms)
				TOTAL: 18 Pins

5.3 Filter/Reference

Name	Type	Pin No	Description	Characteristic Definition

VREF	O	27	Reference voltage	Analog output
VREFOUT	O	28	Ref. voltage out with 5mA drive	Analog output (2.25V – 2.75V)
AFILT1	O	29	ADC anti-aliasing filter capacitor	Analog output
AFILT2	O	30	ADC anti-aliasing filter capacitor	Analog output
VRAD	O	31	Vref for ADC	Analog output
VRDA	O	32	Vref for DAC	Analog output
				TOTAL: 7 Pins

5.4 Power/Ground

Name	Type	Pin No	Description	Characteristic Definition
AVDD1	I	25	Analog VDD (5.0V)	
AVDD2	I	38	Analog VDD (5.0V)	
AVSS1	I	26	Analog GND	
AVSS2	I	42	Analog GND	
VDD1	I	1	Digital VDD (3.3V)	
VDD2	I	9	Digital VDD (3.3V)	
VSS1	I	4	Digital GND	
VSS2	I	7	Digital GND	
				TOTAL: 8 Pins

5.5 Others

Name	Type	Pin No	Description	Characteristic Definition
TEST1	O	44	Output DAC clock and ADC clock	Digital output
NC		33,34,40	No Connection.	
				TOTAL: 4 Pins

6. Registers

6.1 Mixer Registers

Access to registers with an odd number will return a 0. Reading unimplemented registers will also return a 0.

REG. (HEX)	NAME	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
00h	Reset	X	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	5950h
02h	Master Volume	Mute	X	X	ML4	ML3	ML2	ML1	ML0	X	X	X	MR4	MR3	MR2	MR1	MR0	8000h
04h	Headphone volume	Mute	X	X	HPL 4	HPL 3	HPL 2	HPL 1	HPL 0	X	X	X	HPR 4	HPR 3	HPR 2	HPR 1	HPR 0	8000h
06h	Mono-Out Volume	Mute	X	X	X	X	X	X	X	X	X	X	MM 4	MM 3	MM 2	MM 1	MM 0	8000h
0Ah	PC_BEEP Volume	Mute	X	X	X	X	X	X	X	X	X	X	PB3	PB2	PB1	PB0	X	0000h
0Ch	PHONE Volume	Mute	X	X	X	X	X	X	X	X	X	X	PH4	PH3	PH2	PH1	PH0	8008h
0Eh	MIC Volume	Mute	X	X	X	X	X	X	X	X	20d B	X	MI4	MI3	MI2	MI1	MI0	8008h
10h	Line-In Volume	Mute	X	X	NL4	NL3	NL2	NL1	NL0	X	X	X	NR4	NR3	NR2	NR1	NR0	8808h
12h	CD Volume	Mute	X	X	CL4	CL3	CL2	CL1	CL0	X	X	X	CR4	CR3	CR2	CR1	CR0	8808h
14h	Video Volume	Mute	X	X	VL4	VL3	VL2	VL1	VL0	X	X	X	VR4	VR3	VR2	VR1	VR0	8808h
16h	Aux Volume	Mute	X	X	AL4	AL3	AL2	AL1	AL0	X	X	X	AR4	AR3	AR2	AR1	AR0	8808h
18h	PCM Out Volume	Mute	X	X	PL4	PL3	PL2	PL1	PL0	X	X	X	PR4	PR3	PR2	PR1	PR0	8808h
1Ah	Record Select	X	X	X	X	X	LRS 2	LRS 1	LRS 0	X	X	X	X	X	RRS 2	RRS 1	RRS 0	0000h
1Ch	Record Gain	Mute	X	X	X	LRG 3	LRG 2	LRG 1	LRG 0	X	X	X	X	RRG 3	RRG 2	RRG 1	RRG 0	8000h
20h	General Purpose	POP	X	3D	X	X	X	MIX	MS	LBK	X	X	X	X	X	X	X	0000h
22h	3D Control	X	X	X	X	X	X	X	X	X	X	X	X	X	X	DP1	DP0	0000h
24h	Alias MX6A	SM1	SM0	0	X	X	X	X	X	X	X	0	0	0	0	0	0	0000h
26h	Power Down Ctrl/Status	EAP D	PR6	PR5	PR4	PR3	PR2	PR1	PR0	X	X	X	X	REF	ANL	DAC	ADC	000Fh
28h	Extended Audio ID	ID1	ID0	X	X	REV 1	REV 0	AM AP	X	X	X	X	X	X	SPD IF	X	VRA	0605h
2Ah	Extended Audio Status	X	X	X	X	X	SPC V	X	X	X	X	SPS A1	SPS A0	X	SPD IF	X	VRA	0000h
2Ch	PCM front Out Sample Rate	FSR 15	FSR 14	FSR 13	FSR 12	FSR 11	FSR 10	FSR 9	FSR 8	FSR 7	FSR 6	FSR 5	FSR 4	FSR 3	FSR 2	FSR 1	FSR 0	BB80h
32h	PCM Input Sample Rate	ISR 15	ISR 14	ISR 13	ISR 12	ISR 11	ISR 10	ISR 9	ISR 8	ISR 7	ISR 6	ISR 5	ISR 4	ISR 3	ISR 2	ISR 1	ISR 0	BB80h
3Ah	S/PDIF Ctl	V	0	SPS R1	SPS R0	L	CC6	CC5	CC4	CC3	CC2	CC1	CC0	PRE	COP Y	/AU DIO	PRO	2000h
6Ah	Multi-chann el Ctl	SM1	SM0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	0000h
7Ch	Vendor ID1	0	1	0	0	0	0	0	1	0	1	0	0	1	1	0	0	414Ch
7Eh	Vendor ID2	0	1	0	0	0	1	1	1	0	0	0	1	V3	V2	V1	V0	4710h

X: reserved bit

*: MX04 is used to control the 'Headphone Output Volume' as per AC'97 rev2.2 specifications.
MX24 is the alias mixer of MX6A when the ALC201/ALC201A is identified as operating in 'Chain' mode.

6.2 MX00 Reset
Default: 5950H

Writing any value to this register will start a register reset, and causes all of the registers to revert to their default values. Reading this register returns the ID code of the specific part.

Bit	Type	Function
15		**Reserved**
14:10	R	Returns 10110b
9	R	Read as 0 (Does not support 20-bit ADC)
8	R	Read as 1 (Supports 18-bit ADC)
7	R	Read as 0 (Does not support 20-bit DAC)
6	R	Read as 1 (Supports 18-bit DAC)
5	R	Read as 0 (No support for Loudness)
4	R	Read as 1 (Headphone output support)
3	R	Read as 0 (No simulated stereo, for analog 3D block use)
2	R	Read as 0 (No Bass & Treble Control)
1	R	**Reserved**, Read as 0
0	R	Read as 0 (No Dedicated Mic PCM input)

Writing to this register will reset all mixer registers to their default value. The write data is ignored.

6.3 MX02 Master Volume
Default: 8000H / 0000H

This register controls the overall volume level of the output functions. Each step on the left and right channels correspond to 1.5dB in increase/decrease in volume.

Bit	Type	Function
15	R/W	**Mute Control** 0: Normal 1: Mute (-∞ dB)
14:13		**Reserved**
12:8	R/W	**Master Left Volume** (MLV[4..0]) in 1.5 dB steps
7:5		**Reserved**
4:0	R/W	**Master Right Volume** (MRV[4..0]) in 1.5 dB steps

❶ For MRV/MLV: 00h 0 dB attenuation
1Fh 46.5 dB attenuation

❷ Implement 5-bit volume control only. Writing 1xxxxx will be interpreted as x11111 and when read will respond with x11111.

❸ When ID=01,10,11, the default value is 0000H.

6.4 MX04 Headphone/True Line Output Volume
Default: 8000H

Register 04h controls the headphone (ALC201)/True Line (ALC201A) output volume. Each step in bits 0..4 and 8..12 correspond to 1.5dB in increase/decrease in volume, allowing 32 levels of volume, from 00000 to 11111.

Bit	Type	Function
15	R/W	**Mute Control** 0: Normal 1: Mute (-∞ dB)
14:13		**Reserved**
12:8	R/W	**Headphone Output Left Volume** (HPL[4..0]) in 1.5 dB steps
7:5		**Reserved**
4:0	R/W	**Headphone Output Right Volume** (HPR[4..0]) in 1.5 dB steps

❶ For HPR/HPL: 00h 0 dB attenuation
1Fh 46.5 dB attenuation

❷ Implement 5-bit volume control only. Writing 1xxxxx will be interpreted as x11111 and when read will respond with x11111.

6.5 MX06 MONO_OUT Volume
Default: 8000H

Register 06h controls the mono volume output. Mono output is the same data sent on all output channels. Each step in bits 0..4 correspond to 1.5dB in increase/decrease in volume, allowing 32 levels of volume from 00000 to 11111.

Bit	Type	Function
15	R/W	**Mute Control** 0: Normal 1: Mute (-∞ dB)
14:5		**Reserved**
4:0	R/W	**Mono Master Volume** (MMV[4..0]) in 1.5 dB steps

❶ For MMV: 00h 0 dB attenuation
1Fh 46.5 dB attenuation

❷Implement 5-bit volume control only. Writing 1xxxxx will be interpreted as x11111 and when read will respond with x11111.

6.6 MX0A PC BEEP Volume
Default: 0000H

This register controls the input volume for the PC beep signal. Each step in bits 1..4 correspond to a 3dB increase/decrease in volume. 16 levels of volume are available, from 0000 to 1111.

The purpose of this register is to allow the PC Beep signals to pass through the ALC210/ALC210A, eliminating the need for an external system speaker/buzzer. The PC BEEP pin is directly routed (internally hardwired) to the LINE-OUTL & R pins. If the PC speaker/buzzer is eliminated, it is recommended to connect the external speakers at all times so the POST codes can be heard during reset.

Bit	Type	Function
15	R/W	**Mute Control** 0: Normal 1: Mute (-∞ dB)
14:5		**Reserved**
4:1	R/W	**PC Beep Volume** (PBV[3..0]) in 3 dB steps
0		**Reserved**

For PBV: 00h 0 dB attenuation
0Fh 45 dB attenuation

6.7 MX0C PHONE Volume
Default: 8008H

Register 0Ch controls the telephone input volume for software modem applications. Because software modem applications may not have a speaker, the CODEC can offer a speaker-out service. Each step in bits 0..4 correspond to 1.5dB in increase/decrease in volume, allowing 32 levels of volume, from 00000 to 11111.

Bit	Type	Function
15	R/W	**Mute Control** 0: Normal 1: Mute (-∞ dB)
14:5		**Reserved**
4:0	R/W	**Phone Volume** (PV[4..0]) in 1.5 dB steps

For PV: 00h +12 dB Gain
08h 0dB gain
1Fh -34.5dB Gain

6.8 MX0E MIC Volume
Default: 8008H

Register 0Eh controls the microphone input volume. Each step in bits 0..4 correspond to 1.5dB in increase/decrease in volume, allowing 32 levels of volume, from 00000 to 11111. Each step in bit 6 corresponds to a magnification of 20dB increase in volume.

Bit	Type	Function
15	R/W	**Mute Control** 0: Normal 1: Mute (-∞ dB)
14:7		**Reserved**
6	R/W	**20 dB Boost Control** 0: Normal 1: 20 dB boost
5		**Reserved**
4:0	R/W	**Mic Volume** (MV[4..0]) in 1.5 dB steps

For MV: 00h +12 dB Gain
08h 0dB gain
1Fh -34.5dB Gain

6.9 MX10 LINE_IN Volume
Default: 8808H

Register 10h controls the LINE_IN input volume. Each step in bits 0..4 correspond to 1.5dB in increase/decrease in volume for the right channel, allowing 32 levels of volume, from 00000 to 11111. Each step in bits 8..12 correspond to 1.5dB in increase/decrease in volume for the left channel, allowing 32 levels of volume, from 00000 to 11111.

Bit	Type	Function
15	R/W	**Mute Control** 0: Normal 1: Mute (-∞ dB)
14:13		**Reserved**
12:8	R/W	**Line-In Left Volume** (NLV[4..0]) in 1.5 dB steps
7:5		**Reserved**
4:0	R/W	**Line-In Right Volume** (NRV[4..0]) in 1.5 dB steps

For NLV/NRV: 00h +12 dB Gain
08h 0dB gain
1Fh -34.5dB Gain

6.10 MX12 CD Volume
Default: 8808H

Register 12h controls the CD input volume. Each step in bits 0..4 correspond to 1.5dB in increase/decrease in volume for the right channel, allowing 32 levels of volume, from 00000 to 11111. Each step in bits 8..12 correspond to 1.5dB in increase/decrease in volume for the left channel, allowing 32 levels of volume, from 00000 to 11111.

Bit	Type	Function
15	R/W	**Mute Control** 0: Normal 1: Mute (-∞ dB)
14:13		**Reserved**
12:8	R/W	**CD Left Volume** (CLV[4..0]) in 1.5 dB steps
7:5		**Reserved**
4:0	R/W	**CD Right Volume** (CRV[4..0]) in 1.5 dB steps

For CLV/CRV: 00h +12 dB Gain
08h 0dB gain
1Fh -34.5dB Gain

6.11 MX14 VIDEO Volume
Default: 8808H

Register 14h controls the video input volume. Each step in bits 0..4 correspond to 1.5dB in increase/decrease in volume for the right channel, allowing 32 levels of volume, from 00000 to 11111. Each step in bits 8..12 correspond to 1.5dB in increase/decrease in volume for the left channel, allowing 32 levels of volume, from 00000 to 11111.

Bit	Type	Function
15	R/W	**Mute Control** 0: Normal 1: Mute (-∞ dB)
14:13		**Reserved**
12:8	R/W	**Video Left Volume** (VLV[4..0]) in 1.5 dB steps
7:5		**Reserved**
4:0	R/W	**Video Right Volume** (VRV[4..0]) in 1.5 dB steps

For VLV/VRV: 00h +12 dB Gain
08h 0dB gain
1Fh -34.5dB Gain

6.12 MX16 AUX Volume
Default: 8808H

Register 16h controls the auxiliary input volume. Each step in bits 0..4 correspond to 1.5dB in increase/decrease in volume for the right channel, allowing 32 levels of volume, from 00000 to 11111. Each step in bits 8..12 correspond to 1.5dB in increase/decrease in volume for the left channel, allowing 32 levels of volume, from 00000 to 11111.

Bit	Type	Function
15	R/W	**Mute Control** 0: Normal 1: Mute (-∞ dB)
14:13		**Reserved**
12:8	R/W	**AUX Left Volume** (ALV[4..0]) in 1.5 dB steps
7:5		**Reserved**
4:0	R/W	**AUX Right Volume** (ARV[4..0]) in 1.5 dB steps

For ALV/ARV: 00h +12 dB Gain
08h 0dB gain
1Fh -34.5dB Gain

6.13 MX18 PCM_OUT Volume
Default: 8808H

Register 18h controls the PCM_OUT output volume. Each step in bits 0..4 correspond to 1.5dB in increase/decrease in volume for the right channel, allowing 32 levels of volume, from 00000 to 11111. Each step in bits 8..12 correspond to 1.5dB in increase/decrease in volume for the left channel, allowing 32 levels of volume, from 00000 to 11111.

Bit	Type	Function
15	R/W	**Mute Control** 0: Normal 1: Mute (-∞ dB)
14:13		**Reserved**
12:8	R/W	**PCM Volume** (PLV[4..0]) in 1.5 dB steps
7:5		**Reserved**
4:0	R/W	**PCM Right Volume** (PRV[4..0]) in 1.5 dB steps

For PLV/PRV: 00h +12 dB Gain
08h 0dB gain
1Fh -34.5dB Gain

6.14 MX1A Record Select
Default: 0000H

Register 1Ah controls the record input selection. Depending on the value entered, the record input can be taken from the Mic, CD, Video, Aux, Line, Stereo Mixer, Mono Mixer or Phone.

Bit	Type	Function
15:11		**Reserved**
10:8	R/W	**Left Record Source Select** (LRS[2..0])
7:3		**Reserved**
2:0	R/W	**Right Record Source Select** (RRS[2..0])

❶ For LRS

0 MIC
1 CD LEFT
2 VIDEO LEFT
3 AUX LEFT
4 LINE LEFT
5 STEREO MIXER OUTPUT LEFT
6 MONO MIXER OUTPUT
7 PHONE

❷ For RRS

0 MIC
1 CD RIGHT
2 VIDEO RIGHT
3 AUX RIGHT
4 LINE RIGHT
5 STEREO MIXER OUTPUT RIGHT
6 MONO MIXER OUTPUT
7 PHONE

6.15 MX1C Record Gain
Default: 8000H

Register 1Ch controls the record gain. Each step in bits 0..3 correspond to 1.5dB in increase/decrease in gain for the right channel, allowing 16 levels of gain, from 0000 to 1111. Each step in bits 8..11 correspond to 1.5dB in increase/decrease in gain for the left channel, allowing 16 levels of gain, from 0000 to 1111.

Bit	Type	Function
15	R/W	**Mute Control** 0: Normal 1: Mute (-∞ dB)
14:12		**Reserved**
11:8	R/W	**Left Record Gain Select** (LRG[3..0]) in 1.5 dB steps
7:4		**Reserved**
3:0	R/W	**Right Record Gain Select** (RRG[3..0]) in 1.5 dB steps

For LRG/RRG: 0Fh +22.5dB
00h 0 dB (No Gain)

6.16 MX20 General Purpose
Default: 0000H

This register is used to control several functions. Bit 13 enables or disables 3D control. Bit 9 allows selection of mono output. Bit 8 controls the mic selector. Bit 7 enables loopback of the AD output to the DA input without involving the AC-Link, allowing for full system performance measurements.

Bit	Type	Function
15:14		**Reserved**, Read as 0
13	R/W	**3D Control** 1: On 0: Off
12:10		**Reserved**, Read as 0
9	R/W	**Mono Output Select** 0: MIX 1: MIC
8	R/W	**Mic Select** 0: Mic 1 1: Mic 2
7	R/W	**AD to DA Loopback Control** 0: Disable 1: Enable
6:0		**Reserved**

6.17 MX22 3D Control
Default: 0000H

This register is used to control the 3D stereo enhancement function built into the AC'97 component. The register bits, DP1-DP0 are used to control the separation ratios in the 3D control for both LINE_OUT and DAC_OUT respectively. This allows for independent control of the stereo enhancement between LINE_OUT and DAC_OUT.

The 3D stereo enhancement function provides for a deeper and wider sound experience with a potential 6-speaker arrangement. Note that the 3D bit in the general purpose register (bit 13) must be set to 1 to enable this function.

Bit	Type	Function
15:2		**Reserved**, Read as 0
1:0	R/W	**Depth Control** (DP[1..0])

3D effect control:

DP[1..0]	Function
00	0%(off)
01	50%
10	75%
11	100%

6.18 MX24 Reserved/Alias Mixer of MX6A
Default: 0000h

Bit	Type	Function
15:0	R/W	Refers to MX6A.

In normal mode, this mixer is a reserved mixer defined in AC'97 rev2.2, any write to MX24 is ignored, and read as 0.

In 'Chain-In' mode (session 9-8), this mixer is the alias mixer of MX6A. The functions defined in MX6A are moved into MX24, any write to MX6A is no more effective, and read MX6A as 0.

6.19 MX26 Powerdown Control/Status
Default: 000FH

This read/write register is used to program powerdown states and monitor subsystem readiness. The lower half of this register is read only status; a "1" indicating that the subsection is "ready." Ready is defined as the subsection's ability to perform in its nominal state. When this register is written, the bit values that come in on AC-Link will have no effect on read only bits 0-7 and bit 15.

When the AC-Link "CODEC Ready" indicator bit (SDATA_IN slot 0, bit 15) is a 1, it indicates that the AC-Link and AC'97 control and status registers are in a fully operational state. The AC'97 controller must further probe this powerdown control /status register to determine exactly which subsections, if any are ready.

Bit	Type	Function
15	R/W	PR7 **External Amplifier Power Down** (EAPD) 0: normal 1: Power down
14	R/W	PR6 0: Normal 1:Power down Headphone Out / True-Line-Out
13	R/W	PR5 0: Normal 1: Disable internal clock
12	R/W	PR4 0: Normal 1: Power down AC-Link
11	R/W	PR3 0: Normal 1: Power down Mixer (Vref off)
10	R/W	PR2 0: Normal 1: Power down Mixer (Vref still on)
9	R/W	PR1 0: Normal 1: Power down PCM DAC
8	R/W	PR0 0: Normal 1: Power down PCM ADC and input MUX
7:4		**Reserved**, Read as 0
3	R	**Vref Status** 1: Vref is up to normal level 0: Not yet
2	R	**Analog Mixer Status** 1: Ready 0: Not yet
1	R	**DAC Status** 1: Ready 0: Not yet
0	R	**ADC Status** 1: Ready 0: Not yet

True table for power down mode:

	ADC	DAC	Mixer	Vref	ACLINK	Int CLK	HP-OUT	EAPD
PR0=1	PD							
PR1=1		PD						
PR2=1	PD	PD	PD				PD	
PR3=1	PD	PD	PD	PD			PD	
PR4=1	PD	PD			PD			
PR5=1	PD	PD				PD		
PR6=1							PD	
PR7=1								PD

PD: Power down Blank: Don't care

6.20 MX28 Extended Audio ID
Default: 0605H

The Extended Audio ID register is a read only register used to communicate information to the digital controller on two functions. ID1 and ID0 echo the configuration of the CODEC as defined by the programming of pins 47 and 48 externally. "00" returned defines the CODEC as the primary CODEC, while any other code identifies the CODEC as one of three secondary CODEC possibilities.

Bit	Type	Function
15	R	**ID1**
14	R	**ID0**
13:12		**Reserved**, Read as 0
11:10	R	**REV** [1:0]=01 to indicates ALC201/ALC201A is AC'97 rev2.2 compliant.
9	R	**AMAP**, Read as 1 (DAC mapping base on CODEC ID)
8:3		**Reserved**, Read as 0
2	R	**SPDIF**, Read as 1 (S/PDIF is supported)
1		**Reserved**, Read as 0
0	R	**VRA**, Read as 1 (Variable sample rate is supported)

❶ ID1 is latched inversely from pin 46 when the system is reset. ID0 is latched inversely from pin 45 when the system is reset.

❷ The ALC201/ALC201A maps the DAC slot according to the following table (AC'97 rev2.2)

ID[1..0]	PCM Left DAC slot #	PCM Right DAC slot #	Comment
00	3	4	Primary
01	7	8	Secondary (Surround)
10	7	8	Secondary (Surround)
11	6	9	Secondary (Center/LFE)

6.21 MX2A Extended Audio Status and Control Default: 00X0H

This register contains two active bits for powerdown and status of the surrounding DACs. Bits 0, 1 & 2 are read/write bits which are used to enable or disable VRA, DRA and SPDIF respectively. Bits 4 & 5 are read/write bits used to determine the AC-LINK slot assignment of the S/PDIF. Bits 6, 7 & 8 are read only bits which tell the controller when the Center, Surround and LFE DACs are ready to receive data. Bit 10 is a read only bit which tells the controller if the S/PDIF configuration is valid. Bits 11, 12 & 13 are read/write bits which are used to powerdown the Center, Surround and LFE DACs respectively.

Bit	Type	Function
15:11		**Reserved**
10	R	**SPCV*** (S/PDIF Configuration Valid) 0: current S/PDIF configuration {SPSA,SPSR,DAC/slot rate} is not valid. 1: current S/PDIF configuration {SPSA,SPSR,DAC/slot rate} is valid.
9:6		**Reserved**
5:4	R/W	**SPSA**[1:0] (S/PDIF Slot Assignment) 00: S/PDIF source data assigned to AC-LINK slot3/4. 01: S/PDIF source data assigned to AC-LINK slot7/8 (**default when ID=00**). 10: S/PDIF source data assigned to AC-LINK slot6/9 (**default when ID=01,10**). 11: S/PDIF source data assigned to AC-LINK slot10/11 (**default when ID=11**).
3		**Reserved**
2	R/W	**SPDIF Enable** 1: enable 0: disable(Hi-Z)
1		**Reserved**
0	R/W	**VRA**† 1: enable 0: disable

* SPCV is a read only bit that indicates whether the current S/PDIF configuration is supported or not. If the configuration is supported, SPCV is set as 1 by H/W. So driver can check this bit to determine the status of the S/PDIF transmitter system. SPCV is always operating, independent of the SPDIF enable bit (MX2A.2). Please contact with Avance for detail description about S/PDIF output function.

† If VRA = 0, ALC201/ALC201A AD/DA operate at fixed 48KHz sampling rate. Otherwise, it operates with variable sampling rate defined in MX2C and MX32. VRA also controls write operation of MX2Cand MX32.

6.22 MX2C PCM Front Output Sampling Rate Default: BB80H

The ALC201/ALC201A allows adjustment of the front output sample rate. This register is used to adjust the sample rate. By changing the values, sampling rates from 8000 to 48000 can be chosen.

Bit	Type	Function
15:0	R/W	**FOSR** [15:0] Output sampling rate (in 100Hz resolution)

❶ The ALC201/ALC201A supports the following sampling rates required in PC99 design guide.

Sampling rate	FOSR[15:0]
8000	1F40h
11025	2B11h
12000	2EE0
16000	3E80h
22050	5622h
24000	5DC0
32000	7D00h
44100	AC44h
48000	BB80h

❷ Note that If the value written is not support, the closest value is returned (higher in case of a tie).

❸ When MX2A.0=0 (VRA is disabled), this register will return BB80h when read.

6.23 MX32 PCM Input Sampling Rate
Default: BB80H

The ALC201/ALC201A allows adjustment of the PCM input sample rate. This register is used to adjust the sample rate. By changing the values, sampling rates from 8000 to 48000 can be chosen.

Bit	Type	Function
15:0	R/W	**ISR** [15:0] Output sampling rate (in 100Hz resolution)

❶ The ALC201/ALC201A supports the following sampling rates required in PC99 design guide.

Sampling rate	ISR[15:0]
8000	1F40h
11025	2B11h
12000	2EE0
16000	3E80h
22050	5622h
24000	5DC0
32000	7D00h
44100	AC44h
48000	BB80h

❷ Note that If the value written is not support, the closest value is returned (higher in case of a tie).

❸ It also is write-protected by VRA.

6.24 MX3A S/PDIF Channel Status and Control Default: 2000H

Bit	Type	Function
15	R/W	**Validity Control** (control V bit in Sub-Frame) 0: the V bit (valid flag) in sub-frame depends on whether the S/PDIF data is under-run or over-run. 1: the V bit in sub-frame is always send as 1 to indicate the invalid data is not suitable for receiver.
14	R	**DRS** (Double Rate S/PDIF) Double rate SPDIF is not supported.
13:12	R/W	**SPSR** [1:0] (S/PDIF Sample Rate) 00: sample rate set to 44.1KHz, Fs[**0:3**]=0000 01: reserved 10: sample rate set to 48.0KHz, Fs[**0:3**]=0100 (default) 11: sample rate set to 32.0KHz, Fs[**0:3**]=1100
11	R/W	**LEVEL** (Generation Level)
10:4	R/W	**CC** [6:0] (Category Code)
3	R/W	**PRE** (Preemphasis) 0: None 1: filter preemphasis is 50/15 usec
2	R/W	**COPY** (Copyright) 0: Not asserted 1: Asserted
1	R/W	/**AUDIO** (Non-Audio Data type) 0: PCM data 1: AC3 or other digital non-audio data
0	R	**PRO** (Professional or Consumer format) 0: consumer format 1: professional format ALC201/ALC201A support consumer channel status format, this bit is always 0.

6.25 MX7C Vendor ID1 Default: 414CH

The two registers (MX7C Vendor ID1 and MX7E Vendor ID2) contain four 8-bit ID codes. The first three codes have been assigned by Microsoft for Plug and Play definitions. The fourth code is a Realtek assigned code identifying the ALC210/ALC210A. The MX7C Vendor ID1 register contains the value 414Ch, which is the first and second characters of the Microsoft ID code. The MX7C Vendor ID2 register contains the value 4720h, which is the third of the Microsoft ID code.

Bit	Type	Function
15:0	R	**Vendor ID** "AL"

6.26 MX7E Vendor ID2 Default: 4710H

Bit	Type	Function
15:8	R	**Vendor ID** "G"
7:0	R	Read as 10h (Avance CODEC: ALC201/ALC201A)

7. Electrical Characteristics

7.1 DC Characteristics

7.1.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Typical	Max	Units
Power Supplies Digital Analog	 DVdd AVdd	 3.0 4.5	 3.3 5.0	 3.6 5.5	 V V
Operating Ambient Temperature	Ta	0	-	+70	^{o}C
Storage Temperature	Ts			+125	^{o}C
ESD (Electrostatic Discharge)					
	Susceptibility Voltage				
Pin-38 (AVdd2)	4000V				
Others	Over 5000V				

7.1.2 Threshold Hold Voltage

Dvdd= 3.3V±5%, $T_{ambient}$=25^{0}C, with 50pF external load.

Parameter	Symbol	Min	Typical (Dvdd=3.3v)	Max	Units
Input voltage range	V_{in}	-0.30	-	Dvdd+0.30	V
Low level input voltage **(SYNC,SDATA_OUT,RESET#)**	V_{IL}	-	0.7	0.35Dvdd	V
Low level input voltage **(XTAL_IN,BIT_CLK)**	V_{IL}	-	1.0	0.35Dvdd	V
Low level input voltage **(ID1#,ID0#)**	V_{IL}	-	1.2	0.35Dvdd	V
High level input voltage **(SYNC,SDATA_OUT,RESET#)**	V_{IH}	0.4DVdd	1.7	-	V
High level input voltage **(XTAL_IN,BIT_CLK)**	V_{IH}	0.4DVdd	2.2	-	V
High level input voltage **(ID1#,ID0#)**	V_{IH}	0.4DVdd	1.7	-	V
High level output voltage	V_{OH}	0.9DVdd		-	V
Low level output voltage	V_{OL}	-	-	0.1DVdd	V
Input leakage current	-	-10	-	10	uA
Output leakage current (Hi-Z)	-	-10	-	10	uA
Output buffer drive current	-	-	5	-	mA
Internal pull up resistance	-	50k	100k	200k	Ohm

7.1.3 Digital Filter Characteristics

Filter	Symbol	Min	Typical	Max	Units
ADC Lowpass Filter	Passband	0	-	19.2	KHz
	Stopband	28.8			KHz
	Stopband Rejection		-76.0		dB
	Passband Frequency Response		+- 0.15		dB
DAC Lowpass Filter	Passband	0	-	19.2	KHz
	Stopband	28.8			KHz
	Stopband Rejection		-78.5		dB
	Passband Frequency Response		+- 0.15		dB

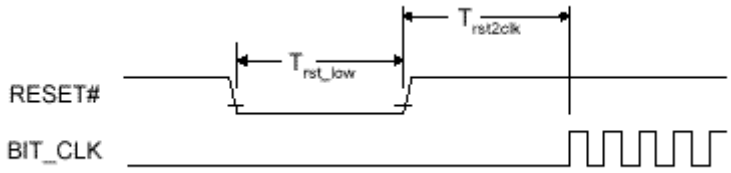
7.1.4 S/PDIF Output Characteristics

Dvdd= 3.3V, $T_{ambient}$=25^{0}C, with 75 ohm external load.

Parameter	Symbol	Min	Typical	Max	Units
High level output voltage	V_{OH}	3.0	3.3		V
Low level output voltage	V_{OL}	-	0	0.5	V

7.2 AC Timing Characteristics

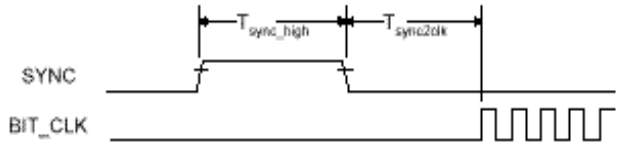
7.2.1 Cold Reset



Cold reset timing diagram

Parameter	Symbol	Min	Typical	Max	Units
RESET# active low pulse width	T_{rst_low}	1.0	-	-	us
RESET# inactive to BIT_CLK Startup delay	$T_{rst2clk}$	162.8	-	-	ns

7.2.2 Warm Reset



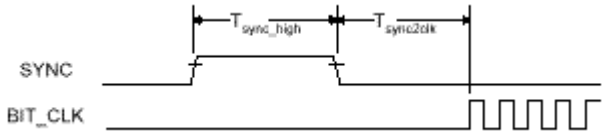
Warm reset timing diagram

Parameter	Symbol	Min	Typical	Max	Units
SYNC active high pulse width	T_{sync_high}	1.0	-	-	us
SYNC inactive to BIT_CLK Startup delay	$T_{sync2clk}$	162.8	-	-	ns

7.2.3 AC-Link Clocks

The ALC201/ALC201A derives its clock internally from an externally connected 24.576MHz crystal or an oscillator through the XTAL_IN pin. Synchronization with the AC'97 controller is achieved through the BIT_CLK pin at 12.288MHz (half of crystal frequency.

The beginning of all audio sample packets, or "Audio Frames," transferred over AC-Link is synchronized to the rising edge of the "SYNC" signal driven by the AC'97 controller. Data is transitioned on AC-Link on every rising edge of BIT_CLK, and subsequently sampled by the receiving side on each immediately following falling edge of BIT_CLK.



BIT_CLK and SYNC timing diagram

Parameter	Symbol	Min	Typical	Max	Units
BIT_CLK frequency		-	12.288	-	MHz
BIT_CLK period	T_{clk_period}	-	81.4	-	ns
BIT_CLK output jitter		-	-	750	ps
BIT_CLK high pulse width (note 2)	T_{clk_high}	36	40.7	45	ns
BIT_CLK low pulse width (note 2)	T_{clk_low}	36	40.7	45	ns
SYNC frequency		-	48.0	-	KHz
SYNC period	T_{sync_period}	-	20.8	-	us
SYNC high pulse width	T_{sync_high}	-	1.3	-	us
SYNC low pulse width	T_{sync_low}	-	19.5	-	us
Note 1: 47.5~70pF **********					
Note 2: Worse case duty cycle restricted to 45/55.					

7.2.4 Data Output and Input Times

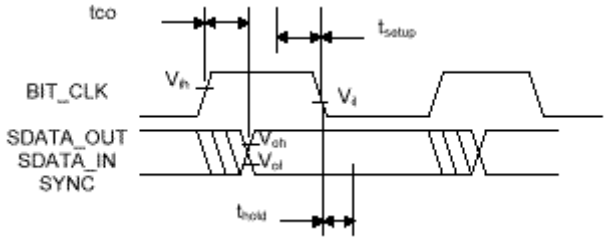


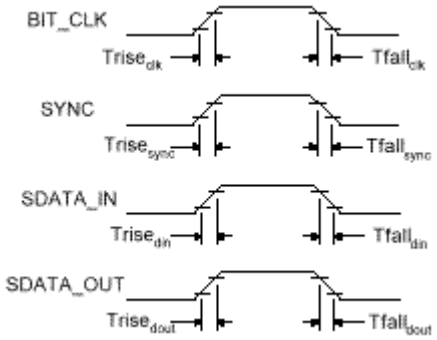
Fig 6.2.4-1 Data Output and Input timing diagram

Parameter	Symbol	Min	Typical	Max	Units
Output Valid Delay from rising edge of BIT_CLK	t_{co}	-	-	15	ns
Note 1: Timing is for SDATA and SYNC outputs with respect to BIT_CLK *at the device driving the output.*					
Note 2: 50pF external load					

Parameter	Symbol	Min	Typical	Max	Units
Input Setup to falling edge of BIT_CLK	t_{setup}	10	-	-	ns
Input Hold from falling edge of BIT_CLK	t_{hold}	10	-	-	ns
Note: Timing is for SDATA and SYNC outputs with respect to BIT_CLK *at the device driving the output.*					

Parameter	Symbol	Min	Typical	Max	Units
BIT_CLK combined rise or fall plus flight time		-	-	7	ns
SDATA combined rise or fall plus flight time		-	-	7	ns
Note: Combined rise or fall plus flight times are provided for worst case scenario modeling purpose.					

7.2.5 Signal Rise and Fall Times

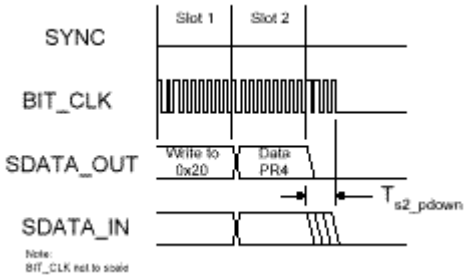


Signal Rise and Fall timing diagram

Parameter	Symbol	Min	Typical	Max	Units
BIT_CLK rise time	$Trise_{clk}$	-	-	6	ns
BIT_CLK fall time	$Tfall_{clk}$	-	-	6	ns
SYNC rise time	$Trise_{sync}$	-	-	6	ns
SYNC fall time	$Tfall_{sync}$	-	-	6	ns
SDATA_IN rise time	$Trise_{din}$	-	-	6	ns
SDATA_IN fall time	$Tfall_{din}$	-	-	6	ns
SDATA_OUT rise time	$Trise_{dout}$	-	-	6	ns
SDATA_OUT fall time	$Tfall_{dout}$	-	-	6	ns
Note 1: 75pF external load (50 pF in AC'97 rev2.1) Note 2: rise is from 10% to 90% of Vdd (V_{ol} to V_{oh}) Note 3: fall is from 90% to 10% of Vdd (V_{oh} to V_{ol})					

7.2.6 AC-Link Low Power Mode Timing

The ALC201/ALC201A AC-Link can be placed into low power mode by programming register 12h. Both BIT_CLK and SDATA_IN will be brought to and held at a logic low voltage level. The AC'97 controller can wake up the ALC201/ALC201A by providing the proper reset signals.

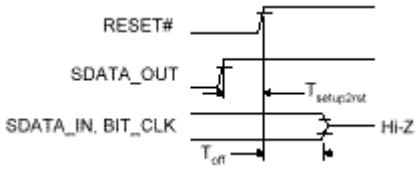


AC-Link low power mode timing diagram

Parameter	Symbol	Min	Typical	Max	Units
End of slot 2 to BIT_CLK, SDATA_IN low	T_{s2_pdown}	-	-	1.0	Us

BIT_CLK and SDATA_IN are transitioned low immediately (within the maximum specified time) following the decode of the write to the Powerdown register (12h) with PR4. When the AC'97 controller driver is at the point where it is ready to program the AC-Link into its low power mode, slots 1 and 2 are assumed to be the only valid stream in the audio output frame after all audio sources have been neutralized. The AC'97 controller should also drive SYNC and SDATA_OUT low after changing the ALC201/ALC201A to low power mode.

7.2.7 ATE Test Mode



ATE test mode timing diagram

****To meet AC'97 rev2.2, there are EAPD, SPDIFO, BIT_CLK and SDATA_IN should be floating in test mode.***

Parameter	Symbol	Min	Typical	Max	Units
Setup to trailing edge of RESET# (also applies to SYNC)	$T_{setup2rst}$	15.0	-	-	ns
Rising edge of RESET# to Hi-Z delay	T_{off}	-	-	25.0	ns

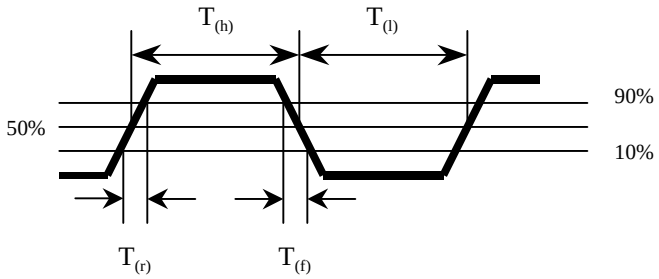
7.2.8 AC-Link IO Pin Capacitance and Loading

Output Pin	1 CODEC	2 CODEC	3 CODEC	4 CODEC
BIT_CLK (must support ≥ 2 CODECs)	55pF	62.5pF	75pF	85pF
SDATA_IN	47.5pF	55pF	60pF	62.5pF

7.2.9 SPDIF Output

SPDIF_OUT	Min	Typical	Max	Unit
Rise time/fall time	0		10	%
Duty cycle	45		55	%

Note:



Rise time = 100 * $T_{(r)}$/ ($T_{(l)}$+ $T_{(h)}$)%
Fall time = 100 * $T_{(f)}$/ ($T_{(l)}$+ $T_{(h)}$)%
Duty cycle = 100 * $T_{(h)}$/ ($T_{(l)}$+ $T_{(h)}$)%

7.2.10 BIT-CLK and SDATA-IN State

When RESET# is active, BIT-CLK and SDATA-IN must be floating. The ac-link signals are driven by another AC'97 on a CNR board. This requirement is not mentioned in the AC'97 specifications Rev 2.2. Please refer to CNR (Communication Network Riser) specifications Rev.1.0 pages 23~25 or AC'97 Rev.2.2 for detailed information.

8. Analog Performance Characteristics

Standard test condition: $T_{ambient}=25^0C$, Dvdd=3.3V ±5%,Avdd=5.0V±5%
1KHz input sine wave; Sampling frequency=48KHz; 0dB=1Vrms
10KΩ/50pF load; Test bench Characterization BW: 10Hz~22KHz
0dB attenuation; tone and 3D disabled

Parameter	Min	Typical	Max	Units
Full scale input voltage				
Line inputs (Mixers)	-	1.6	-	Vrms
Line inputs (A/D)	-	1.2	-	
Mic input (0 dB)	-	1.6	-	
Mic input (20 dB boost)	-	0.16	-	
Full scale output voltage				
LINE-OUT (ALC201/ALC201A)	-	1.1 / 1.7	-	Vrms
HEADPHONE-OUT (ALC201)	-	1.7	-	Vrms
TRUE-LINE-OUT (ALC201A)	-	1.1	-	
Analog to Analog S/N				
CD to LINE_OUT	-	95	-	dB
Other to LINE_OUT	-	95	-	
Analog frequency response	16	-	22,000	Hz
S/N (A-weighted)				
D/A	-	90	-	dB
A/D	-	90	-	
Total Harmonic Distortion (A-weighted)				
D/A	-	-85	-	dB
A/D	-	-85	-	
D/A & A/D frequency response	20	-	19,200	Hz
Transition Band	19,200	-	28,800	Hz
Stop Band	28,800	-	∞	Hz
Stop Band Rejection	-75	-	-	dB
Out-of-Band Rejection	-	-65	-	dB
Group delay	-	-	1	ms
Power Supply Rejection	-	-65	-	dB
MIC Amplifier 20dB Gain	18	20	22	dB
Master Volume (Mono, Stereo): 32 step				
Step Size	-	1.5	-	dB
Attenuation Control Range	0	-	46.5	dB
PC Beep Volume: 16 step				
Step Size	-	3.0	-	dB
Attenuation Control Range	0	-	45	dB
Analog Mixer Volume: 32 step				
Step Size	-	1.5	-	dB
Gain Control Range	-34.5	-	+12	dB
Record Gain: 16 step				
Step Size	-	1.5	-	dB
Gain Control Range	0	-	+22.5	dB
Input impedance (gain = 0dB)				
PC BEEP only		32		KΩ
Others (PHONE,LINE,CD,AUX,VIDEO)		32		KΩ
MIC1, MIC2		16		KΩ
Output Impedance (LINE-OUT, ALC201)		200		Ω
Output Impedance (HP-OUT, ALC201)		10		Ω
Output Impedance (LINE-OUT, ALC201A)		10		Ω
Output Impedance(TRUE-OUT,ALC201A)		200		Ω

Power Supply Current VA=5.0v, VD=3.3v		 60 10	- 70	 mA mA
Power Down Current VA=5.0v VD=3.3v		 -	 500 1000	 uA uA
V_{refout}	-	2.50	-	V
V_{refout} Drive Current	-	8	-	mA

9. Design Suggestions

9.1 Clocking

The clock source for different configurations are listed below:

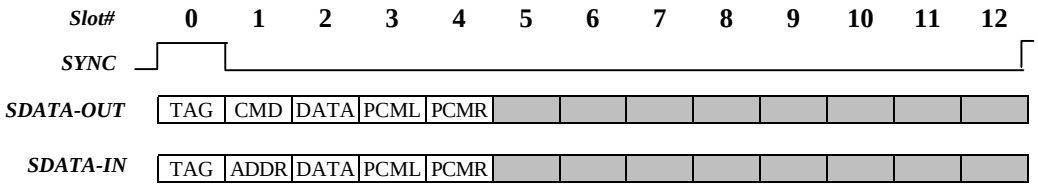
CODEC ID[1..0]	BIT-CLK	Clock source
00	Output	Crystal or external clock (XTAL-IN)
01	Input	external clock (XTAL-IN)
10	Input	external clock (XTAL-IN)
11	Input	external clock (XTAL-IN)

9.2 AC-Link

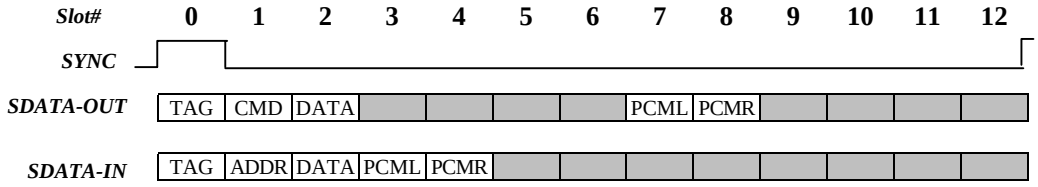
When the ALC201/ALC201A takes serial data from the AC97 controller, it samples **SDATA_OUT** on the falling edge of **BIT_CLK**. When the ALC201/ALC201A sends serial data to the AC97 controller, it starts to drive **SDATA_IN** on the rising edge of **BIT_CLK**.

The ALC201/ALC201A will return any uninstalled bits or registers with 0 for read operations. The ALC201/ALC201A also stuffs the unimplemented slot or bit with 0 in **SDATA-IN**. Note that AC-LINK is MSB-justified.

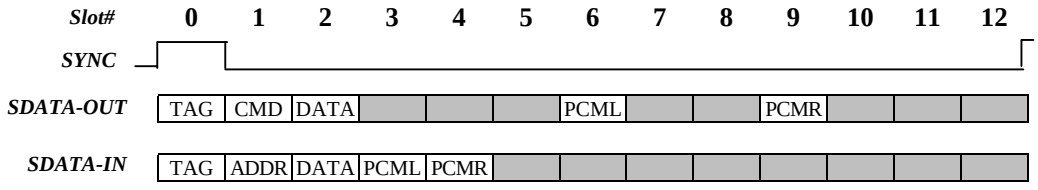
Refer to "Audio CODEC '97 Component Specification Revision 2.1/2.2" for details.



ALC201/ALC201A slot arrangement – CODEC ID = 00



ALC201/ALC201A slot arrangement – CODEC ID = 01, 10



ALC201/ALC201A slot arrangement – CODEC ID = 11

9.3 Reset

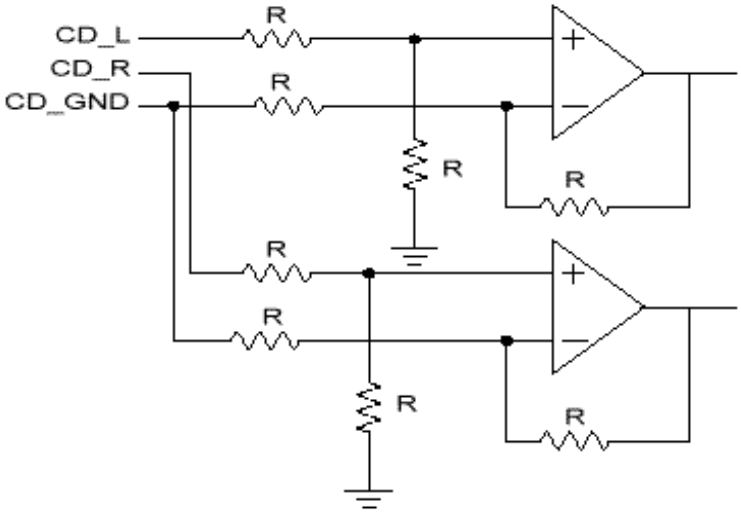
There are 3 kinds of reset operations: ***Cold***, ***Warm*** and ***Register***, which are listed below:

Reset Type	Trigger condition	CODEC response
Cold	Assert RESET# for a specified period	Reset all hardware logic and all registers to their default value.
Register	Write register indexed 00h	Reset all registers to its default value.
Warm	Driven SYNC high for specified period without BIT_CLK	Reactivates AC-LINK, no change to register values.

The AC97 controller should drive SYNC and SDATA-OUT low during the period of RESET# assertion to guarantee that the ALC201/ALC201A resets successfully.

9.4 CD Input

Differential CD input requires special attention. Below is an example of a differential CD input circuit.



Example of differential CD input

9.5 Odd Addressed Register Access

The ALC201/ALC201A will return “0000h” when the odd-addressed registers and unimplemented registers are read.

9.6 Power-down Mode

The power down control register (index 26h) requires special attention, especially PR4 (powerdown AC-link).

9.7 Test Mode

9.7.1 ATE In Circuit Test Mode

SDATA_OUT is sampled high at the trailing edge of RESET#. In this mode the ALC201/ALC201A will drive BIT_CLK, SDATA_IN, EAPD and SPDIFO to high impedance.

9.7.2 Vendor Specific Test Mode

SYNC is sampled high at the trailing edge of RESET#. At this mode ALC201/ALC201A will drive BIT_CLK, SDATA_IN, EAPD and SPDIFO to high impedance.

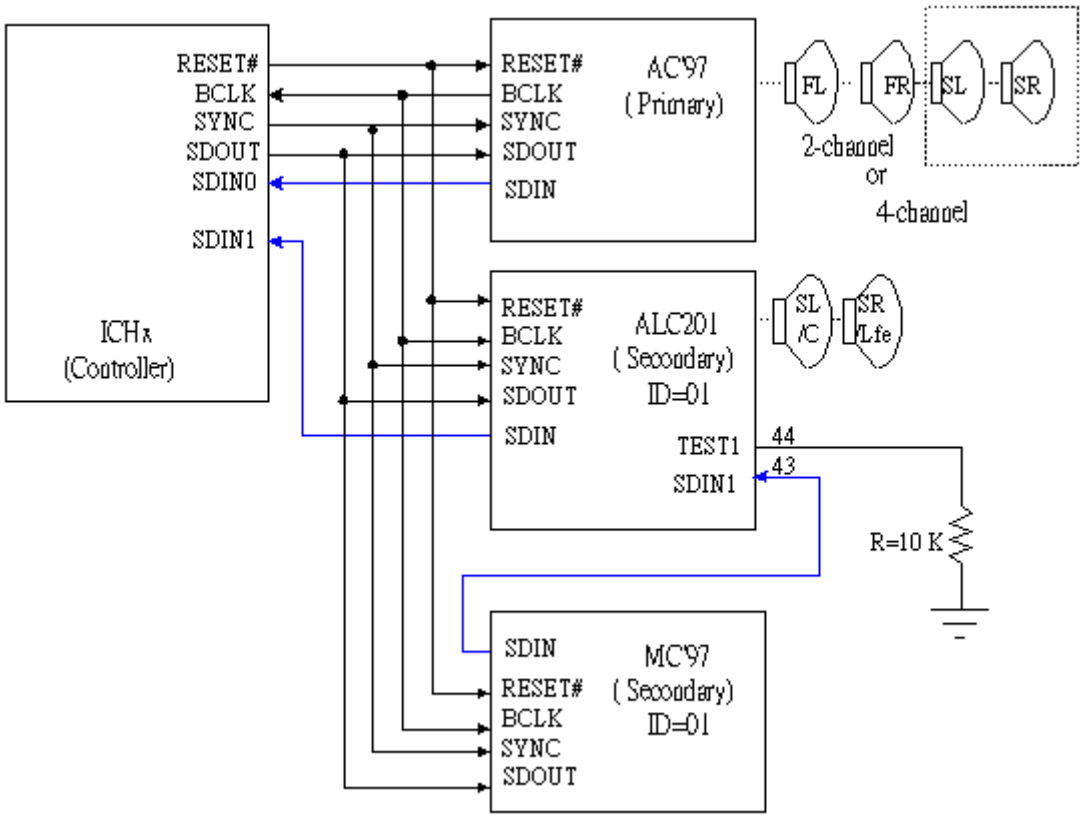
Note: To make the most compatibility with AC'97 rev2.2, ALC201/ALC201A will float its digital output pins in both ATE and Vendor-Specific test mode. Please refer to AC'97 rev2.2 section 9.2 for detail description about test mode.

9.8 Chain-In Function

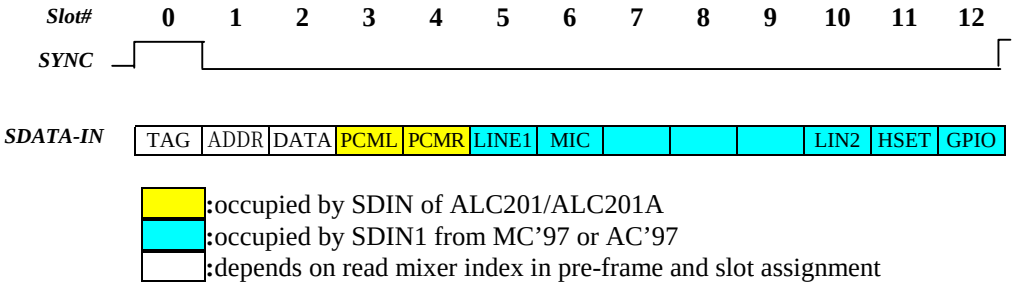
Only SDIN0 and SDIN1 are supported by Intel's ICHx. It is impossible to implement 2 AC'97 and 1 MC'97 simultaneously. To achieve a 5.1 channel application by connecting one 4-channel AC'97 and an ALC201/ALC201A. The ALC201/ALC201A supports a function called "Chain-In," which shares SDIN1 by the ALC201/ALC201A and MC'97.

When the ALC201/ALC201A is identified as a secondary CODEC and latches the value of pin 44 (TEST1) low in power on internal reset duration, pin 43 (JD/SDIN1) is used as input SDIN from MC'97. Then the SDIN sent to ICHx is composed of the ALC201's SDIN and MC97's SDIN. (See figure below)

Configuration	Pin 43 Function
Secondary (ID[1:0]≠00) & (TEST1 is pull low in power on reset)	SDIN1from MC'97
Others	Jack-Detect

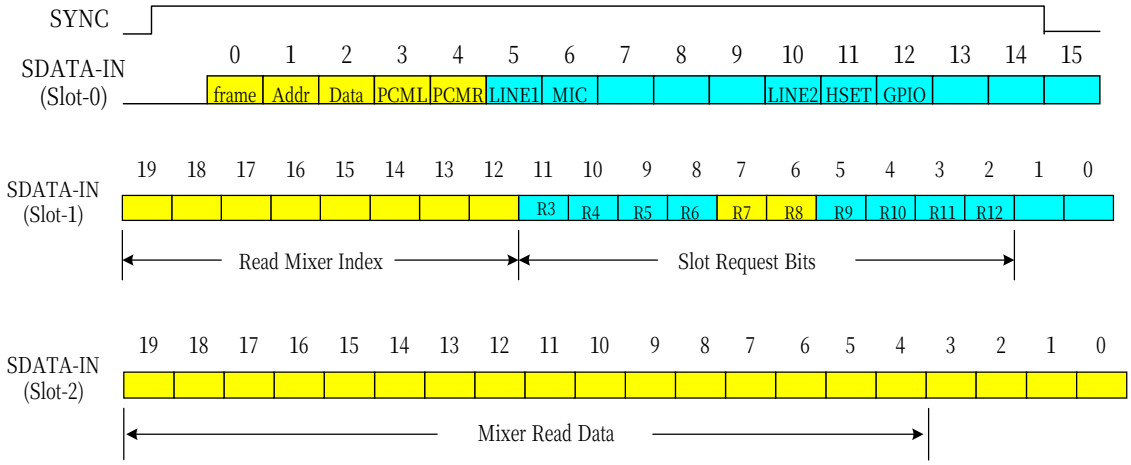


Chain-In Connection between ALC201/ALC201A and MC'97

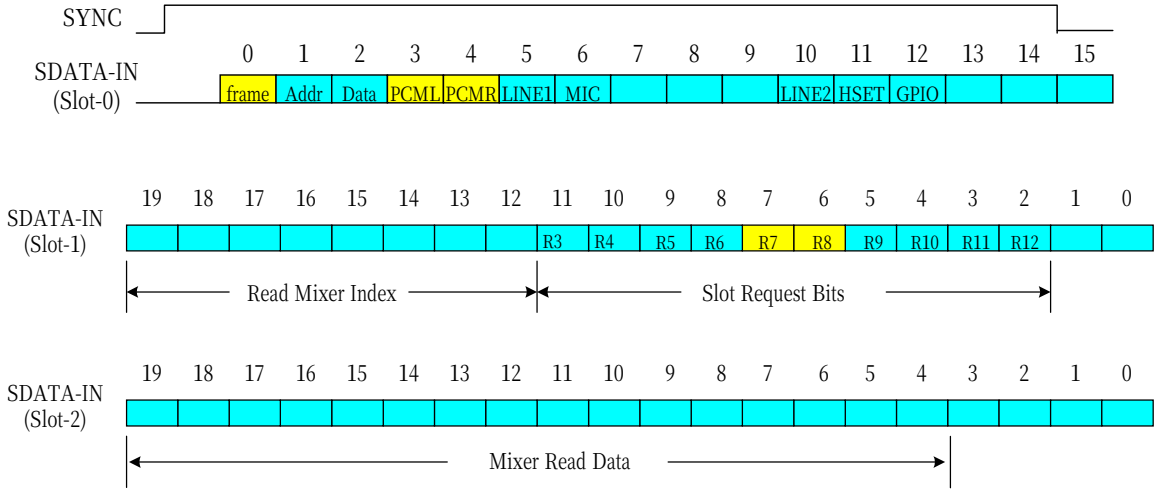


:occupied by SDIN of ALC201/ALC201A
:occupied by SDIN1 from MC'97 or AC'97
:depends on read mixer index in pre-frame and slot assignment

SDATA-IN slot is multiplex between ALC201/ALC201A and MC97



SDATA-IN slot-0, slot-1and slot-2 timing (controller command read MX00~MX3A in pre-frame; example: current DAC slot are set to slot 7/8)



SDATA-IN slot-0, slot-1and slot-2 timing (controller read Mixer except MX00~MX3A in pre-frame; example: current DAC slot are set to slot 7/8)

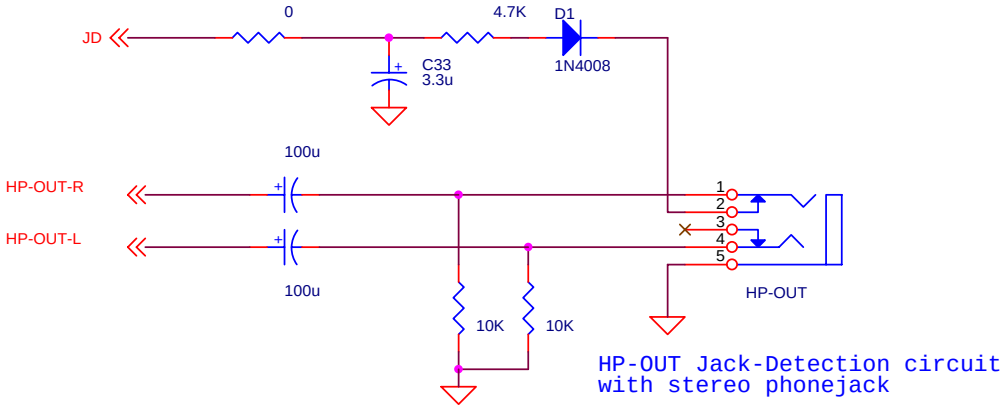
Note:
If AC-Link is off and system enters suspend (S1) or deep sleep mode (S3, S4), the MC'97 may issue a low-to-high edge at its SDIN when an external ring event is triggered. To achieve the wake-on modem function in Chain-In mode, output SDATA-IN must be auto switched to SDIN1 when AC-Link is off (PR4 in MX26 is set). According to CNR rev1.0, all logic on CNR board driven by AC-LINK signals must be powered by +Vdual (+Vaux). Only +Vdual is active in S3 and S4 mode, so we recommend to power the ALC201/ALC201A and MC'97 by +Vdual when the Chain-In function is implemented on a CNR board.

9.9 Jack-Detect Function

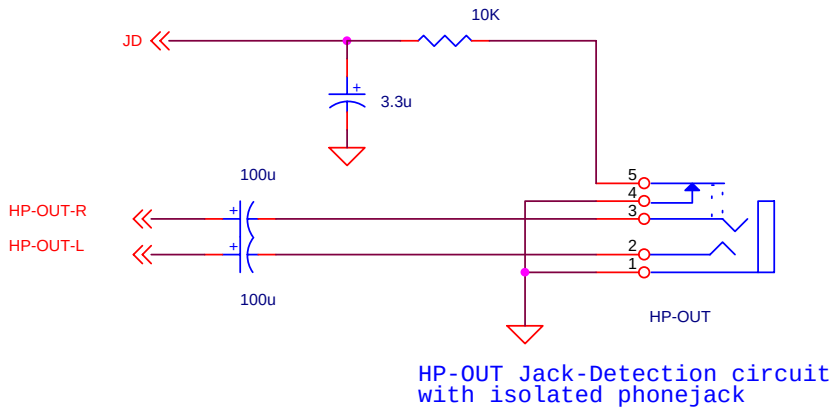
Pin-43, named 'JD (Jack-Detect),' is an internal pull high input pin used to decide whether or not LINE-OUT should be auto muted. If JDE (Jack Detect Enable) is set and when the ALC201/ALC201A detects that the JD is floating or pulled high (JDS=1), it will disable the analog output of LINE-OUT even if the MX02 is not muted.

The example- figure below shows an example to implement this function. When there is no audio plug inserted in HP-OUT jack, JD is detected as low, LINE output normal. If there is an audio plug inserted, the ALC201/ALC201A disables LINE output, still outputs to HP-OUT/TRUE-LINE-OUT and MONO-OUT. This is useful on some PC applications, especially in a notebook environment.

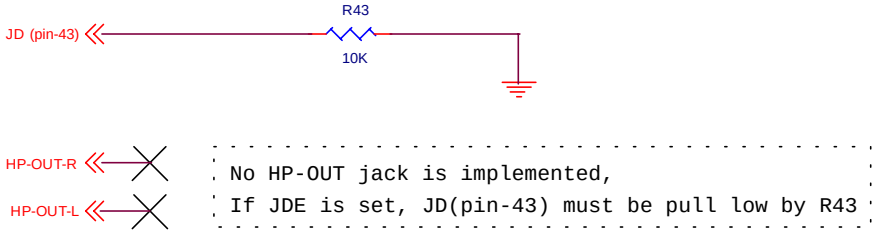
If the headphone output jack is not implemented and HP-OUT/TRUE-LINE-OUT is kept as floating, once JDE is enabled, LINE output will be muted unless JD is pulled low by a 10K ohm resistor (see the example-2 figure). To overcome this issue, the Jack-Detect mute LINE-OUT function is disabled after power up (default JDE is 0), which will make the ALC201/ALC201A compatible with other AC'97 products. So it is the responsibility of the software to enable this function if headphone jack detection is implemented.



Jack detect connection example-1



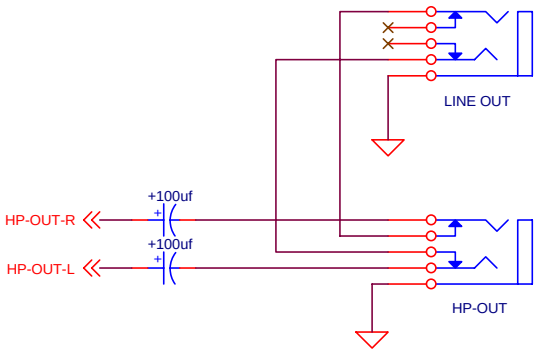
Jack detect connection example-2



JD is pull low by a 10K ohm resistor

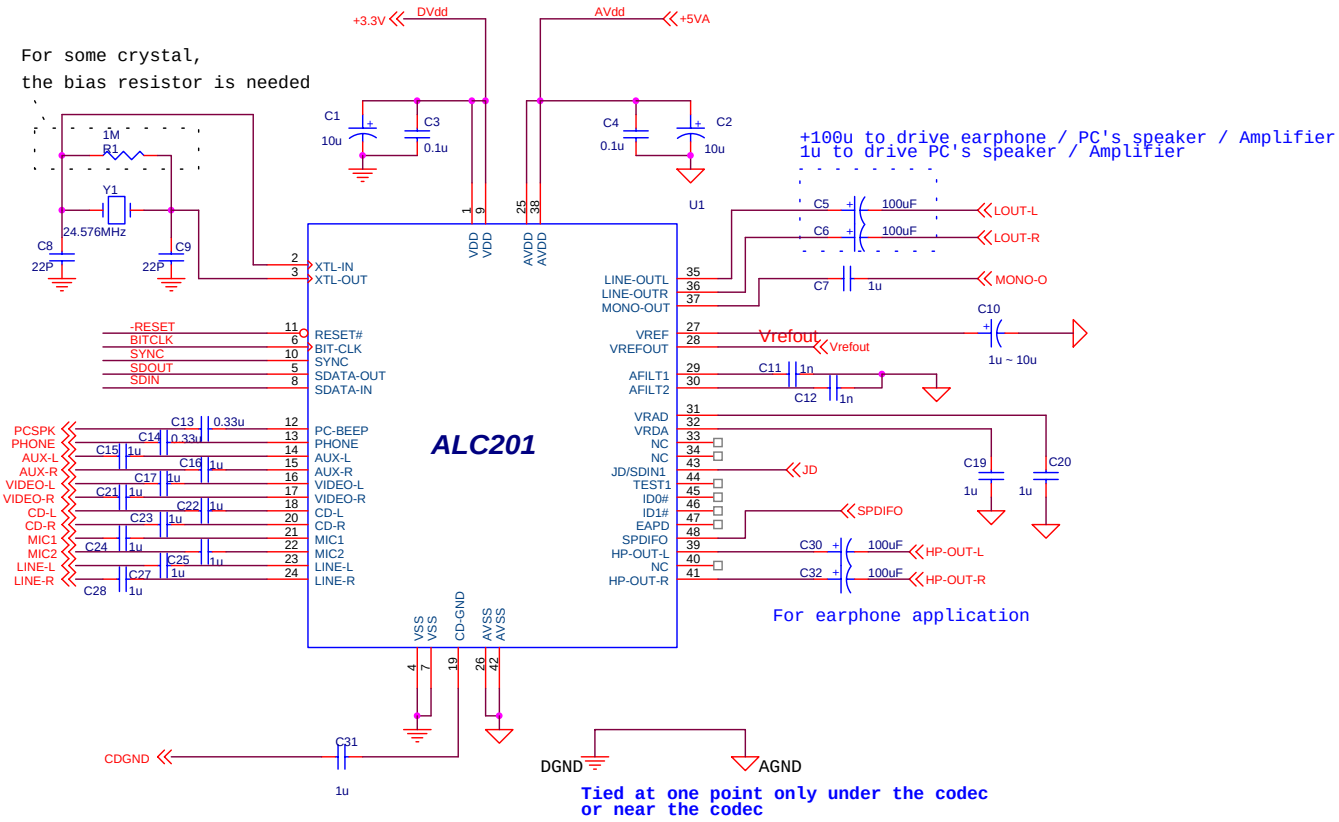
The figure below shows another simple way to implement the jack detect function without using the ALC201's JD pin. It is especially easy for motherboard design. No extra components are needed, only layout issues exist.

Once the HP-OUT jack is plugged in, output signals to LINE-OUT will be isolated, and no signals will be output at the LINE-OUT jack. The only drawback to this plan is that software will not sense the HP-OUT jack is plugged in. It may be not convenient for software to approach this special application.



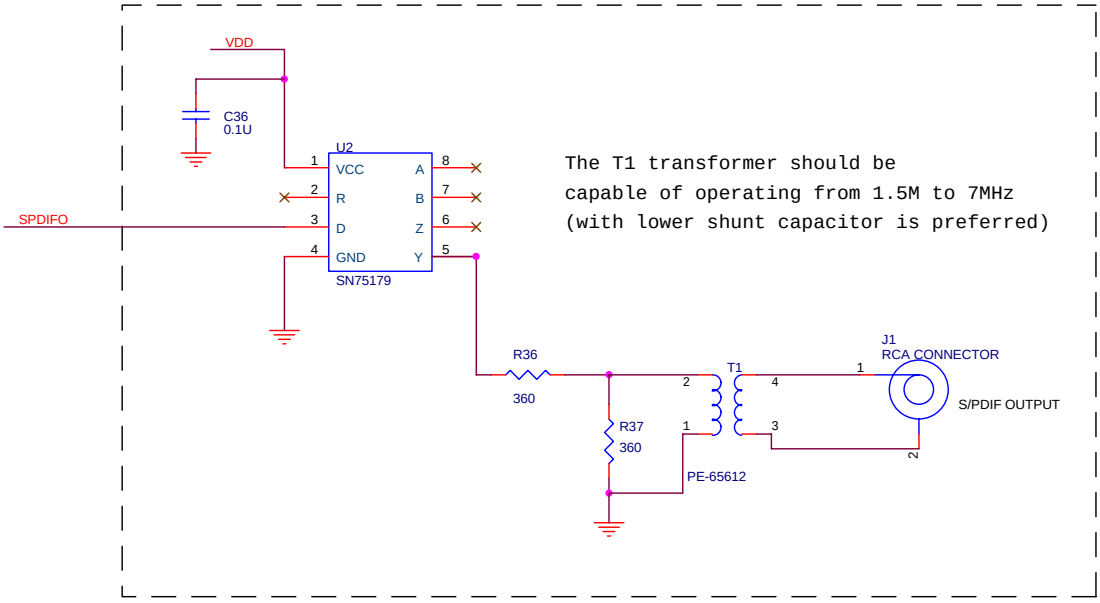
Implement Jack-Detect function without using ALC201's pin

10. Application Circuit

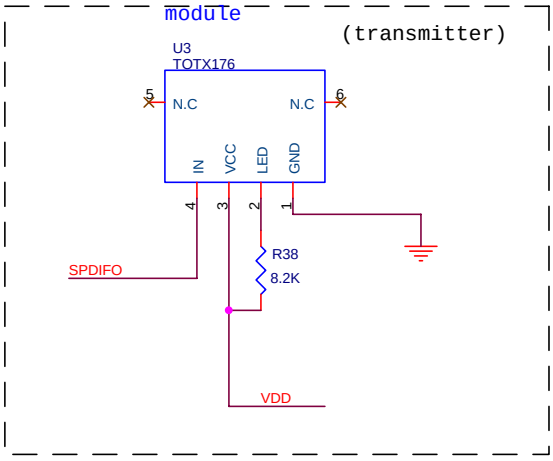


Filter Connection for ALC201

Option (I): S/PDIF signal use RCA connector
+ Line Driver/ Receiver (is suitable for long transmission line)

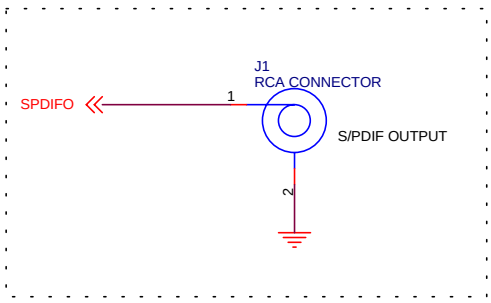


Option (II): S/PDIF signal use fiber optic transmitter and receiver module

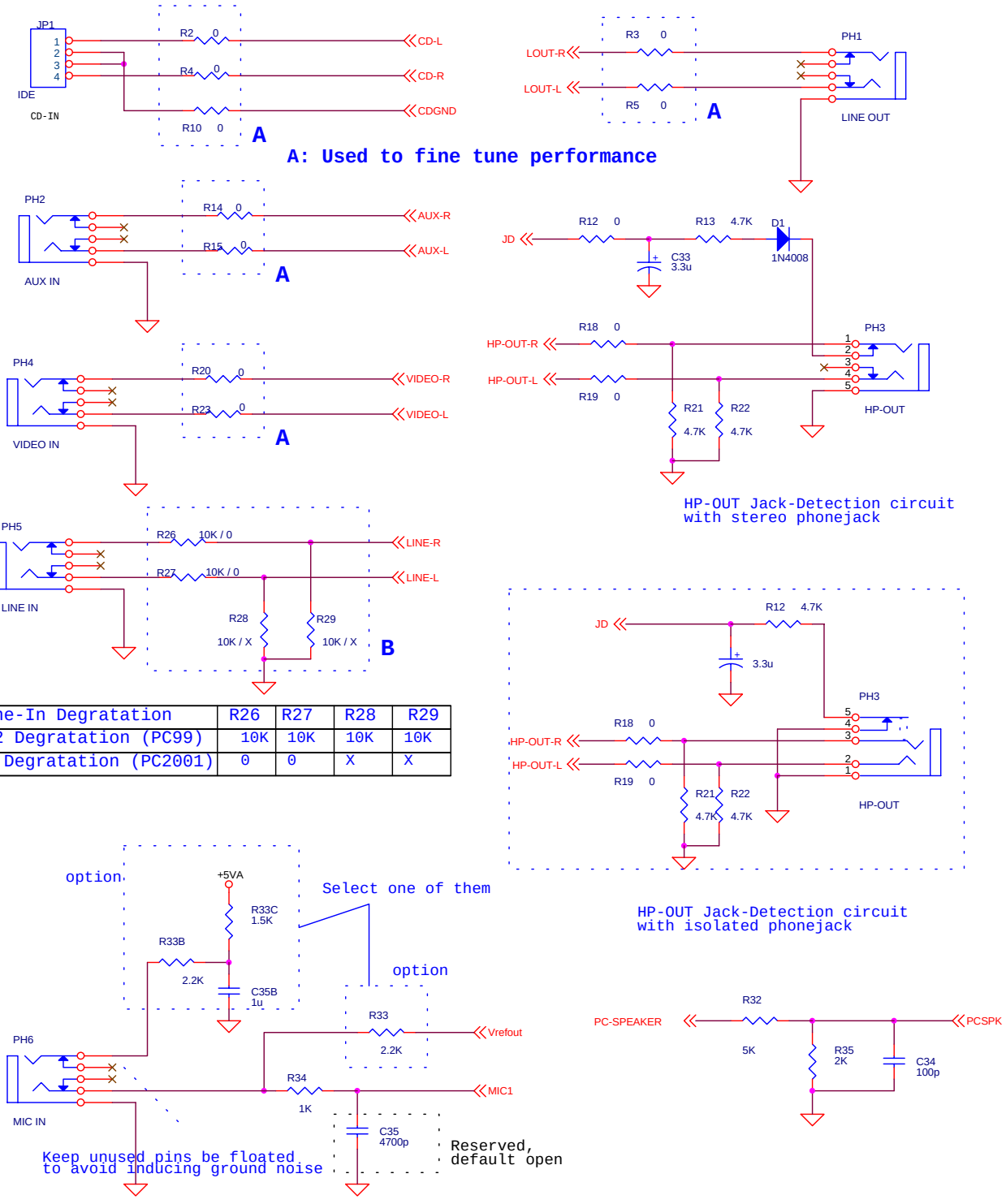


Option (III): Without Line Driver/ Receiver

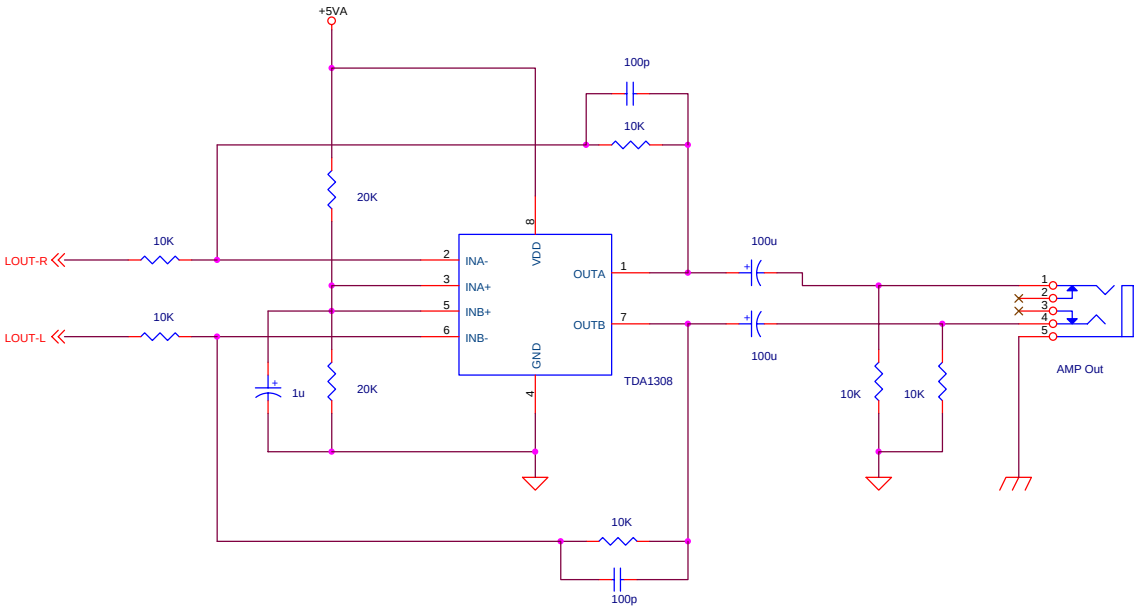
(Guaranteed transmission distance <= 7 feet)



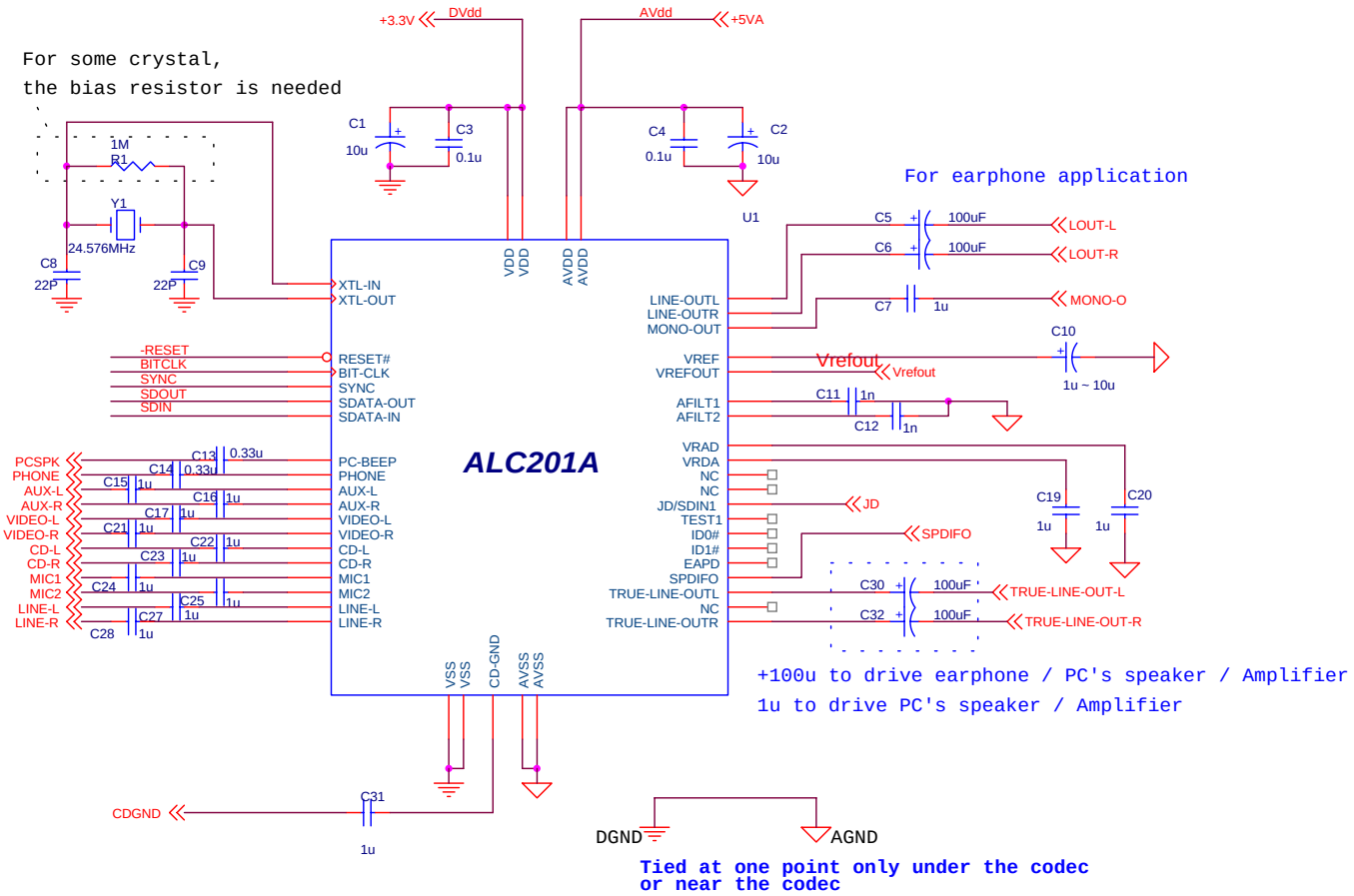
S/PDIF Out Connection Option (I /II /III are optional) for ALC201/ALC201A



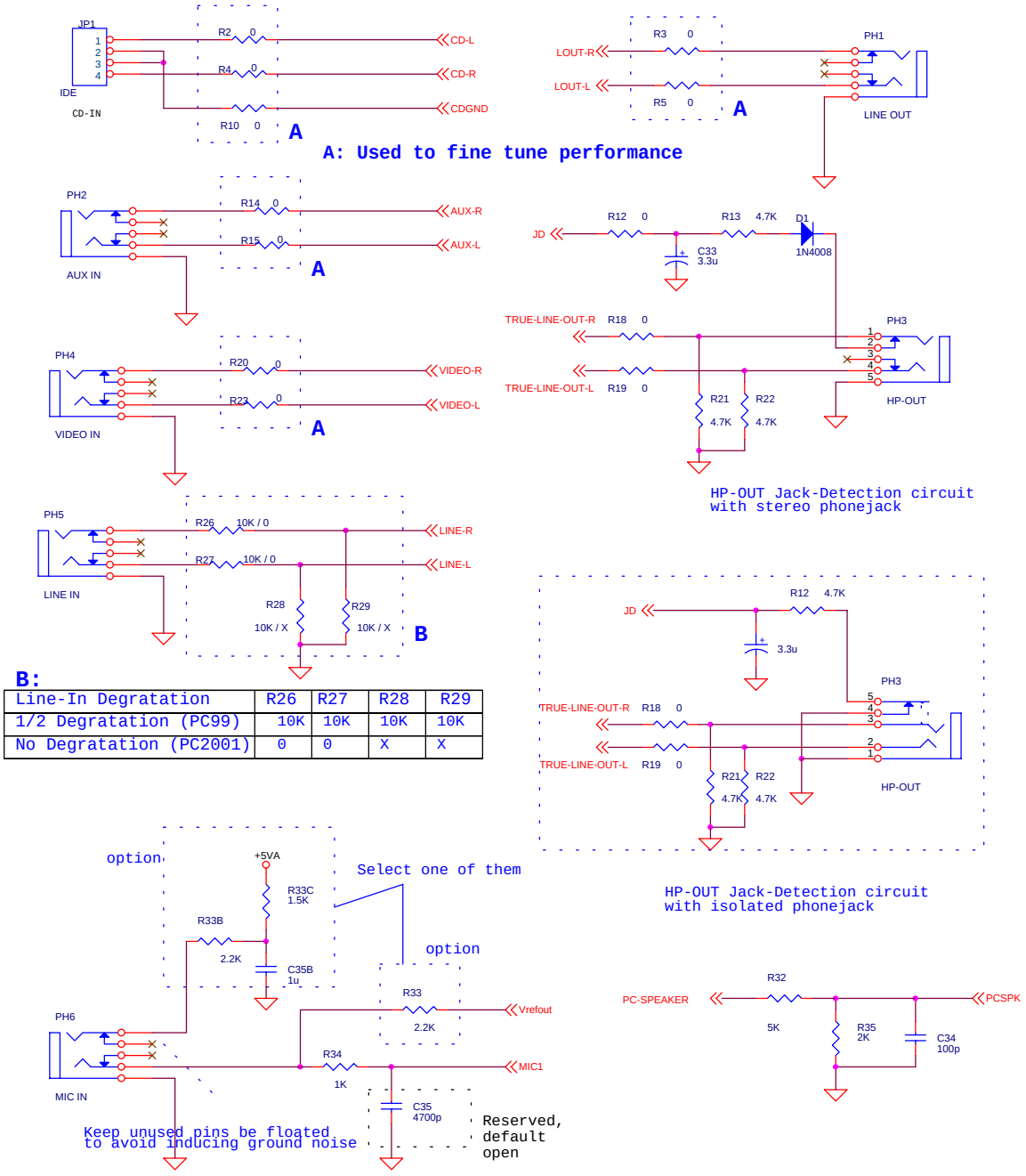
Input/Output Connection for ALC201



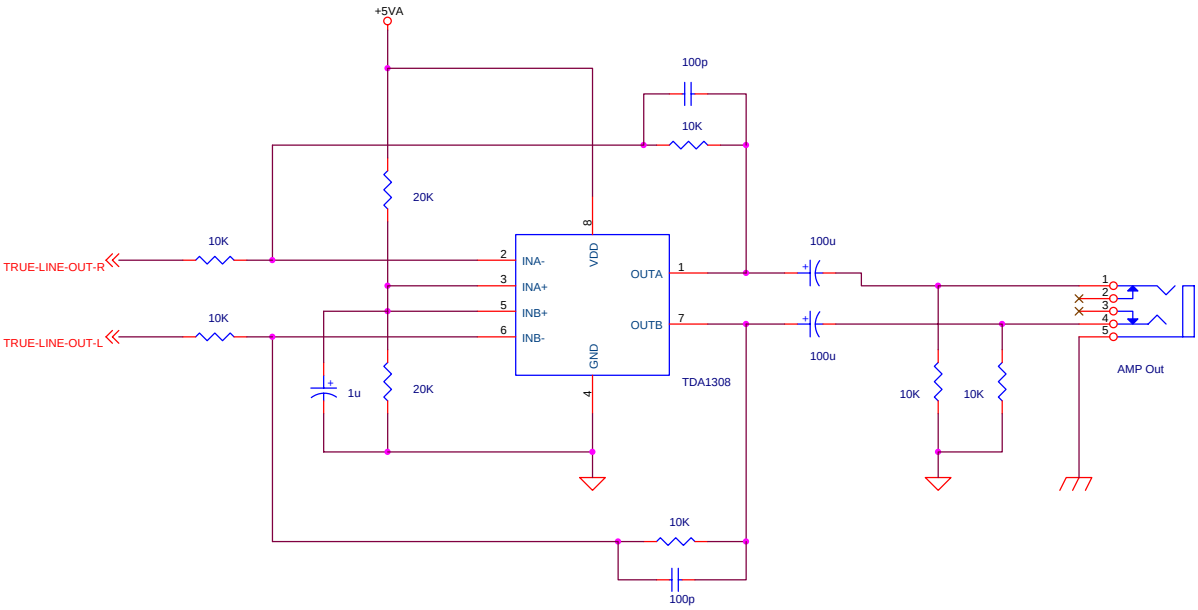
Amplifier Connection example for ALC201



Filter Connection for ALC201A

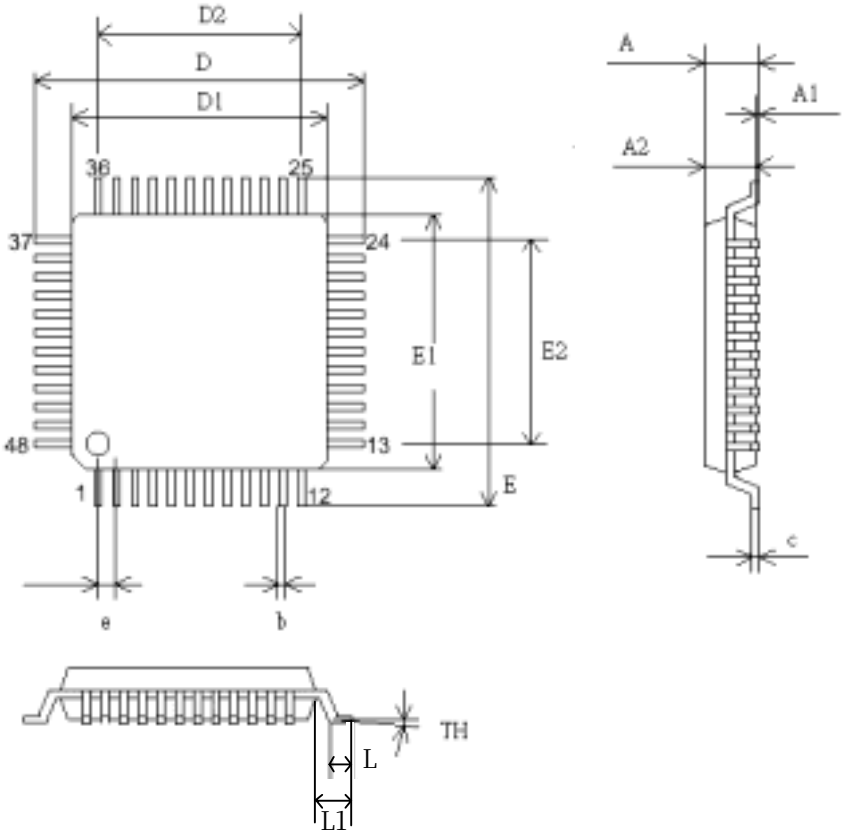


Input/Output Connection for ALC201A



Amplifier Connection example for ALC201A

11. Mechanical Dimensions



SYMBOL	MILLIMETER			INCH		
	MIN.	TYPICAL	MAX.	MIN.	TYPICAL	MAX
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
c	0.09		0.20	0.004		0.008
D	9.00 BSC			0.354 BSC		
D1	7.00 BSC			0.276 BSC		
D2	5.50			0.217		
E	9.00 BSC			0.354 BSC		
E1	7.00BSC			0.276 BSC		
E2	5.50			0.217		
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC			0.016 BSC		
TH	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.0236	0.030
L1		1.00			0.0393	

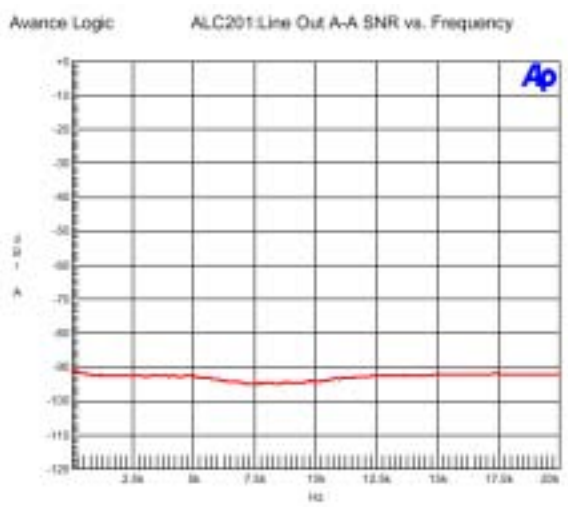
TITLE: LQFP-48 (7.0x7.0x1.6mm) PACKAGE OUTLINE DRAWING, FOOTPRINT 2.0mm		
LEADFRAME MATERIAL		
APPROVE	DOC. NO.	
	VERSION	02
CHECK	DWG NO.	PKGC-065
	DATE	
REALTEK SEMICONDUCTOR CORP.		

Appendix - I

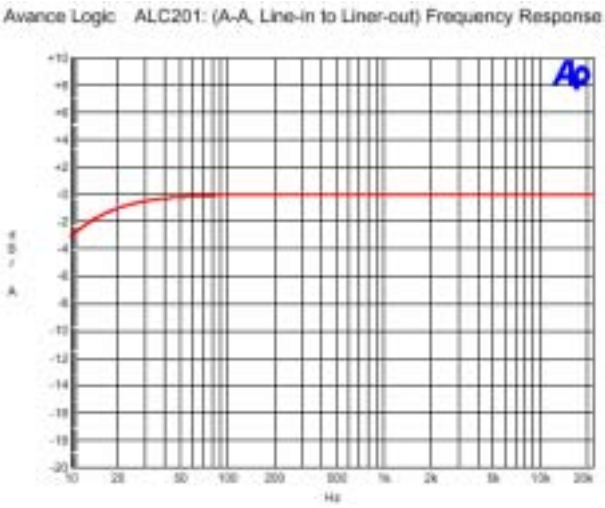
Performance Measured by Audio Precision System II

The following diagrams are analog performance measured by Audio-Precision system II. The methodology is according to WHQL PC99, as defined by Microsoft.

1. Analog Input to Analog Output (SNR spectrum, frequency response)

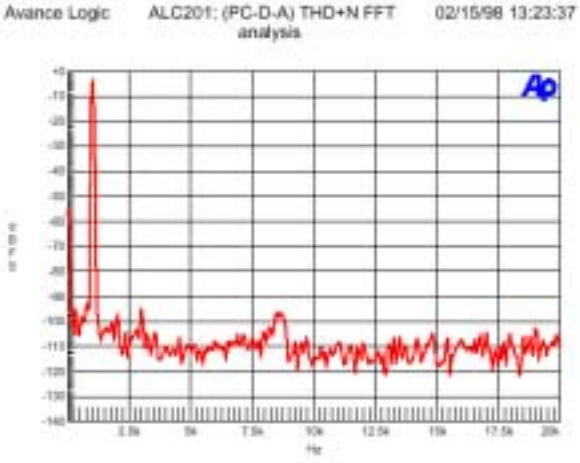


Mixer S/N Ratio vs. Frequency

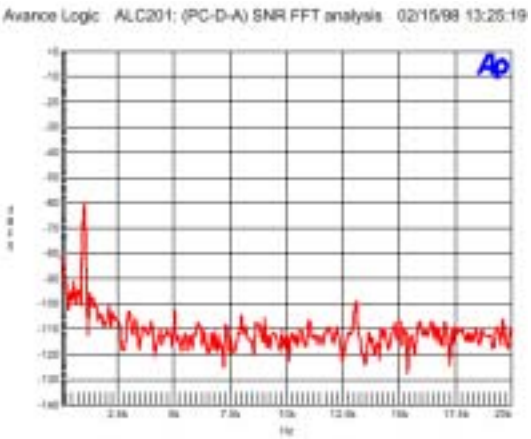


Mixer Frequency Response

2. Digital to Analog Output (DAC)

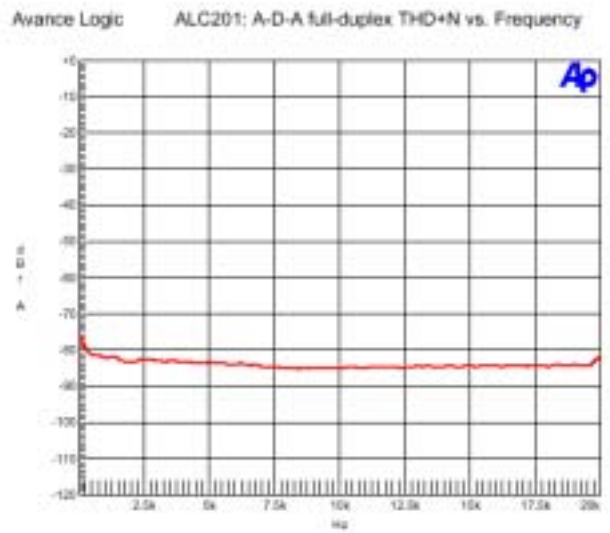


DAC THD+N Spectrum

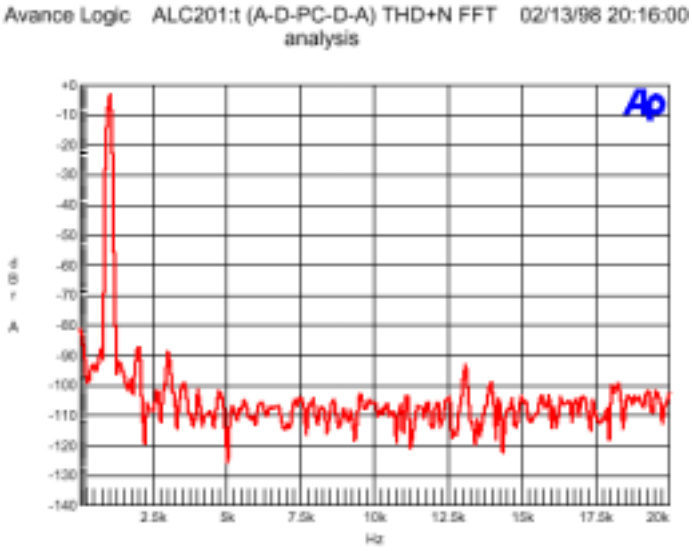


DAC S/N Ratio Spectrum

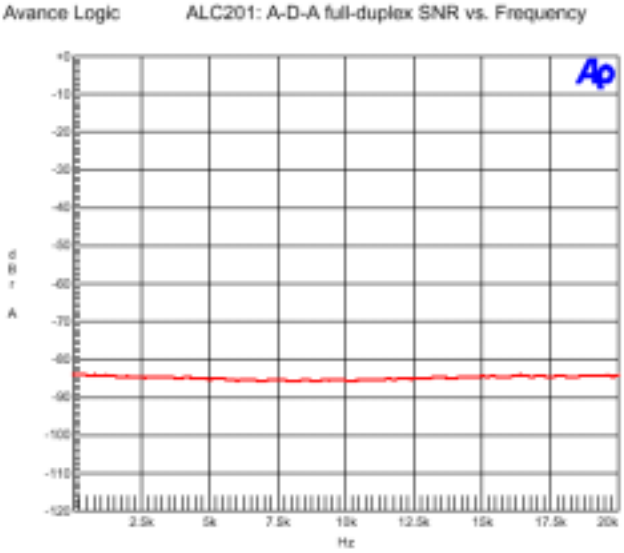
3. Analog Input to Digital (ADC)



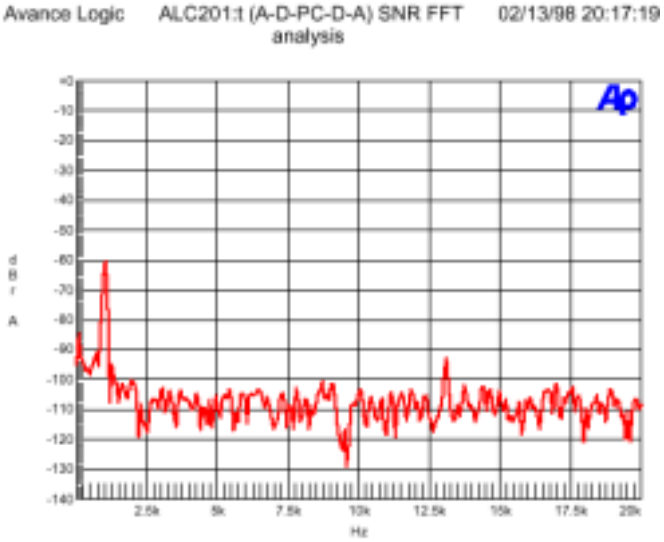
ADC-to-DAC THD+N vs. Frequency



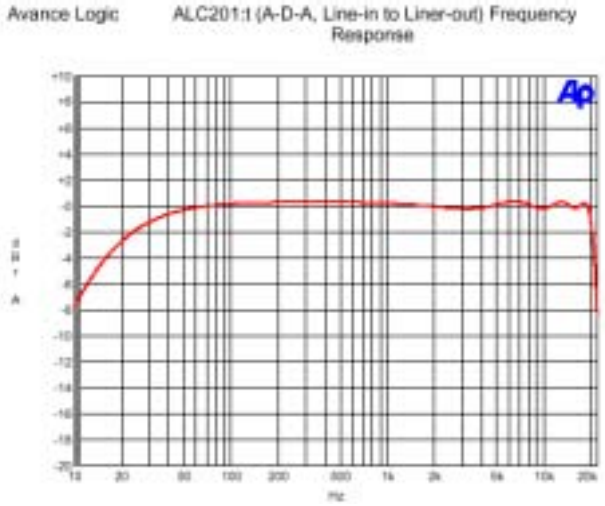
ADC-to-DAC THD+N Spectrum



ADC-to-DAC S/N Ratio vs. Frequency

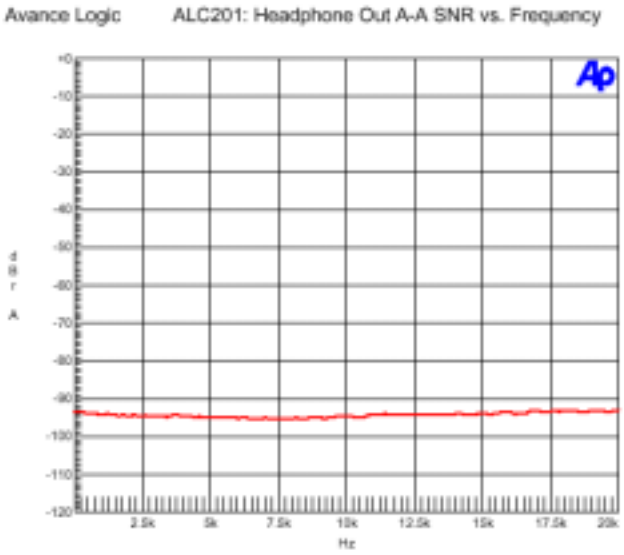


ADC-to-DAC S/N Ratio Spectrum

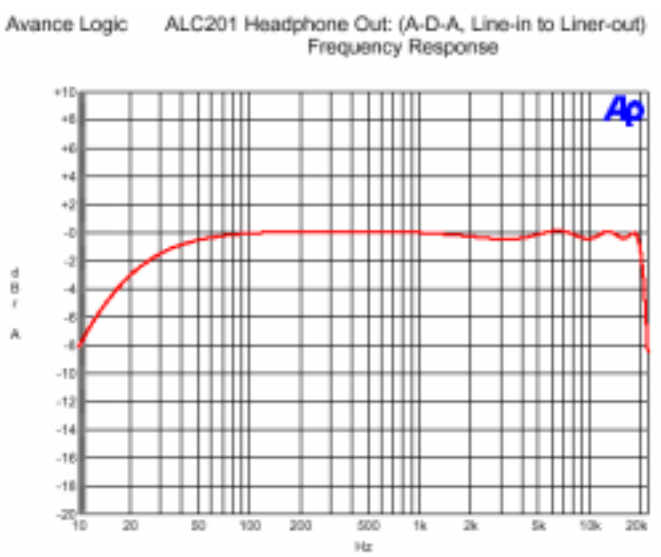


ADC-to-DAC Frequency Response

4. Head-Phone Out Performance



Head-Phone Out S/N Ratio vs. Frequency



Head-Phone Out Frequency Response

Appendix - II

PC2001 rev1.0 Audio Performance Requirements

Feature	*Measurement*	*PC2001*	*ALC201*
Full-scale input voltage	FSIV(A-D-PC) Line-In	≥1.0 Vrms	1.0~1.75Vrms
	FSIV(A-D-PC) Mic-In	≥100 mVrms	0.10~1.75Vrms
Full-scale output voltage	FSIV(D-A-PC) Line-Out	≥1.0 Vrms	1.0~1.50Vrms
Analog pass-through			
Line-In to Line-Out	FR (-3dB)		17 ~22 k
(A-A)	Dynamic range		95 dBFSA[1]
	THD+N		-92 dBFSA[1]
Mic-In to Line-Out	FR (-3dB		17 ~22 k
	Dynamic range		95 dBFSA[1]
	THD+N		-92 dBFSA[1]
Digital Playback	FR (-3dB)		
	44.1-kHz source	20 ~17.6 k	19 ~20 k
(PC-D-A) for Line-Out	48.0-kHz source	20 ~19.2 k	18 ~20.5 k
	Passband ripple[3]	≤+/-0.5dB	+/-0.2dB
	Dynamic range[2]	≥80 dBFSA[1]	90 dBFSA
	THD+N[2]	≤-65 dBFSA[1]	-85 dBFSA
Digital recording	FR (-3dB)		
	44.1-kHz source	20 ~17.6 k	19 ~20 k
(A-D-PC) for Line-In	48.0-kHz source	20 ~19.2 k	18 ~20.5 k
	Passband ripple[3]	≤+/-0.5dB	+/-0.2dB
	Dynamic range[2]	≥70 dBFSA[1]	90 dBFSA
	THD+N[2]	≤-60 dBFSA[1]	-85 dBFSA
Digital recording	FR (-3dB)		
	22.05-kHz source	100 ~8.8 k	50 ~10.5 k
(A-D-PC) for Mic-In	Passband ripple[3]	≤+/-0.5dB	+/-0.2dB
	Dynamic range[2]	≥70 dBFSA[1]	85 dBFSA
	THD+N[2]	≤-60 dBFSA[1]	-80 dBFSA
Line output cross-talk	Channel separation between		
	Left and right line out	≥60 dB	80 dB
Sampling frequency	Playback	0.1%	0.1%
accuracy	Record	0.1%	0.1%

*1: Decibels relative to full scale (FS), applied with the "A-weighting" filters.
*2: For mobile PC, measurements are relaxed by 10 dBFS
*3: Passband ripple measured from 40Hz to (0.4xFs)/2 Hz
*4: These performances are measured on motherboard environment.

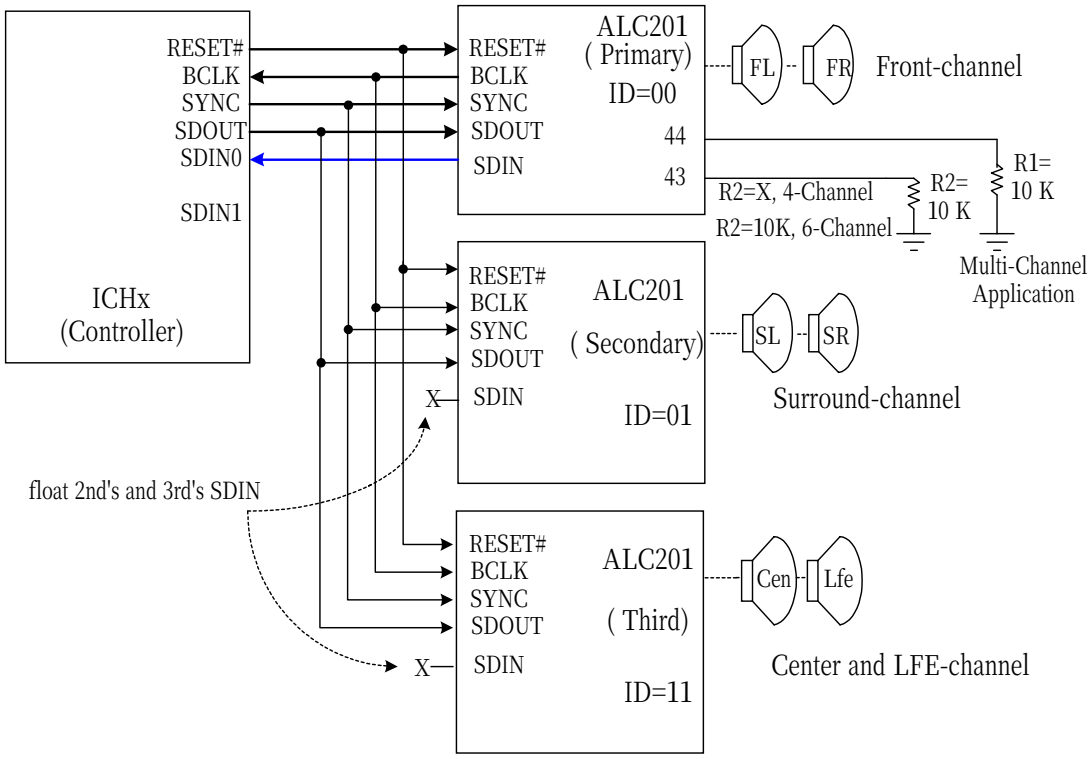
Appendix - III

Multi-Channel Implementation With Parallel ALC201 Devices

Only SDIN0 and SDIN1 are supported by Intel's ICHx. It is impossible to implement multiple AC'97 and MC'97 simultaneously. Two or Three ALC201 chips can be paralleled to achieve four or six channel applications instead of using the "Chain-In" function described earlier. Though it is also not difficult to implement multi-channel applications, there are some rules which should be followed to remain compatible with the Avance driver.

1. Only 48K sample rate is supported.
2. Jack-Detect function is forbidden with 4-6 channel applications.
3. Configuration must follow specifications in the table: (X: no pull low resistor)

	R1	R2	
2-Channel	X	--	Driver only supports 2 channel capability
4-Channel	10K	X	Driver enables 4 channel capability
6-Channel	10K	10K	Driver enables 6 channel capability



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