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-Preliminary-

AK4520A

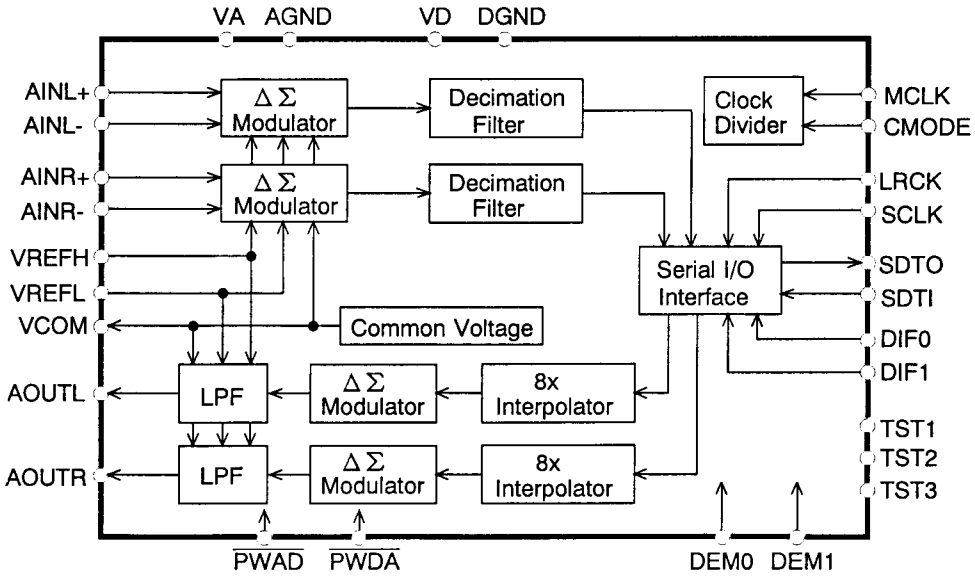
100dB 20Bit Stereo Δ Σ ADC & DAC

General Description

The AK4520 is a stereo CMOS A/D & D/A converter for middle-range MD/DAT, Surround System and musical instruments. Signal inputs and outputs are single-ended. The DAC outputs are analog filtered to remove out of band noise. External components are minimized.

Features

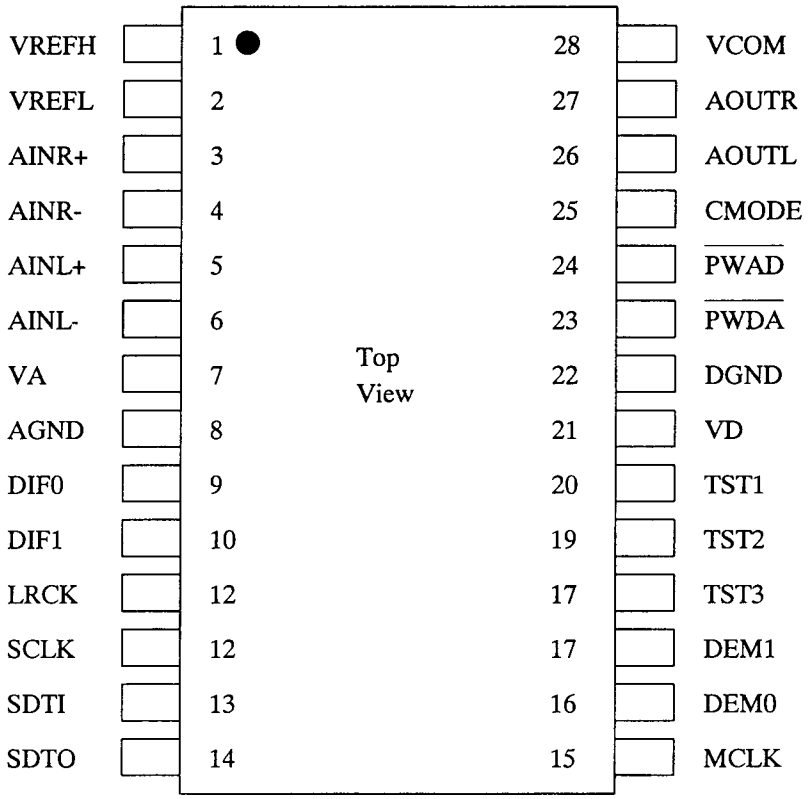
- ☐ Δ Σ Stereo ADC
  - 64x Oversampling
  - S/(N+D): 90dB at 5V, 86dB at 3V
  - Dynamic Range: 100dB at 5V, 96dB at 3V
  - S/N: 100dB at 5V, 96dB at 3V
  - Digital HPF for offset cancel
- ☐ Δ Σ Stereo DAC
  - 128x Oversampling
  - 2nd order SCF + 2nd order CTF
  - Digital de-emphasis for 32kHz, 44.1kHz, 48kHz sampling
  - S/(N+D): 90dB at 5V, 90dB at 3V
  - Dynamic Range: 100dB at 5V, 96dB at 3V
  - S/N: 100dB at 5V, 96dB at 3V
- ☐ High Jitter Tolerance
- ☐ Sample Rate Ranging from 16kHz to 54kHz
- ☐ Master Clock: 256fs or 384fs
- ☐ 2.7 to 3.6V or 4.5 to 5.5V supply
- ☐ Low Power Dissipation: 255mW
- ☐ Small 28pin VSOP Package



■ Ordering Guide

AK4520A-VF	-10 ~ +70 ℃	28pin VSOP
AKD4520	AK4520A Evaluation Board	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	VREFH	I	Positive Voltage Reference Input Pin, VA Used as a positive voltage reference by ADC & DAC. VREFH is connected externally to filtered VA.
2	VREFL	I	Negative Voltage Reference Input Pin, AGND Used as a negative voltage reference by ADC & DAC. VREFL is connected externally to AGND.
3	AINR+	I	Rch Analog Positive Input pin
4	AINR-	I	Rch Analog Negative Input Pin
5	AINL+	I	Lch Analog Positive Input pin
6	AINL-	I	Lch Analog Negative Input Pin
7	VA	-	Analog Power Supply Pin
8	AGND	-	Analog Ground pin
9	DIF0	I	Audio Data Interface Format Pin
10	DIF1	I	Audio Data Interface Format Pin
11	LRCK	I	Input/Output Channel Clock Pin
12	SCLK	I	Audio Serial Data Clock Pin
13	SDTI	I	Audio Serial Data Input Pin
14	SDTO	O	Audio Serial Data Output Pin
15	MCLK	I	Master Clock Input Pin
16	DEM0	I	De-emphasis Frequency Select Pin
17	DEM1	I	De-emphasis Frequency Select Pin
18 19 20	TST3 TST2 TST1	I/O I/O I	Test Pins (Pull down pins) Must be left open or connected to DGND.
21	VD	-	Digital Power Supply Pin
22	DGND	-	Digital Ground Pin
23	$\overline{\text{PWDA}}$	I	DAC Power-Down Mode Pin
24	$\overline{\text{PWAD}}$	I	ADC Power-Down Mode Pin
25	CMODE	I	Master Clock Select Pin "H": 384fs, "L": 256fs
26	AOUTL	O	Lch analog output pin
27	AOUTR	O	Rch analog output pin
28	VCOM	O	Common Voltage Output Pin, VA/2

Note: All input pins except pull-down pins should not be left floating.

ABSOLUTE MAXIMUM RATINGS

(AGND,DGND=0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supplies:	Analog	VA	-0.3	6.0	V
	Digital	VD	-0.3	6.0	V
	|AGND-DGND|	Δ GND	-	0.3	V
Input Current, Any Pin Except Supplies		IIN	-	± 10	mA
Analog Input Voltage		VINA	-0.3	VA+0.3	V
Digital Input Voltage		VIND	-0.3	VD+0.3	V
Ambient Temperature	(power applied)	Ta	-10	70	℃
Storage Temperature		Tstg	-65	150	℃

Note: 1 . All voltages with respect to ground.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AGND,DGND=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies:	3V operation					
(Note 2)	Analog	VA	2.7	3.0	3.6	V
	Digital	VD	2.7	3.0	VA	V
	5V operation					
	Analog	VA	4.5	5.0	5.5	V
	Digital	VD	4.5	5.0	VA	V

Note: 1. All voltages with respect to ground.
2. The power up sequence between VA and VD is not critical.

ANALOG CHARACTERISTICS

(Ta=25 ℃ ; VA,VD=5.0V; AGND=DGND=0V; VREFH=VA; VREFL=AGND; fs=44.1kHz; SCLK=64fs, Signal Frequency=1kHz; 20bit Data; Measurement frequency=10Hz ~ 20kHz; unless otherwise specified)

Parameter		min	typ	max	Units
ADC Analog Input Characteristics: Differential Inputs; Analog Source Impedance=470 Ω					
Resolution				20	Bits
S/(N+D) (-0.5dB Input)	VA=3V	80	86		dB
(Note 2)	VA=5V	84	90		dB
DR (-60dB Input, A-Weighted)	VA=3V	90	96		dB
(Note 3)	VA=5V	94	100		dB
S/N (A-Weighted)	VA=3V	90	96		dB
(Note 3,4)	VA=5V	94	100		dB
Interchannel Isolation		90	110		dB
Interchannel Gain Mismatch			0.1	0.3	dB
Gain Drift			20		ppm/ ℃
Input Voltage	VA=3V	1.7	1.8	1.9	Vpp
AIN=0.6x(VREFH-VREFL)	VA=5V	2.85	3.0	3.15	Vpp
Input Resistance		20	30		k Ω
Power Supply Rejection (Note 5)			50		dB
DAC Analog Output Characteristics:					
Resolution				20	Bits
S/(N+D)	VA=3V	84	90		dB
	VA=5V	84	90		dB
DR (-60dB Output, A-Weighted)	VA=3V	92	96		dB
(Note 3)	VA=5V	96	100		dB
S/N (A-Weighted)	VA=3V	92	96		dB
(Note 6,4)	VA=5V	96	100		dB
Interchannel Isolation		90	110		dB
Interchannel Gain Mismatch			0.1	0.3	dB
Gain Drift			20		ppm/ ℃
Output Voltage	VA=3V	1.77	1.87	1.97	Vpp
AOUT=0.62x(VREFH-VREFL)	VA=5V	2.95	3.1	3.25	Vpp
Load Resistance		10			k Ω
Load Capacitance				25	pF
Power Supply Rejection (Note 5)			50		dB

Note: 2. In case of single ended input, S/(N+D)=84dB(typ, @VA=5V).
3. In case of 16bit, DR and S/N of ADC are 98dB. DR of DAC is 98dB.
4. S/N measured by CCIR-ARM is 96dB at each converter and 94dB at ADC to DAC loopback.
5. PSR is applied to VA,VD with 1kHz, 50mVpp. VREFH/VREFL pin is held a constant voltage.
6. As the input data is "0", S/N is 100dB regardless of resolution.

Parameter			min	typ	max	Units
Power supply Current		VA=VD=5V				
Analog	AD+DA	PWAD="H",PWDA="H"		41	62	mA
VA	AD	PWAD="H",PWDA="L"		17	26	mA
	DA	PWAD="L",PWDA="H"		25	38	mA
Digital	AD+DA	PWAD="H",PWDA="H"		10	15	mA
VD	AD	PWAD="H",PWDA="L"		6	9	mA
(Note 7)	DA	PWAD="L",PWDA="H"		4	6	mA
VA+VD	Power down	PWAD="L",PWDA="L"		0.2	0.4	mA

Note: 7. The typical supply current of VD drops to AD+DA=5.5mA, AD=3.5mA, DA=2mA at 3.0V supply voltage.

FILTER CHARACTERISTICS

(Ta=25 ℃ ; VA,VD=2.7 ~ 5.5V; fs=44.1kHz; DEM0="1", DEM1="0")

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter(Decimation LPF):						
Passband (Note 8)	-0.005dB	PB	0		19.76	kHz
	-0.02dB		0		20.02	kHz
	-0.06dB		0		20.20	kHz
	-6.0dB		0		22.05	kHz
Stopband		SB	24.34			kHz
Passband Ripple		PR			± 0.005	dB
Stopband Attenuation		SA	80			dB
Group Delay (Note 9)		GD		29.3		1/fs
Group Delay Distortion		Δ GD		0		us
ADC Digital Filter(HPF):						
Frequency Response (Note 5)	-3dB	FR		0.9		Hz
	-0.5dB			2.7		Hz
	-0.1dB			6.0		Hz
DAC Digital Filter:						
Passband (Note 8)	-0.06dB	PB	0		20.0	kHz
	-6.0dB		0		22.05	kHz
Stopband		SB	24.1			kHz
Passband Ripple		PR			± 0.06	dB
Stopband Attenuation		SA	43			dB
Group Delay (Note 9)		GD		14.7		1/fs
DAC Digital Filter+Analog Filter:						
Frequency Response 0 ~ 20.0kHz		FR		± 0.1		dB

Notes: 8. The Passband and stopband frequencies scale with fs. For example, 20.02kHz at -0.02dB is 0.454 x fs. The reference frequency of these responses is 1kHz.

9. The calculating delay time which occurred by digital filtering. This time is from the input of analog signal to setting the 20bit data of both channels to the output register for ADC.
For DAC, this time is from setting the 20bit data of both channels on input register to the output of analog signal.

DIGITAL CHARACTERISTICS

(Ta=25 ℃ ; VA,VD=2.7 ~ 5.5V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	70%VD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%VD	V
High-Level Output Voltage (Iout=-100uA)	VOH	VD-0.5	-	-	V
Low-Level Output Voltage (Iout=100uA)	VOL	-		0.5	V
Input Leakage Current	Iin	-	-	± 10	uA

SWITCHING CHARACTERISTICS

(Ta=25 ℃ ; VA,VD=2.7 ~ 5.5V; C_L=20pF)

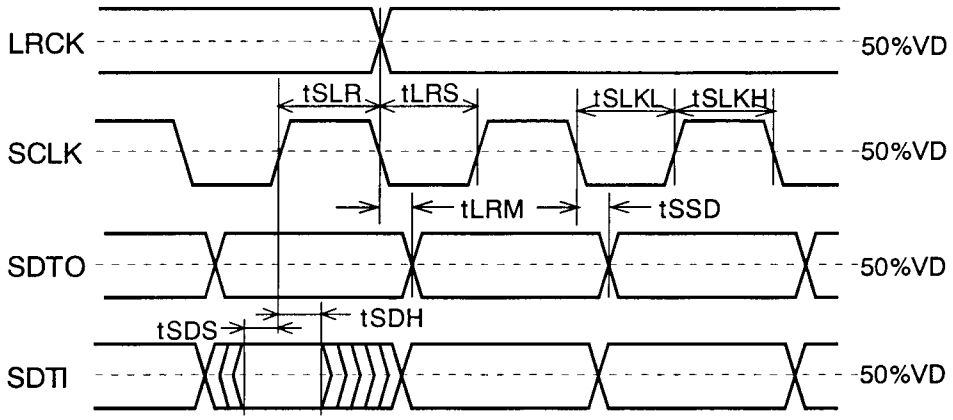
Parameter		Symbol	min	typ	max	Unit
Master Clock Timing	256fs:	fCLK	4.096		13.824	MHz
	Pulse Width Low	tCLKL	27			ns
	Pulse Width High	tCLKH	27			ns
	384fs:	fCLK	6.144		20.736	MHz
	Pulse Width Low	tCLKL	20			ns
	Pulse Width High	tCLKH	20			ns
LRCK Frequency	(Note 10)	fs	16	44.1	54	kHz
Duty Cycle			45		55	%
Serial Interface Timing						
SCLK Period		tSCK	289.4			ns
SCLK Pulse Width Low		tSCKL	120			ns
Pulse Width High		tSCKH	120			ns
LRCK Edge to SCLK " ↑ "	(Note 11)	tLRS	30			ns
SCLK " ↑ " to LRCK Edge	(Note 11)	tSLR	30			ns
LRCK to SDTO(MSB)		tLRM			100	ns
SCLK " ↓ " to SDTO		tSSD			100	ns
SDTI Hold Time		tSDH	40			ns
SDTI Setup Time		tSDS	40			ns
Reset Timing						
PWAD & PWDA Pulse Width		tPW	150			ns
PWAD " ↑ " to SDTO valid	(Note 12)	tPWV		516		1/fs

Notes: 10. If the duty cycle of LRCK changes larger than 5 to 50%, the AK4520A is reset by the internal phase circuit automatically.

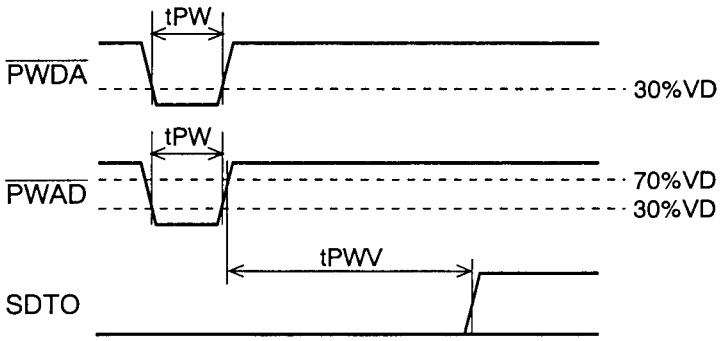
11. SCLK rising edge must not occur at the same time as LRCK edge.

12. These cycles are the number of LRCK rising from PWAD rising.

■ Timing Diagram



Serial Interface Timing



Reset & Initialize Timing

OPERATION OVERVIEW

■ System Clock Input

The AK4520A with CMODE is used to select either MCLK=256fs or 384fs. The relationship between the external clock applied to the MCLK input and the desired sample rate is defined in Table 1. The LRCK clock input must be synchronized with MCLK, however the phase is not critical. Internal timing is synchronized to LRCK upon power-up or when the internal timing becomes out of phase. All external clocks must be present unless both PWDA and PWAD ="L", otherwise excessive current may result from abnormal operation of internal dynamic logic.

fs	MCLK		SCLK	
	256fs CMODE="L"	384fs CMODE="H"	64fs	32fs
32.0kHz	8.1920MHz	12.2880MHz	2.048MHz	1.0240MHz
44.1kHz	11.2896MHz	16.9344MHz	2.822MHz	1.4112MHz
48.0kHz	12.2880MHz	18.4320MHz	3.072MHz	1.5360MHz

Table 1. System Clock Example

■ Audio Serial Interface Format

Data is shifted in/out the SDTI/SDTO pins using SCLK and LRCK inputs. Four serial data modes are supported selected by the DIF0 and DIF1 pins as shown in Table 2. In all modes the serial data is MSB-first, 2's compliment format is clocked on the falling edge of SCLK. For mode 3, if SCLK is 32fs, then the least significant bits will be truncated.

Mode	DIF1	DIF0	SDTO(ADC)	SDTI(DAC)	L/R	SCLK
0	0	0	16bit, MSB justified	16bit, LSB justified	H/L	≧ 32fs
1	0	1	20bit, MSB justified	20bit, LSB justified	H/L	≧ 40fs
2	1	0	20bit, MSB justified	20bit, MSB justified	H/L	≧ 40fs
3	1	1	IIS(I2S)	IIS(I2S)	L/H	32fs or ≧ 40fs

Table 2. Serial Data Modes

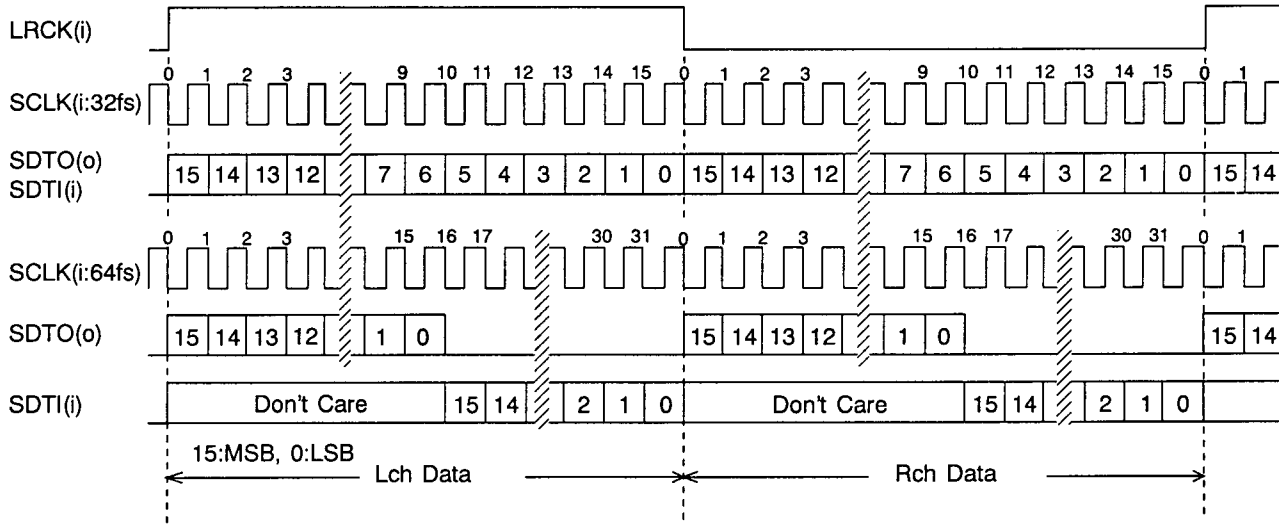


Figure 1. Mode 0 Timing

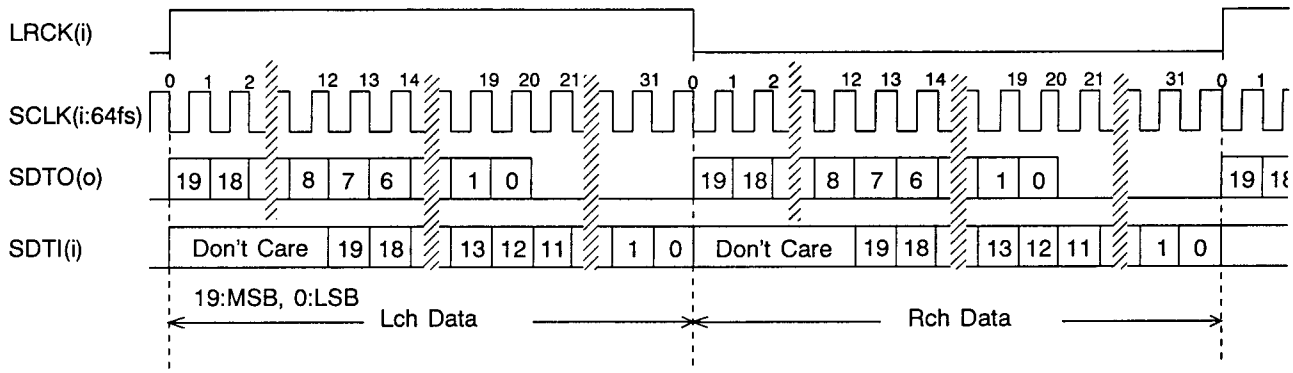


Figure 2. Mode 1 Timing

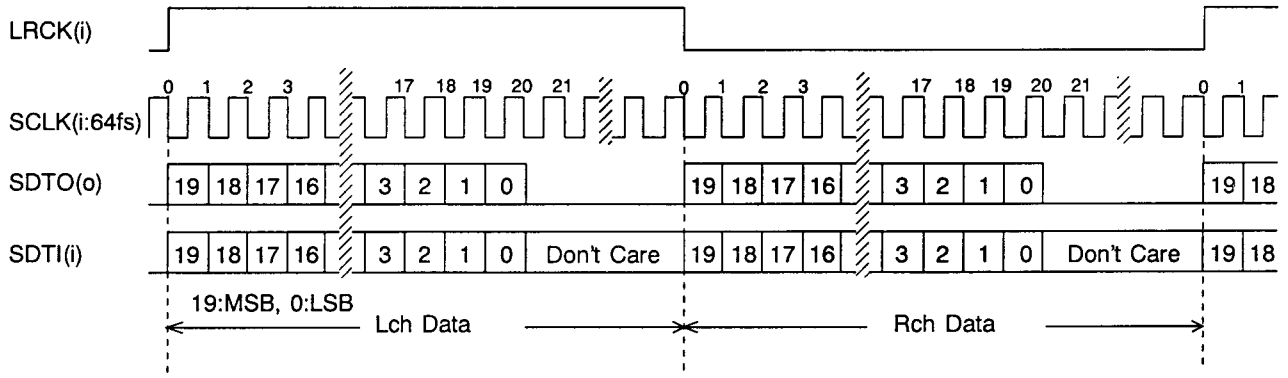


Figure 3. Mode 2 Timing

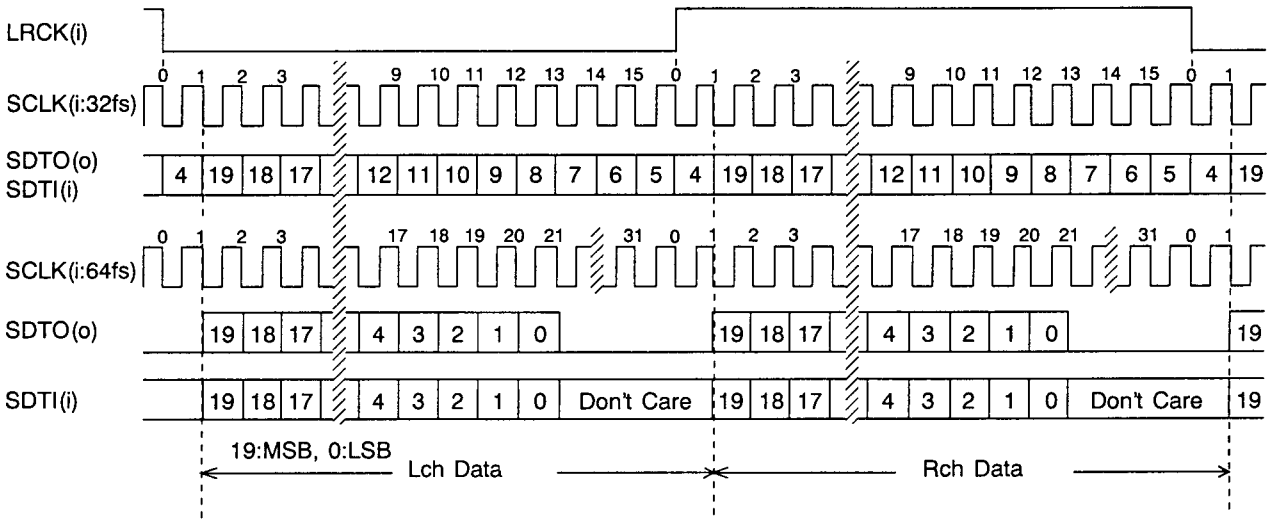


Figure 4. Mode 3 Timing

■ Digital High Pass Filter

The ADC of AK4520A has a digital high pass filter for DC offset cancel. The cut-off frequency of the HPF is 0.9Hz at fs=44.1kHz and also scales with sampling rate(fs).

■ De- emphasis filter

The DAC of AK4520A includes the digital de-emphasis filter(tc=50/15us) by IIR filter. This filter corresponds to three frequencies (32kHz,44.1kHz,48kHz). The de-emphasis filter selected by DEM0 and DEM1 is enabled for input audio data. The de-emphasis is also disabled at DEM0="1" and DEM1="0".

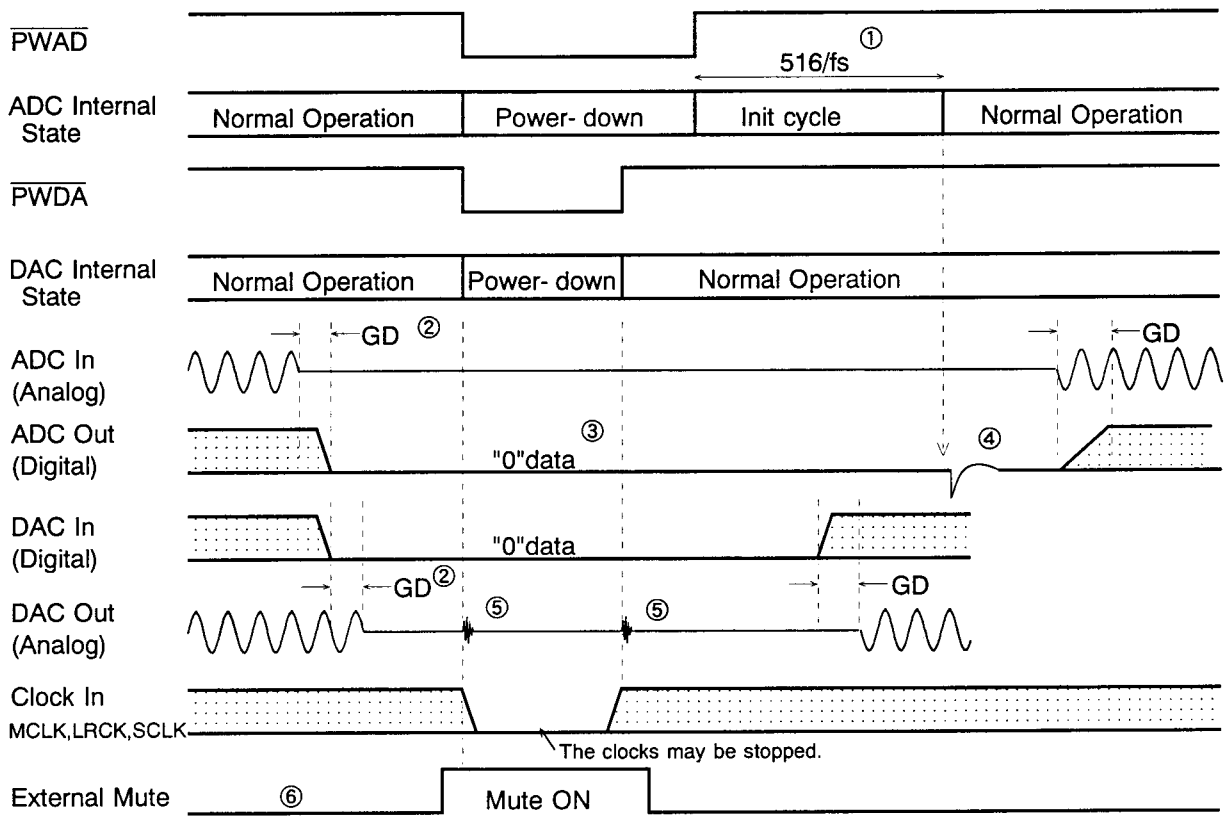
DEM 1	DEM0	Mode
0	0	44.1kHz
0	1	OFF
1	0	48kHz
1	1	32kHz

Table 3. De-emphasis filter control

■ Power- Down & Reset

The ADC and DAC of AK4520A are placed in the power-down mode by bringing each power down pin, $\overline{\text{PWAD}}$ $\overline{\text{PWDA}}$ "L" independently and each digital filter is also reset at the same time. This reset should always be done after power-up. In case of the ADC, an analog initialization cycle starts after exiting the power-down mode. Therefore, the output data, SDTO becomes available after 516 cycles of LRCK clock. This initialization cycle does not affect the DAC operation.

Figure 5 shows the power-up sequence when the DAC is powered up before the ADC power-up.



① The analog part of ADC is initialized after exiting the power-down state.
② Digital output corresponding to analog input and analog output corresponding to digital input have the group delay(GD).
③ A/D output is "0" data at the power-down state.
④ Click noise occurs at the end of initialization of the analog part. Please mute the digital output externally if the click noise influences system application. Required muting time depends on the configuration of the input buffer circuits.
Figure 6: 1s
Figure 9: 200ms
⑤ Click noise occurs at the edge of $\overline{\text{PWDA}}$.
⑧ Please mute the analog output externally if the click noise(⑥) influences system application.

Figure 5. Power-up sequence

SYSTEM DESIGN

Figure 6 shows the system connection diagram. This is an example which analog signal is input by single ended circuit. In case of differential input, please refer to Figure 9. An evaluation board is available which demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.

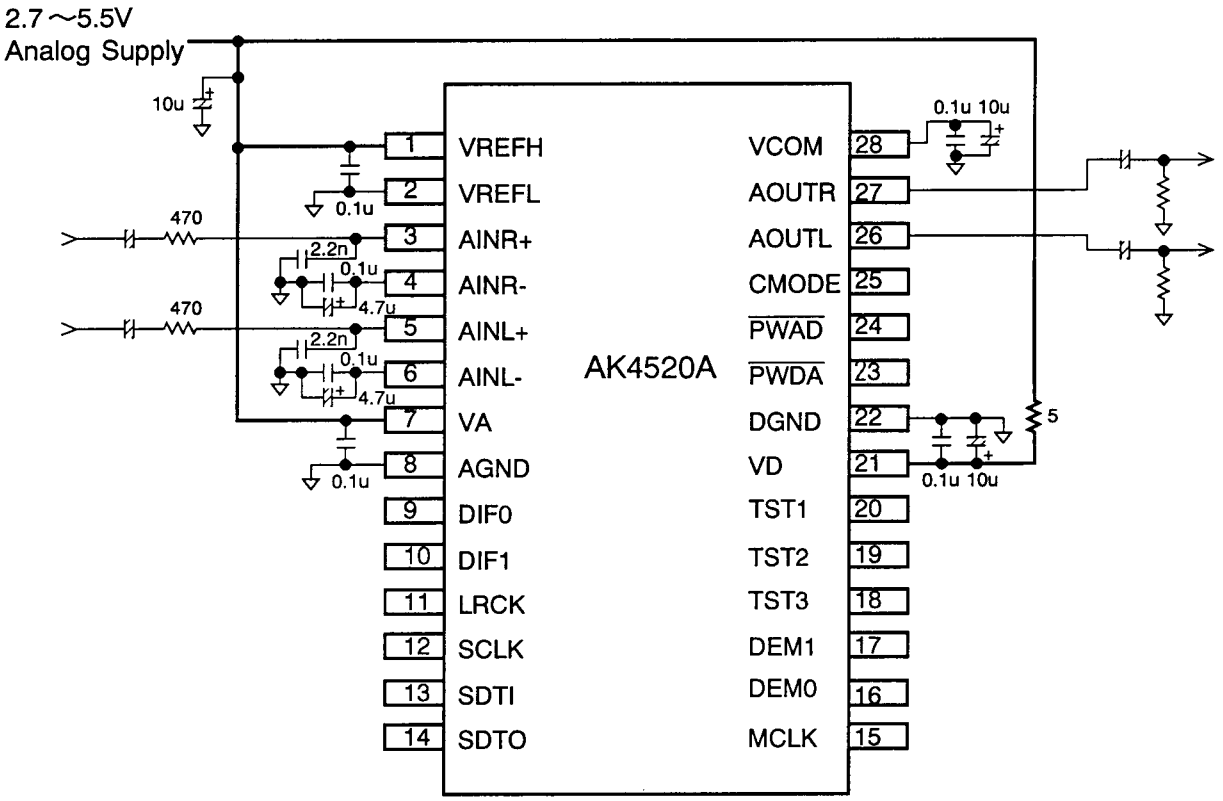


Figure 6. Typical Connection Diagram

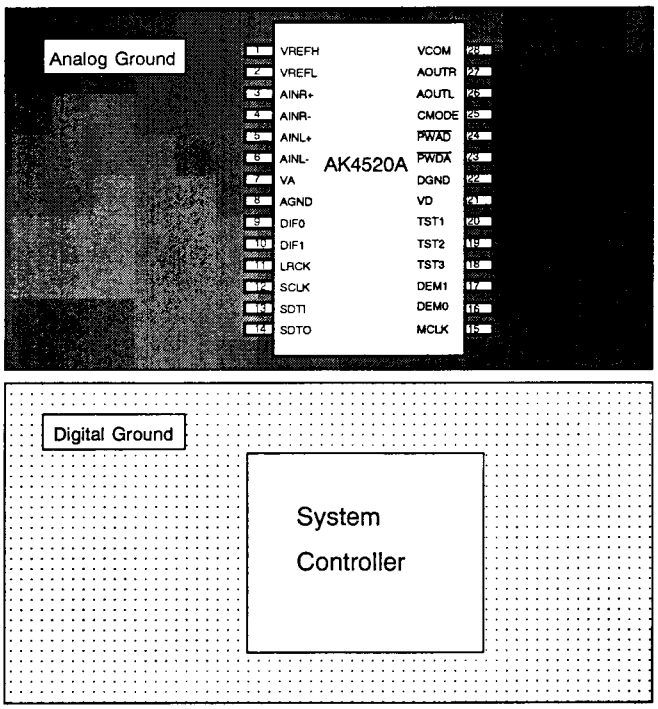
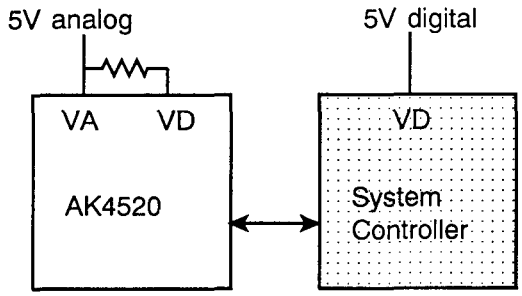
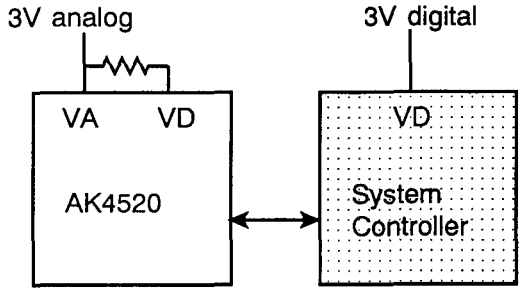


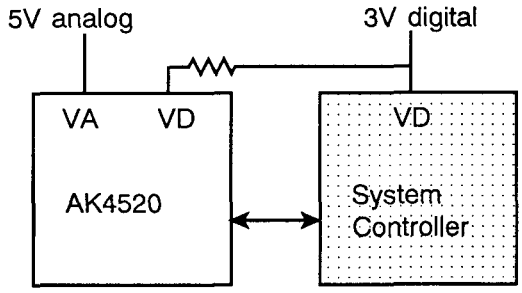
Figure 7. Ground Layout



Case 1. 5V system



Case 2. 3V system



Case 3. 5V/3V system

Figure 8. Power Supply Arrangement

1. Grounding and Power Supply Decoupling

The AK4520A requires careful attention to power supply and grounding arrangements. VA and VD are usually supplied from analog supply in system. Alternatively if VA and VD are supplied separately, the power up sequence is not critical. AGND and DGND of the AK4520A should be connected to analog ground plane. System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4520A as possible, with the small value ceramic capacitor being the nearest.

2. On-chip voltage reference

The differential Voltage between VREFH and VREFL sets the analog input/output range. VREFH pin is normally connected to VA with a 0.1uF ceramic capacitor and VREFL pin is connected to AGND. VCOM is a signal ground of this chip. An electrolytic capacitor 10uF parallel with a 0.1uF ceramic capacitor attached to VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from VCOM pin. All signals, especially clocks, should be kept away from the VREFH,VREFL and VCOM pins in order to avoid unwanted coupling into the AK4520A.

3. Analog Inputs

The ADC inputs are differential and internally biased to the common voltage(VA/2) with 30k Ω (typ) resistance. Figure 6 is a circuit example which analog signal is input by single end. the signal can be input from either positive or negative input and the input signal range scales with the supply voltage and nominally 0.6 x (VREFH-VREFL) Vpp. In case of single ended input, the distortion around full scale degrades compared with differential input. Figure 9 is a circuit example which analog signal is input to both positive and negative input and the input signal range scales with the supply voltage and nominally 0.3 x (VREFH-VREFL) Vpp. The AK4520A can accept input voltages from AGND to VA. The ADC output data format is 2's complement The output code is 7FFFFH(@20bit) for input above a positive full scale and 80000H(@20bit) for input below a negative full scale. The ideal code is 00000H(@20bit) with no input signal. The DC offset is removed by the internal HPF.

The AK4520A samples the analog inputs at 64fs. The digital filter rejects noise above the stop band except for multiples of 64fs. A simple RC filter(fc=150kHz) may be used to attenuate any noise around 64fs and most audio signals do not have significant energy at 64fs.

The AK4520A has tone noise with around -110dB on the ADC output. There are two methods of dropping VD to 3V or adding a small DC offset at the ADC input to reduce the noise level. The evaluation board(AKD4520) manual should be referred about the detail.

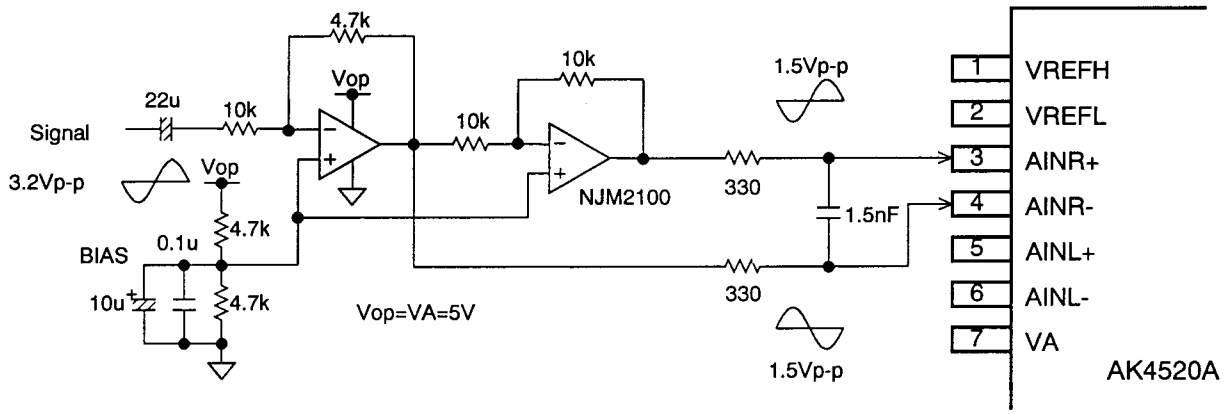


Figure 9. Differential Input Buffer Example

4. Analog Outputs

The analog outputs are also single-ended and centered around the VCOM voltage. The input signal range scales with the supply voltage and nominally 0.62 x (VREFH-VREFL) Vpp. The DAC input data format is 2's complement. The output voltage is a positive full scale for 7FFFFH(@20bit) and a negative full scale for 80000H(@20bit). The ideal output is VCOM voltage for 00000H(@20bit). The internal switched-capacitor filter and continuous-time filter removes most of the noise generated by the delta-sigma modulator of DAC beyond the audio passband.

DC offsets on analog outputs are eliminated by AC coupling since DAC outputs have DC offsets of a few mV. Figure 10 shows the example of external op-amp circuit with 6dB gain. The output signal is inverted by using the circuit in this case.

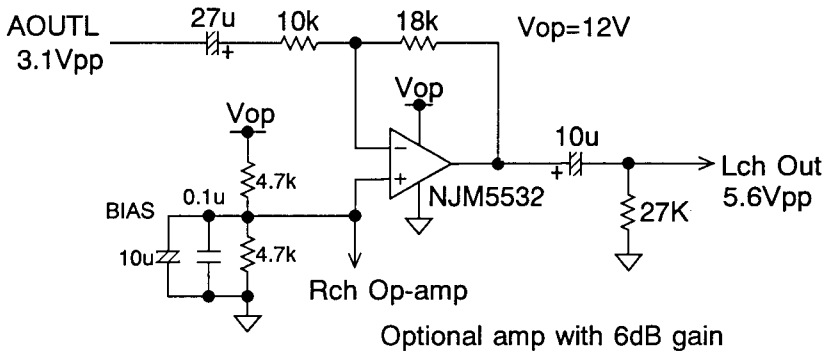
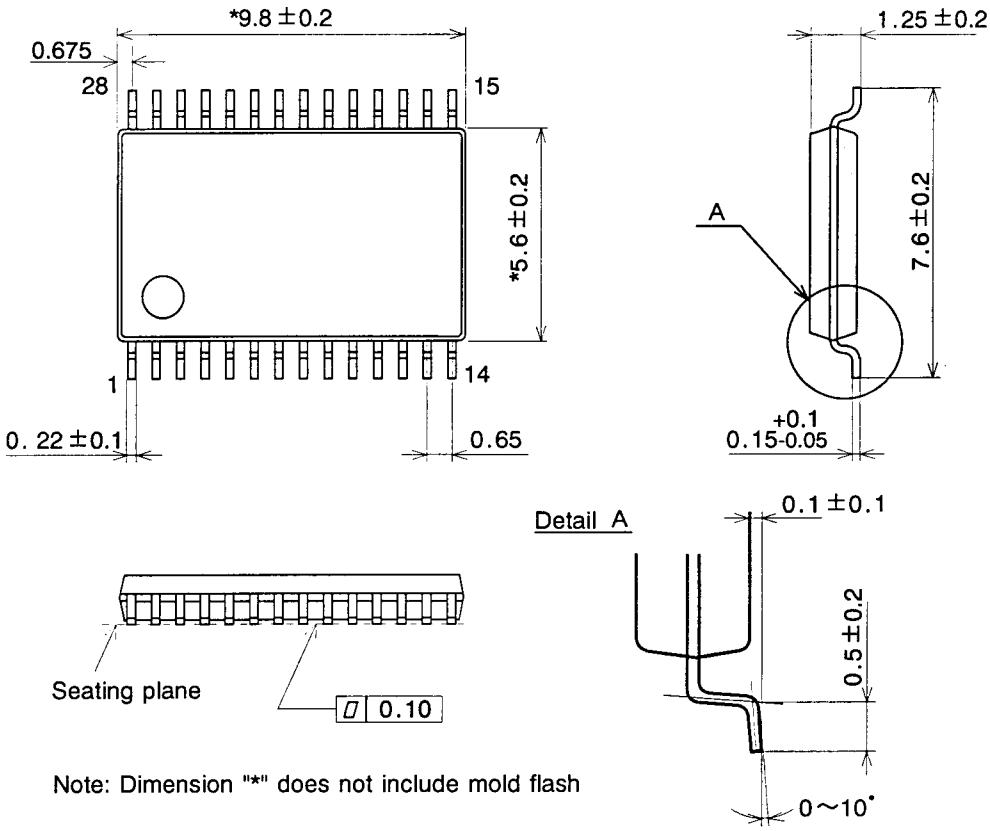


Figure 10. External analog circuit example(gain=6dB)

PACKAGE

● 28pin VSOP (Unit: mm)

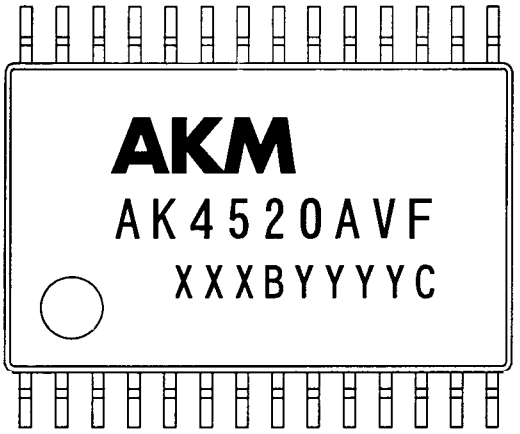


Note: Dimension "*" does not include mold flash

■ Material & Lead finish

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder plate

MARKING



XXXBYYYYC data code identifier

XXXB : Lot number (X : Digit number, B : Alpha character)
YYYYC : Assembly date (Y : Digit number, C : Alpha character)

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AK4520A datasheet(Rev 1.2) Revised Point

1997.2.12

Old(Rev 1.1)		New(Rev 1.2)		Comments
Page	Contents	Page	Contents	
13	Figure 6. Pin No No.3- AINL+, No.4- AINL- No.5- AINR+, No.6- AINR-	13	Figure 6. Pin No No.3- AINR+, No.4- AINR- No.5- AINL+, No.6- AINL-	Erratum Pin layout on Page 2 is correct.
15	Figure 9. Pin No.5- AINL-	15	Figure 9. Pin No.5- AINL+	Erratum