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https://www.ardent-tool.com/Reply/Appian_ADI2.html

Description

Function: VESA Local Bus IDE controller

Manufacturer:

- Appian Technology, Inc. (ADI/2)
- Cirrus Logic, Inc. (CL-PD7220)
- Adaptec (AIC-25VL01)

Features:

- One IDE channel
- IORDY support
- Read ahead support

Used in: various boards, IWILL SIDEjr L, Acculogic sIDE4-VL

Manufacturer support: Appian Technology bankrupted, Adaptec none

Documentation available: none

Drivers available: DOS, Win 3.1x, OS/2 2.11, WARP

Control Registers Address

0x034, 0x038, 0x03C - alternate addresses

0x0B4, 0x0B8, 0x0BC - standard addresses

0xAD4, 0xAD8, 0xADC - addresses added in rev. "B" of the silicon

Used address is selected by jumpers.

Detection

From address 0x034, 0x0B4 or 0xAD4 can be read ID, this ID can be 0x30, 0x31, 0x32, 0x33 and is set by jumpers.

Programming

0x038, 0x0B8 or 0xAD8 - address register

0x03C, 0x0BC or 0xADC - data register

There are 15 registers:

Register 1 - Configuration Register

Bit 0: 1=Enable ADI2 0=Disable ADI2
Bit 1: 1=Enable Data in T2, 0=Data presented in 2nd T2
Bit 2: 1=Enable (LDRY#) in T2 Reads, 0=Read cycles are min 1 wait state
Bit 3: 1=Enable (LDRY#) in T2 Writes, 0=Write cycles are min 1 wait state
Bit 4: 1=Read Ahead always active, 0=Read Ahead not always active
Bit 5: 1=Enable IDE command monitoring, 0=Disable IDE command monitoring
Bit 6: 1=Enable config ready, 0=Disable config ready
Bit 7: 1=Enable fast switch, 0=Disable fast switch

Register 2 - Data Byte Time Register

Bits 3-0: Data Byte Recovery count in number of clock cycles (for 8 bit cycle)
Bits 7-4: Data Byte Active count in number of clock cycles (for 8 bit cycle)

Register 3 - Disk 0 Read Time Register

Bits 3-0: Disk 0 read recovery count in number of clock cycles
Bits 7-4: Disk 0 read active count in number of clock cycles

Register 4 - Disk 0 Write Time Register

Bits 3-0: Disk 0 write recovery count in number of clock cycles
Bits 7-4: Disk 0 write active count in number of clock cycles

Register 5 - Disk 0 R/A Count Register

Bits 7-0: Disk 0 least significant read ahead count bits

Register 6 - Disk 0 R/A Control Register

Bits 1-0: Disk 0 most significant read ahead count bits
Bits 6-3: Reserved
Bit 7: Enable Read Ahead for Disk 0

Register 7 - Disk 0 Control Register

Bits 1-0: Disk 0 address setup bits specify the number of clocks of address setup time before a DIOR# or DIOW#
Bits 7-3: Reserved

Register 8 - Disk 1 Read Time Register

Bits 3-0: Disk 1 read recovery count in number of clock cycles
Bits 7-4: Disk 1 read active count in number of clock cycles

Register 9 - Disk 1 Write Time Register

Bits 3-0: Disk 1 write recovery count in number of clock cycles
Bits 7-4: Disk 1 write active count in number of clock cycles

Register 10 - Disk 1 R/A Count Register

Bits 7-0: Disk 1 least significant read ahead count bits

Register 11 - Disk 1 R/A Control Register

Bits 1-0: Disk 1 most significant read ahead count bits
Bits 6-3: Reserved
Bit 7: Enable Read Ahead for Disk 1

Register 12 - Disk 1 Control Register

Bits 1-0: Disk 1 address setup bits specify the number of clocks of address setup time before a DIOR# or DIOW#
Bits 7-3: Reserved

Register 13 - Rev Revision Register (R/O)

Bits 7-0: IC revision number

Register 14 - R/A Counter Register (R/O)

Bits 7-0: Read ahead counter register. Used primarily for debugging

Register 15 - Mode Register

Bit 0: Enable Read 0x3F7 as an input
Bit 1: 1=Zero wait state for read cycle, 0=One wait state for read cycle
Bits 7-3: Reserved