Appendix A
SiS/ISA 486 SiS85C401

FUNCTIONAL DESCRIPTION
Cache Controller
Direct Mapped Cache

Cache is a good means to de-couple fast processor from slow main memory and get the best performance of the processor. Direct mapped cache is the most suaightforward, flexible, easyto-implement, and cost-effective cache structure. A 2/4-way set associative cache has better performance than the direct mapped cache, but the delta is negligible when the cache size is large enough (e.g. 64KB). The SiS85C401 provides a fast 8-bit tag comparator and all the control logic for a secondary cache of the 80486 processor. To implement a cache, user just needs to add SRAMs for the tag and data memories. The maximum cache size in the configuration register is 256KB but larger (512KB, IMB, etc.) size is still applicable.

Write-Back vs. Write-Through

When the contents of the cache data are modified (i.e. written) by the processor, the same changes should be made in the main memory as well. Failing to do so will raise an inconsistency problem when the stale data in the main memory are accessed. There are two general approaches to update the main memory. The first is the write-through method and the second is the writeback (also called "copy-back") method.

In a write-through cache system, data are written to the main memory immediately while or after they are wntten into the cache. So the main memory always contains valid data. All the memory writes will only be as fast as the DRAM write and do not take the speed advantage of the cache. To improve the write speed, a write buffer (queue) can be used to store the written data, so the processor can do other things before the data are actually written into the main memory. Since there is already a four-level wnte buffer built-in in the 80486, the DRAM access penalty coming from the write cycles is reduced significantly.

In a write-back cache system, there is an "alter" bit per data LINE (data line means the data block referenced to a specific tag). When a write hit happens on the *cache, the* corresponding alter bit will be set. The written data are transferred to the main memory when they are to be over-written by a cache line fill. In this case, the cache controller checks the corresponding alter bit. If the alter bit is set, the cache data will then be written to the main memory before the cache line fill starts.

A write-back cache can offer higher performance than a write-through cache if writes to the main memory are much,slower than writes to the cache. The write-back cache is also favored when a memory location is written several times in the cache before written into the main memory. The performance advantage of the write-back cache over write-through cache is software dependent.

The SiS85C401 can be configured to provide a write-back or write-through cache scheme. Besides tag and data RAM, a write-back cache needs an SRAM for the alter bits. So a writeback cache may have better performance, but costs more, than a write-through cache does. It is up to the indivisual user to judge if the extra cost of the write-back cache is justified.

80486 Burst Cache Line Fill

The internal cache of the 80486 has a 16-byte line size. When a read miss happens in the internal cache, the 80486 initiates off-chip memory read cycles to update current cache line. The 80486 will read 16 continuous bytes (4 doublewords). To increase the bus throughput, the 80486 provides a burst mode transfer, four doublewords can be read sequentially in 5 processor clocks (2-1-1-1) at the fastest.

The secondary cache provided by the SiS85C401 also has a 16-byte line size. It supports the 80486 burst read cycles to get the fastest cache line fill. When both the 80486 intemal and secondary caches encounter a read miss, they are updated with the data read from DRAM simultaneously.

Cache Update Policy

For CPU cycles, the content of the cache memory is renewed when either the cache read miss or write hit occurs. Tag and data RAMs are both updated in the cache read miss cycles. In the cache write hit cycles, the SiS85C401 updates only the data RAM.

In the cache write miss cycles, the 80486 writes data into the main memory (DRAM), while the cache memory remains unchanged. The alter bits in the write-back cache are reset in the cache update (read miss) *cycles* and *set* in the write hit cycles.

When the cache is disabled, all the CPU reads to the cacheable memory, are treated as cachc read miss, so both tag and data RAMs are updated. This feature is used tO initialize the cache memory before enabling it.

In DMA/master cycles, the cache data RAM is written when a write hit occurs, to assure the cache coherency. Cache memory is not accessed in DMA/master write miss or read cycles for the write-through cache. For the write-back cache, DMA/master read hit cycles are conducted to the cache, not to the DRAM.

Cache Size Options(16 * 4 -20)

Cache Size	Tac RAM	Data RAM	Alter RAM	Cacheable Size
32KB	2Kx8	8Kx8 x4	2Kxl	8MB
64KB	4Kx8	8Kx8 x8	4Kxl	16MB
128KB	8Kx8	32Kx8 x4	8Kxl	32MB
256KB	16Kx8	32Kx8 x8	16Kxl	64MB
51 2KB	32Kx8	1 28Kx8 x4	32Kxl	64MB

The cacheable DRAM size is determined by the cache size because the tag address field is always 8-bit wide. The on-board DRAM beyond the cacheable size is not cacheable for the secondary cache. It is still cacheable for the 80486 internal cache, however.

Cache Speed Options

· *The* secondary cache can be configurated to non-interleave or two-bank interleave. Two-bank interleaved *cache can* use slower *cache data* RAM but needs more data RAM chips.

The SiS85C401 provides four cache read speed options: 2-1-1-1, 3-1-1-1, 2-2-2-2 and 3-2-2-2, and two options of cache write cycle: 2T or 3T. The cache read speed x-y-y-y is selected via the bit 7 of configuration register 60 (x) and the bit 0 of configuration register 61 (y). The 2T cache write is applicable only when the first cache read of a burst is also set to 2T (2-1-1-1 or 2-2-2-2).

To reduce the propagation delay of the chip output buffer, the SiS85C401 employs an "advanced clock" instead of CPU clock to clock the cache read control signals. The adv;mced clock should lead CPU clock by 3 to 7 ns. It will increase the margin of data RAM access time. For 16/20 MHZ systems, the ACLK can be connected to CPUCLK to simplify the clock circuit.

The following is a table of cache configurations and suggested speed ratings of the SRAM for implementing the cache data RAM for various speeds of the 80486 CPU.

Cache Confiauration	25MHz CPU	33MHz CPU	40MHz CPU	5OMHz CPU
2-1-2 Interleave (*1)	35 (*2)	-20	-12	---
2-1-2 Non-interleave	-25	-15	---	---
2-1-3 Interleave .	-40	-25	-20	---
2-1-3 Non-interleave	-25	- 15	---	---
3-1-3 Interleave	-55	-35	-25	-15
3-1-3 Non-interleave	-25	-15	---	---
2-2-2 Non-interleave	-35	-20	-12	---
2-2-3 Non-interleave	-40	-25	-20	---
3-2-3 Non-interleave	-65	-45	-35	-25

Note: * 1. x-y-z means x-y-y-y burst read and zT write cycle
* 2. -m means the access speed of SRAM in ns.

The following is a table of cache configurations and suggested speed ratings of the SRAM for implementing the cache tag and alter RAM for various speeds of the 80486 CPU.

Cache ConfiauraUon	25MHz CPU	33MHz CPU	40MHz CPU	50MHz CPU
2-X-2	-25	-20	-1 2	-----
2-X-3	-35	-25	-15	-----
3-X-3	-45	-35	-25	-20

· **Note: X presents elther 1T or 2T cycles.**

Non-Cacheable Regions

In some applications, users desire a block of memory not to be cached. The SiS85C401 provides two programmable non-cacheable regions to serve this function. Besides, the cacheability of the shadow RAM can be programmed in 32KB granularity.

Only the on-board DRAM directly controlled by the SiS85C401 is cacheable. The memory residing on the AT add-ons is non-cacheable. When a memory space is mapped by both the on-board DRAM and AT add-on memory, CPU access will be conducted to the on-board DRAM. If users desire the AT add-on memory to be accessed instead of the on-board DRAM at the overlapped memory space, the two non-cacheable regions can be used to disable the on-board DRAM in the programmed space.

The size and starting address of two non-cacheable regions are programmable in configuration register 64, 65, 66 and 67. The validity of the starting address bits depends on the size of related non-cacheable region.

Size	A23	A22	A21	A20	A19	A18	A17	A16
64K	V	V	V	V	V	V	V	V
128K	V	V	V	V	V	V	V	X
256K	V	V	V	V	V	V	X	X
512K	V	V	V	V	V	X	X	X
IM	V	V	V	V	X	X	X	X
2M	V	V	V	X	X	X	X	X
4M	V	V	X	X	X	X	X	X

V =Valid
X = Don't Care

Cache Initialization

The secondary cache supported by the SiS85C401 does NOT provide the validation flag (bit) for the data lines. All the cache data are assumed valid once the cache is enabled. So the whole cache must be filled by valid data before the cache enable bit is turned on. The cache initialization can be done via sequential reads to a block of on-board DRAM which is equal to or larger than the cache in size.

DRAM Controller

Because the 80486 already has an 8K bytes internal cache, the-performance contribution of a secondary cache in the 80486 systems is not as significant as that in the 80386 systems. Many 80486 systems may therefore be built without the secondary cache. The performance of the DRAM access becomes important in these systems. The SiS85C401 povides a high performance DRAM controller for the 80486 system.

Burst Read for Cache Line Fill

Both the 80486 internal cache and the secondary cache provided by the SiS85C401 have a 16-byte line size. When the read miss happens in both caches memories, the SiS85C401 offers a DRAM burst of 4 doubleword-reads to fill the cache lines in the 80486 and the secondary cache.

Bank (Double-word) Interleave

The 80486 burst read is so fast that wait states are needed for DRAM accesses even in page hit burst cycles. Because Ihe burst cycles are sequential – in even-odd-even-odd sequence, the word interleave scheme is adaptive to hide pre-charge overhead in the burst read cycles. When even bank (doubleword) is accessed, the odd bank does the pre-charge, and vice versa. The commonly used "page interleave" scheme does not take the advantage of the sequential burst because all of the four reads will access the same bank.

The SiS85C401 knows if the DRAM interleave is applicable to current DRAM size configu˙ ration or not. So the DRAM interleave enable bit in configuration regisler 61 can be always set to ON. DRAM interleave will not be tumed on if the size setting is not interleave applicable.

DRAM Speed Options

The SiS85C401 provides 5 read and 2 write speed options in the configuration register. A table of page hit cycle time of all the possible speed configurations is listed as follows:

	Interleave Read	Non-interleave Read	Write
Supper Fast	3 -1-1-1	3-2-2-2	2
Fastest	4 -1-1-1	4-2-2-2	2
Faster	5-2-2-2	5-3-3-3	2/3
Slower	6-2-2-2	6-4-4-4	3/4
Slowest	7-3-3-3	7-5-5-5	4

Note: The unit of the above table is in T cycles.

There will be plenty of timing margin if the user adopt Super Fast for 16/20MHz 80486, Fastest for 25MHz, Faster for 33MHz, Slower for 40MHZ, and Slowest for 50MHz, even when 100ns DRAMs are used.

DRAM Access Timing

	Fastest	Faster	Slower	Slowest	Slow-CPU	
Trcd	2T	2T	3T	3T	1 T	RAS-to-CAS delay
Tcas	1T	2T	2T	3T	1T	Read CAS pulse width
Trp	3T	3T	4T	5T	2T	RAS precharge
Tcp	1 T	1 T	2T	2T	1 T	CAS precharge

DRAM Size Configuration

The SiS85C401 supports 32 different DRAM configurations in 4 banks. Besides the traditional 256K/IM/4M xN DRAMs, the new 512K xN and future 2M xN DRAMs are also supported. The doubleword interleave scheme is applicable when bank 0/1 and bank 2/3 are implemented with same DRAM types, respectively.

Transparent Refresh

In the original PC/AT design, the CPU is held off (i.e. can not do anything) during the DRAM refresh cycles. It happens once per 16us and takes at least 0.Sus each time.

Recently the speed of DRAM is becoming faster so the time needed per refresh cycle is getting shorter. The refresh cycle time for the 100ns DRAM is 200ns minimum, for example. In a system with cache, most of the CPU accesses are referred to the cache so that the DRAM usage (percent of time the DRAM is accessed by the CPU) is significantly reduced.

In the SiS85C401, the main memory refresh is independent to the AT-bus refresh so the cycle time is shorter (need not follow the standard AT-bus timing). When the main memory is refreshed, the CPU is NOT held off so it may execute the program stored in the cache at the same tirne. If the CPU accesses the main memory while it is being refreshed, this access will be pending (i.e. the CPU must wait) until the refresh is finished.

'Ihe following table lists the refresh-related RAS timings of the on-board DRAM:

	Fastest	Faster	Slower	Slowest	Slow-CPU
RAS pre-charge	3T	3T	4T	5T	2T
RA.Ci ctive	3T	4T	5T	6T	3T

On the other hand, the AT bus refresh cycles are issued by the SiS85C401 once per 16us when there is no access from the (CPU, the DMA controller, or the bus master on the AT bus. The 80486 CPU will not feel the existing of the AT bus refresh unless it issues an AT cycle coincidentaly. The SiS85C401 arbitrates among the CPU AT cycle, DMA/master request, and bus refresh so that they can be executed one after another when more than one of them intend to use the AT bus at the same time.

The SiS85C401 has a slow refresh feature to cut the refresh frequency down to 1/4. It should be selected only when the system is equipped with slow-refresh DRAM.

The refresh scheme of local DRAM is the CAS-before-RAS refresh. The CASs go active at least one- T before RASs in local refresh. To reduce the power noise caused by refresh, the RASs of odd banks go active one T aher that of even banks. It is called "staggered refresh".

Shadow RAM

Memory space OAOOOO-OFFFFFh is reserved for the video RAM, 1/0 and system BIOS ROM. Access to this area should not be conducted to the main memory in standard PC/AT. Since the speed of the DRAM is significantly faster than that of the ROM, if contents of the BIOS ROM are copied to the unused DRAM (OAOOOO- OFFFFFh), the DRAM can work as fast BIOS ROM and raise the overall system performance. This is called the "Shadow RAM".

The SiS85C401 provides shadow to OCOOOO-OEFFFFh in 32KB granularity and shadow to OFOOOO-OFFFFFh. Because many 1/0 related codes cannot be executed too fast, the cacheability of each shadow block is also programmable.

256KB Relocation

The SiS85C401 provides the 256KB DRAM relocation from OAOOOO-OBFFFFh and ODOOOOOEFFFFh to the top of configurated DRAM size.

This function works for the DRAM sizes of IMB, 2MB, 4MB, 6MB and 8MB when the shadowing of segments D and E is disabled.

ROM Support

The SiS85C401 provides a chip select signal for the system BIOS ROM. The memory space assigned to the ROM is the highest 64/128KB of the real (IMB) and the protected (4GB) address modes of the 80486.

The system BIOS ROM can be shadowed by the DRAM to improve performance. When the shadow RAM is turned on, the access to system BIOS with address below lOOOOOh will be channeled to the DRAM.

Fast A20GATE And CPU Reset

In the original PC/AT design, the A20GATE and CPU Reset (RC) are controlled by the 8042 keyboard controller to switch the 80286 CPU between the real and protected address modes. The operation of 8042 is quite slow so if the address mode switching happens frequently, the program execution speed will be affected.

The SiS85C401 provides a 8042 emulation to generate the A20GATE and CPU reset in hardware ,This feature is software transparent.

Local Bus Support

The SiS85C401 uses LBD# and LRDYI# pins to support local bus devices suchas Weitek 4167. The interface protocol is very straightforward.

When a local bus device decodes the bus definition/address from 486 CPU and finds this is its cycle at the start of a CPU bus cycle, it should assert LBD# to inform the SiS85C401 this is a local bus device cycle. The SiS85C401 will not send ATCYC# to the SiS85C402 but will wait for LRDYI# to terminate current cycle. When the local bus device want to finish its bus cycle, it should send a LRDYI# pulse to the SiS85C401. The SiS85C401 will synchronize LRDYI# with CPUCLK then send a RDY# to CPU. The local bus device should monitor the RDY# to know when the bus cycle is exactly finished.

When there are more than one local bus devices, their LBD# and LRDYI# signals should be ANDed together then sent to the SiS85C401.

T he SiS85C40 1 samples the LBD# input at the end of T2 when DRAM speed is set to FASTEST or FASTER, and at the end of T3 when DRAM speed is SLOWER or SLOWEST. LBD# should be asserted before the sampling point and kept active till RDY# is asserted.

Turbo Switch

The 80486 can run over 10 times faster than the original PC/AT. But some old applications may get into trouble if the system speed is too fast. The SiS85C401 offer a de-turbo function that can be controlled through a hardware switch or software

programming. When the deturbo function is turned on, the SiS85C401 disables both the 80486 internal and secondary caches, which decreases the system speed to approximately 1/4 of that of the normal speed.

Configuration Registers

There are eight configuration registers inside the SiS85C401. An indexing scheme is used to access all the registers. Port 22h is the index register and port 23h is the data register. T he conhguration registers are accessed by hrst writing the index to port 22h and immediately followed by a read or a write to port 23h. The index is reset aher data access. Every data access to port 23h must be preceded by an index write to port 22h, even if the same register is being accessed. All the reserved bits should be set to zero for future compatibility purpose. The contents of the registers are listed as follows.

SiS85C401 **Conflguration Registers**

Reglster 60 (index 60) Defaull = 00

bit 7,6 DRAM Speed
00: Slowest (50MHz)
01: Slower (40MHz)
10: Faster (33MHz)
11: Fastest (25MHz)

Bit 7 also defines the first cache read cycle time of a burst: 0/1: 3T/2T

bit 5 DRAMWrite CAS PulseWidth
0:2T (~40.50)
1: 1T (33,25,20)

bit 4 -0 DRAM Size Configuration

	Bank-0	Bank-1	Bank-2	Bank-3	Total Main Memory
00000	1 M				1 MB
·00001	1 M	1 M			2MB
00010	1M	1M	2M		4MB
00011	1 M	1 M	4M		6MB
00100	1M	1M	2M	4M	8MB
·00101	1M	1M	4M	4M	10MB
00110	1M	1M	16M		18MB
00111	2M				2MB
0100	2NI	2M			4MB
01001	2M	4M			6MB
01010	2M	2M	4M		8MB
·01011	2M	2M	4M	4M	12MB
01100	2M	16M			18MB
01101	2M	2M	16M		20MB
01110	2M	2M	4M	16M	24MB
·01111	2M	2M	1 6M	1 6M	36MB
10000	4M				4MB
·10001	4M	4M			8MB
10010	4M	4M	4M		12MB
·10011	4M	4M	4M	4M	16MB
10100	4M	16M			20MB
10101	4M	4M	16M		24MB
10110	4M	16M	16M		36MB
·10111	4M	4M	16M	16M	40MB
11000	8M				8MB
·11001	8M	8M			16MB
11010	8M	8M	8M		24MB
·11011	8M	8M	8M	8M	32MB
11100	1 6M				1 6MB
·11101	16M	16M			32MB
11110	16M	16M	16M		48MB
·11111	16M	16M	16M	16M	64MB

Note:
1 MB= 256K x 36bits
2MB= 512K x 36bits
4MB= 1 M x 36bits
8MB= 2M x 36bits
1 6MB= 4M x 36bits

· DRAM InterleaveApplicable

Reglster 61 (index 61) Default = 00

bit 7 Cache Enable
0: Disable
1: Enable

bit 6 Wrlte Back Enable
0: Disable (Write Through)
1: Enable (Write Back)

bit 5,4 Cache Size
00: 32KB
0 1: 64KB
10: 1 28KB
11: 256KB and above

bit 3 Cache Interleave Enable
0: Disable
1: Enable

bit 2 DRAM Interleave Enable (for 2/4 banks only)
0: Disable
1: Enable
bit 1 Reserved
bit 0 Reserved

Register 62 (index 62) Default = 00

bit 7 Shadow RAM Read Enable
0: Disable
1: Enable
bit 6 Shadow RAMWrite Protection Enable
0: Disable
1: Enable
bit 5 E8000h-EFFFFh Shadow RAM Enable
bit 4 E0000h-E7FFFh Shadow RAM Enable
bit 3 D8000h-DFFFFh Shadow RAM Enable
bit 2 D0000h-D7FFFh Shadow RAM Enable
bit 1 C8000h-CFFFFh Shadow RAM Enable
bit 0 C0000h-C7FFFh Shadow RAM Enable

Reglster 63 (index 63) Defaulat = 00

bit 7 System BIOS ROM Size
0: 64K
1: 128K

bit 6 F0000h-FFFFFh Shadow RAM Cacheable

bit 5 E8000h-EFFFFh Shadow RAM Cacheable

bit 4 E0000h-E7FFFh Shadow RAM Cacheable

bit 3 D8000h-DFFFFh Shadow RAM Cacheable

bit 2 D0000h-D7FFFhShadow RAM Cacheable

bit 1 C8000h-CFFFFh Shadow RAM Cacheable

bit 0 C0000h-C7FFFh Shadow RAMCacheable

Register 64 (index 64) Default=00

bit 7 Allocation of Non-Cacheable Area#1
0. Local DRAM
1 AT Bus, local DRAM is disabled

bit 6 4 Size of Non-Cacheable Area #1 (within 16 MB)
000: 0KB disabled)
001: 64KE
010: 1 28KB
011: 256KB
100: 51 2KB
101: 1 MB
110: 2MB
111:4MB

bit 3 Allocation of Non-CacheableArea#2
0: Local DRAM
1: AT Bus, local DRAM is disabled

bit 2-0 Size of Non-Cacheable Area #2 (within 64 MB)
000: OKB (disabled)
001: 64KB
010: 1 28KB
011 . 256KB
100 512KB
101: 1MB
11 0. 2MB
111 4MB

Register 65 (index 65) Default = 00

bit 7-0 A23-Al 6 of Non-Cacheable Area #1 (within 16 **MB)**

Register 66 (index 66) Default=00

bit 7-0 A23-A16 of Non-Cacheable Area #2 (within 64 **MB)**

Reglster 67 (index 67) Default=00

bit 7, 6 A25 and A24 of Non-Cacheable Area #2

bit 5 GATE A20 Emulation Enable
0: Disable
1: Enable
bit 4 Fast Reset Emulation Enable
0: Disable
1: Enabl

bit 3 Fast Reset Latency Control
0: 2us
1: 6us

bit 2 Slow Refresh Enabled (1:4)
0: Normal Refresh
1: Slow Refresh

bit 1 De-Turbo ON/OFF
0: Turbo
1: De-Turbo

bit 0 TurboSwitch Enable
0: Always Turbo, ignores the status of Turbo switch
1: Turbo Switch enable

Register 68 (index 68) Default = 00

bit 7 Super Fast DRAM Access Enable
0: Disable 1: Enable
This function is valid only when
a. DRAM speed is set onto FASTEST and
b. 2nd cache is disabled.

bit 6 Slow CPU (below 25MHz) Enable
0: Disable 1: Enable
This function is valid only when
DRAM speed is set onto FASTEST
This bit optimizes DRAM timing for <25MHz system.
Trcd 2T –> 1T (RAS-to-CAS delay)
Trp 3T –> 2T (RAS precharge time)

bit 5,4 Proprietary Chip Select (pin 149)
00: Port E8 - EFh
01 : Port C8 - CFh
10 : Port 28 - 2Fh
11: Turbo Indicator

blt 3,2,1,0 reservd and should be written with zero.