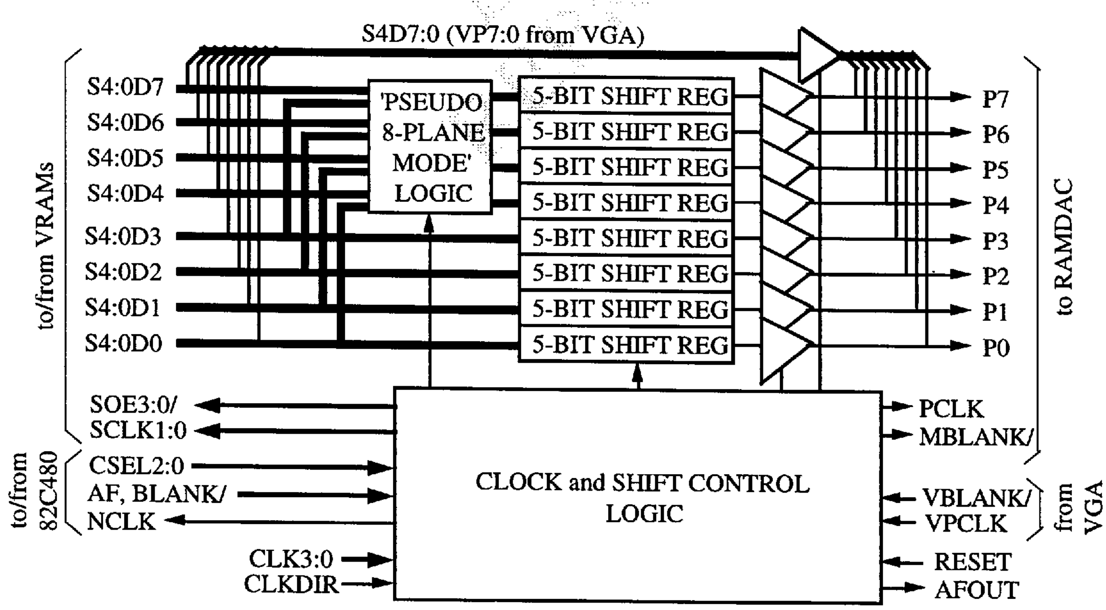
82B484
VIDEO SUPPORT CHIP

- Allows an 8514/A-compatible display adapter to be implemented with 9 chips (including memory):

  1 82C480 Graphics Controller
  1 82B484 Video Support Chip
  1 74LS245 Bus Transceiver
  1 RAMDAC
  1 LM339 Comparator
  4 256Kx4 VRAMs (minimum)
  +1 EPROM (optional)

- Reduces chip count for 82C480 based 8514/A-compatible display adapters
- Supports video rates to 80 MHz
- Supports the 82C403 Clock Chip or up to four discrete oscillators
- Contains VGA Video pass-through circuitry
- Implements VESA-compatible video pass through logic
- High-speed Bi-CMOS process
- Pinouts optimized for PCB layout
- 80-pin Plastic Flat Package

Designed to work with the 82C480, the 82B484 Video Support Chip integrates all TTL components required for 8514/A-compatible display adapters. With the 82B484, a minimum system 1024x768 non-interlaced 8514/A-compatible display adapter can be implemented in 9 chips including VRAM memory. Included in the 82B484 is all clock selection circuitry, video shift registers, and VGA video pass through logic. The 82B484 CMOS circuitry allows 80 MHz clock frequencies supporting non-interlaced monitor resolutions up to 1024x768 and interlaced monitor resolutions up to 1280x1024.



82B484 Block Diagram

Revision History

Revision	Date	By	Comment
1.3	5/20/90	DR	Document updated to reflect Rev. 1 Silicon.
1.4	6/20/90	ST	Changed document font to Chips Standard Data Sheet font.
1.5	7/12/90	DR & ST	Document released with arrival of Rev. 1 Silicon.
1.6	1/25/91	DR	Interface Timing - miscellaneous format correction.
1.7	4/26/91	DR	Revised AC and DC parameters based on characterization.
2.0			

Table of Contents

List of Figures and Tables

Introduction

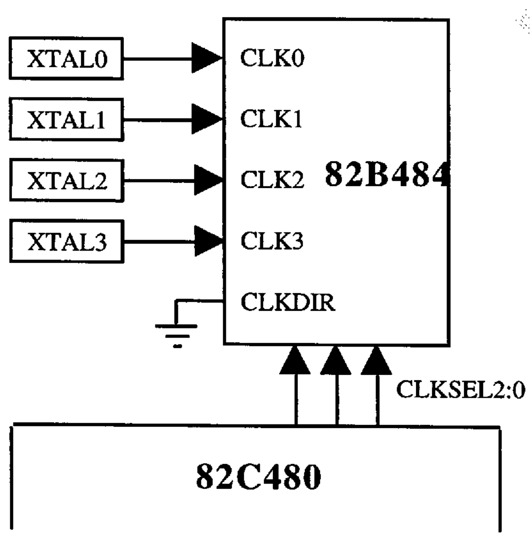
Video Subsystem Total Chip Count

Using the 82C480 and 82B484, a complete 8514/A-compatible 8-bit video subsystem can be built with just 9 ICs (10 ICs for a 16-bit system), including display memory, as shown in the table below:

Qty	Chip Type
1	82C480 Graphics Controller Chip
1	74LS245 Transceiver (2 for 16-bit interface)
1	IMSG176-65 or IMSG178-65 RAMDAC
1	LM339 Comparator
4	256Kx4 VRAM (120 ns) (+4 for 8 planes)
1	82B484 Video Support Chip
9	Total
+1	27256 POST ROM (optional)

Additional components required are 25.175, 32, 44.900, and 65.000 MHz oscillators, 15-pin video connector, LM334 Current reference, 1N4148 diode, and various resistors and capacitors. The indicated configuration supports 640x480 non-interlaced 16-color and 256-color modes and 1024x768 interlaced and non-interlaced 16-color mode.

The 82B484 is capable of interfacing directly to four crystal oscillators or may be configured to interface to a clock synthesis chip selecting from up to eight frequencies.

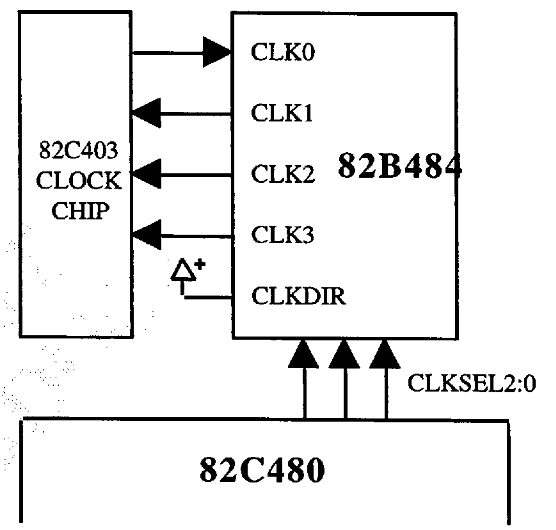


82B484 Crystal Oscillator Interface

Adding 256-color support for 1024x768 would require four additional 256Kx4 VRAM chips.

Adding support for 1280x1024 interlaced would require an additional oscillator (80 MHz), a '-80' RAMDAC, and a total of 5 VRAMs (16-color) or 10 VRAMs (256-color).

The same video subsystem configured for the MCA bus with a 'Power-On-Self-Test' (POST) ROM would require two additional 8-bit address latches (74LS373 or equivalent).



82B484 Clock Chip Interface

Package

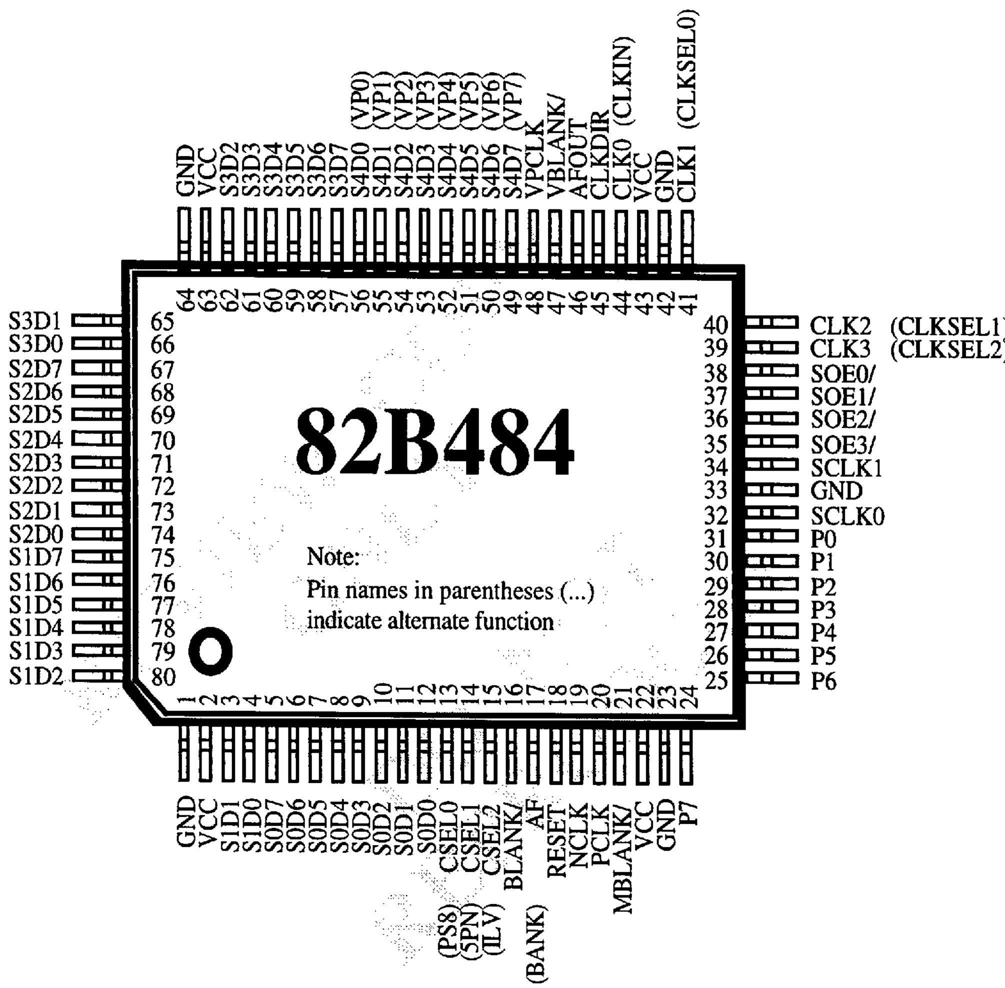
The 82B484 is available in a 80-pin plastic flat pack (PFP).

Complete descriptions of all 82B484 pins are included in this document.

The pins are separated into the following logical groups for discussion: 82C480 Interface, Video, Clock, Power, and Ground.

PAGE(S) INTENTIONALLY BLANK

82B484 Pinouts



82B484 Pin List

Pin Name	Pin #
AF	17
AFOUT	46
BLANK/	16
CLK0 (CLKIN)	44
CLK1 (CLKSEL0)	41
CLK2 (CLKSEL1)	40
CLK3 (CLKSEL2)	39
CLKDIR	45
CSEL0 (PS8)	13
CSEL1 (5PN)	14
CSEL2 (ILV)	15
GND	1
GND	23
GND	33
GND	42
GND	64
MBLANK/	21
NCLK	19
P0	31
P1	30
P2	29
P3	28
P4	27
P5	26
P6	25
P7	24
PCLK	20

Pin Name	Pin #
RESET	18
S0D0	12
S0D1	11
S0D2	10
S0D3	9
S0D4	8
SOD5	7
S0D6	6
S0D7	5
SOE0/	38
S0E1/	37
SOE2/	36
S0E3/	35
S1D0	4
S1D1	3
SCLK0	32
SCLK1	34
S1D2	80
S1D3	79
S1D4	78
S1D5	77
S1D6	76
S1D7	75
S2D0	74
S2D1	73
S2D2	72
S2D3	71

Pin Name	Pin #
S2D4	70
S2D5	69
S2D6	68
S2D7	67
S3D0	66
S3D1	65
S3D2	62
S3D3	61
S3D4	60
S3D5	59
S3D6	58
S3D7	57
S4D0 (VPO)	56
S4D1 (VP1)	55
S4D2 (VP2)	54
S4D3 (VP3)	53
S4D4 (VP4)	52
S4D5 (VP5)	51
S4D6 (VP6)	50
S4D7 (VP7)	49
VBLANK/	47
VCC	2
VCC	22
VCC	43
VCC	63
VPCLK	48

82B484 PIN DESCRIPTIONS

Serial Data

Pin #	Pin Name		Type	Active	Description
49	S4D7	(VP7)	In	High	Serial data from VRAMs. Named SxDy, where x is the pixel location in the nugget (see 82C480 Data Sheet) and y is the bit position (plane) in the pixel. The 82B484 latches the SxDy inputs and shifts them out serially on the P7:0 bus.
50	S4D6	(VP6)	In	High	
51	S4D5	(VP5)	In	High	
52	S4D4	(VP4)	In	High	
53	S4D3	(VP3)	In	High	
54	S4D2	(VP2)	In	High	
55	S4D1	(VP1)	In	High	The 82C480 serial data path will only use S4D7:0 in systems implementing 5 pixel nuggets. In 4 pixel nugget systems S4D7:0 may be used to multiplex VGA video data over the P7:0 bus. This VGA video is transmitted over the VESA (Video Electronics Standards Association) video pass-through connector, and may have a frequency up to 65 MHz, supporting all VGA modes up to 1024x768 non-interlaced. In 5 pixel nugget systems, VGA video data must be multiplexed externally (see AFOUT pin description).
56	S4D0	(VP0)	In	High	
57	S3D7		In	High	
58	S3D6		In	High	
59	S3D5		In	High	
60	S3D4		In	High	
61	S3D3		In	High	
62	S3D2		In	High	
65	S3D1		In	High	
66	S3D0		In	High	
67	S2D7		In	High	
68	S2D6		In	High	
69	S2D5		In	High	
70	S2D4		In	High	
71	S2D3		In	High	
72	S2D2		In	High	
73	S2D1		In	High	
74	S2D0		In	High	
75	S1D7		In	High	
76	S1D6		In	High	
77	S1D5		In	High	
78	S1D4		In	High	
79	S1D3		In	High	
80	S1D2		In	High	
3	S1D1		In	High	
4	S1D0		In	High	
5	S0D7		In	High	
6	S0D6		In	High	
7	S0D5		In	High	
8	S0D4		In	High	
9	S0D3		In	High	
10	S0D2		In	High	
11	S0D1		In	High	
12	S0D0		In	High	

82B484 PIN DESCRIPTIONS

Pin #	Pin Name		Type	Active	Description
45	CLKDIR		In	High	Clock direction control: 0=internal clock multiplexing, 1=external (default). This pin has an internal pullup.
44 41 40 39	CLK0 CLK1 CLK2 CLK3	(CLKIN) (CLKSEL0) (CLKSEL1) (CLKSEL2)	In I/O I/O I/O	High High High High	If CLKDIR is sampled low on the falling edge of RESET, the CLK0-3 pins are inputs for the following recommended clock frequencies: **Input / Frequency / Resolution** CLK0 25.175 MHz 640x480 non-interlaced CLK1 44.900 MHz 1024x768 interlaced CLK2 65.000 MHz 1024x768 non-interlaced CLK3 80.000 MHz 1280x1024 interlaced If CLKDIR is sampled high at the falling edge of RESET (default), CLK0 becomes the input for all clock frequencies (80 MHz maximum frequency), and CLK1-3 become latched clock select outputs for control of an external clock multiplexer or clock synthesizer.
15 14 13	CSEL2 CSEL1 CSEL0	(ILV) (5PN) (PS8)	In In In	High High High	These pins serve two functions: when BLANK/ = 0 they select the clock source; when BLANK/ = 1 they select VRAM configuration modes: **2 1 0 BLANK/ = 0** 0 0 0 CLK0 (25.175 MHz) 0 0 1 CLK1 (44.900 MHz) 0 1 0 CLK2 (65.000 MHz) 0 1 1 CLK3 (80.000 MHz) **2 1 0 BLANK/ = 1** x x 1 PS8 (Pseudo 8-plane) mode x 1 x 5PN (5 pixel nugget) mode 1 x x Interleave mode (see AF pin)

CSEL2:0 are latched by the rising edge of NCLK, and BLANK/ is synchronous to the rising edge of NCLK, so all changes of CLKSEL are synchronous to NCLK.

If one bank of VRAM is used per scan line, only four pixels are provided to the serial data logic each SCLK cycle; therefore either SCLK0 or SCLK1 run at 1/4 PCLK, as determined by BANK (see table under AF pin description).

If two or four banks of VRAM are used, bank 0 is horizontally interleaved with bank 1, and bank 2 is horizontally interleaved with bank 3. SCLK0 clocks banks 0 and 2; SCLK1 clocks banks 1 and 3. In this case SCLK0 and SCLK1 run 180° out of phase, at 1/8 PCLK frequency. The 82C480 provides serial output enables for each bank (SOE3:0/) so that serial outputs of all banks may be bused to the 82B484 SxDy pins.

Entering VGA mode (i.e. exiting AF mode) will not affect NCLK or SCLK1:0, but PCLK will change to the VGA PCLK frequency. Entering PS8 mode will not affect PCLK or NCLK frequency, but SCLK1:0 frequency will double. Entering 5PN mode will change NCLK from 1/8 to 1/10 PCLK frequency (and change SCLK1:0 from 1/4 to 1/5 PCLK or 1/8 to 1/10 PCLK) but not affect PCLK.

82B484 PIN DESCRIPTIONS

Clocks

Pin #	Pin Name	Type	Active	Description
20	PCLK	Tri-O	High	Pixel clock (to palette DAC). 80 MHz max.
19	NCLK	Tri-O	High	Double Nugget clock (to 82C480). 1/8 or 1/10 PCLK rate, depending on 5PN. NCLK is the basis for HSYNC, VSYNC, BLANK/, RAM refresh, and Data Transfer timings.
34 32	SCLK1 SCLK0	Out Out	High High	Serial Clocks to VRAMs. If only one bank is used, either SCLK0 or SCLK1 runs at 1/4 (or 1/5) PCLK. If two or four banks are used, SCLK0 and SCLK1 are two-phase clocks, running at 1/8 (or 1/10) PCLK, and control banks 0 and 2, or 1 and 3, respectively.
35 36 37 38	SOE3/ SOE2/ SOE1/ SOE0/	Out Out Out Out	Low Low Low Low	Serial Output Enables to VRAM banks 0-3.
48	VPCLK	In	High	VGA Pixel Clock. From MCA Video Bus Extension or VESA Video Pass-Through connector. VPCLK is only required if VGA pixel data and blanking are multiplexed with 82C480 pixel data and blanking internally (see AFOUT pin description).

82B484 PIN DESCRIPTIONS

Video, Power, and Ground

Pin #	Pin Name	Type	Active	Description
16	BLANK/	In	Low	Blank input from 82C480.
47	VBLANK/	In	Low	Blank input from VGA.
21	MBLANK/	Tri-O	Low	Blank output to monitor, selected from BLANK/ or VBLANK/.
24	P7	Tri-O	High	Pixel bus (to palette/DAC). If AFOUT = 1 on reset, P7:0 are tristated when in VGA mode. P7:0 are also tristated when RESET = 1.
25	P6	Tri-O	High	
26	P5	Tri-O	High	
27	P4	Tri-O	High	
28	P3	Tri-O	High	
29	P2	Tri-O	High	
30	P1	Tri-O	High	
31	P0	Tri-O	High	
18	RESET	In	High	Tristates pins, resets internal toggle flip-flops for chip test, and latches state of AFOUT (falling edge).
17	AF (BANK)	In	High	Advanced Function input from 82C480. AF is latched by the rising edge of NCLK. If BLANK/ = 0, AF = 1 indicates Advanced Function mode and AF = 0 indicates VGA mode; if BLANK/ = 1, AF indicates BANK, as shown in the table below:
46	AFOUT	I/O	High	Advanced Function output. AFOUT is an input during RESET. At the falling edge of RESET, if AFOUT is high (default), P7:0 will tristate when in VGA mode to allow busing VGA pixel data to the palette. If AFOUT is low at the falling edge of RESET, VGA pixel data is input over S4D7:0 and multiplexed internally.
2	VCC	In	--	Power
22	VCC	In	--	
43	VCC	In	--	
63	VCC	In	--	
1	GND	In	--	Ground
23	GND	In	--	
33	GND	In	--	
42	GND	In	--	
64	GND	In	--	

AF (BANK) table:

ILV	BANK	Result
0	0	Display data from bank 0
0	1	Display data from bank 1
1	0	Display data from banks 0 and 1
1	1	Display data from banks 2 and 3

If INTERLEAVE (ILV) =1 (see CSEL2), data is multiplexed between banks on a nugget-by-nugget basis. SOE3:0/ are alternately activated, so serial outputs from all banks may be bused together.

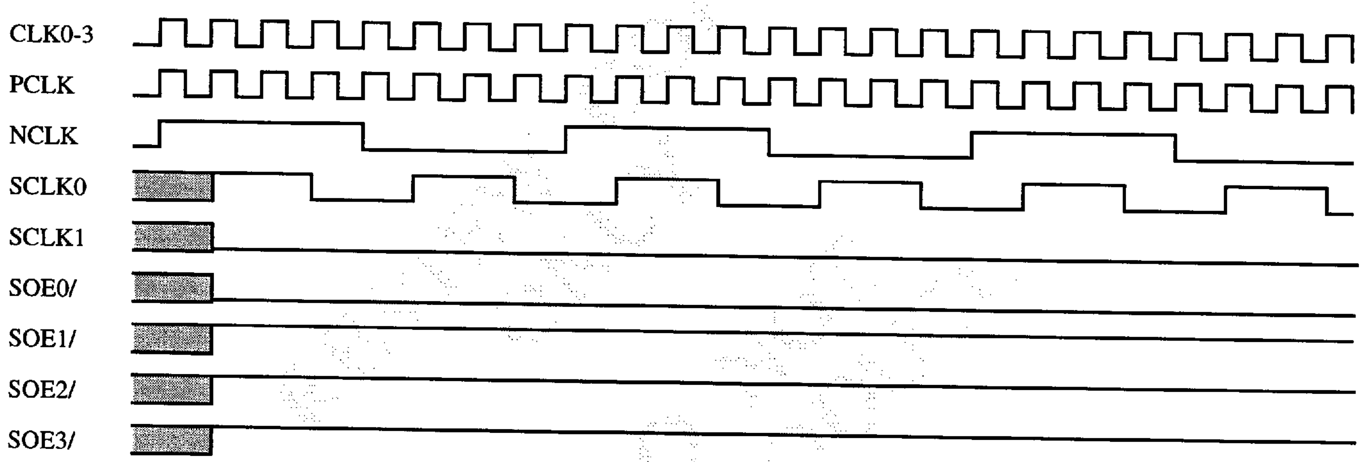
82B484 Functional Description

The clock section of the 82B484 produces the following outputs from CLK0, CLK1, CLK2, or CLK3 based on the control inputs 5PN, ILV (INTERLEAVE), PS8, and BANK:

1) Pixel Clock (PCLK)
2) Nugget Clock (NCLK)
3) VRAM shift output enables (SOE0:3/)
4) VRAM shift clocks (SCLK0:1)

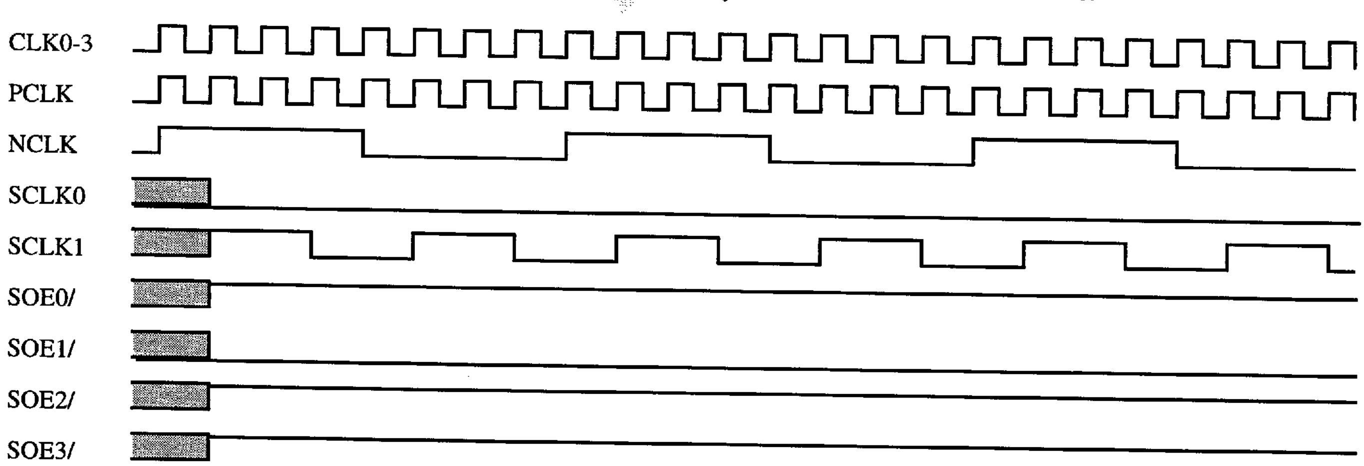
5PN=0, ILV=0, PS8=0, BANK=0

Standard Operating mode for 1 bank 4/8 VRAM configuration.



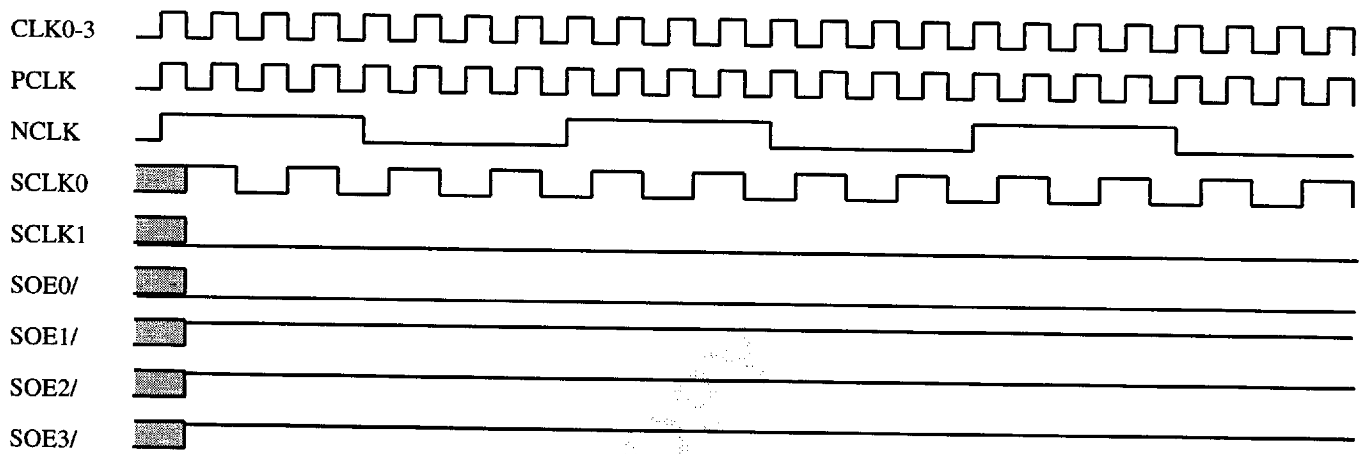
5PN=0, ILV=0, PS8=0, BANK=1

This mode is not accsessible from the 82C480 since it always interleaves 2 or more banks.



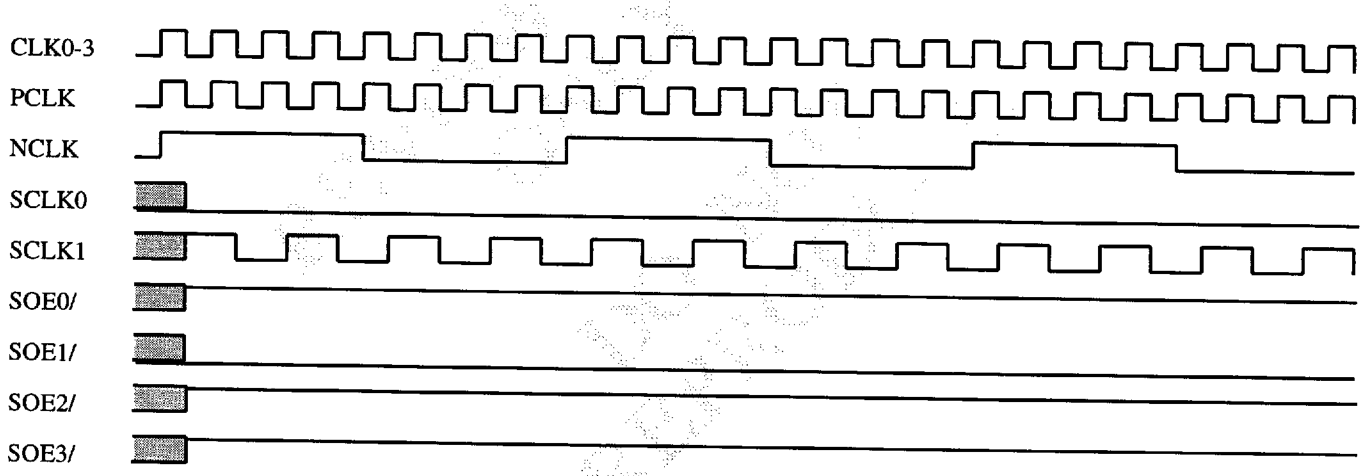
5PN=0, ILV=0, PS8=1, BANK=0

Pseudo 8 plane mode.



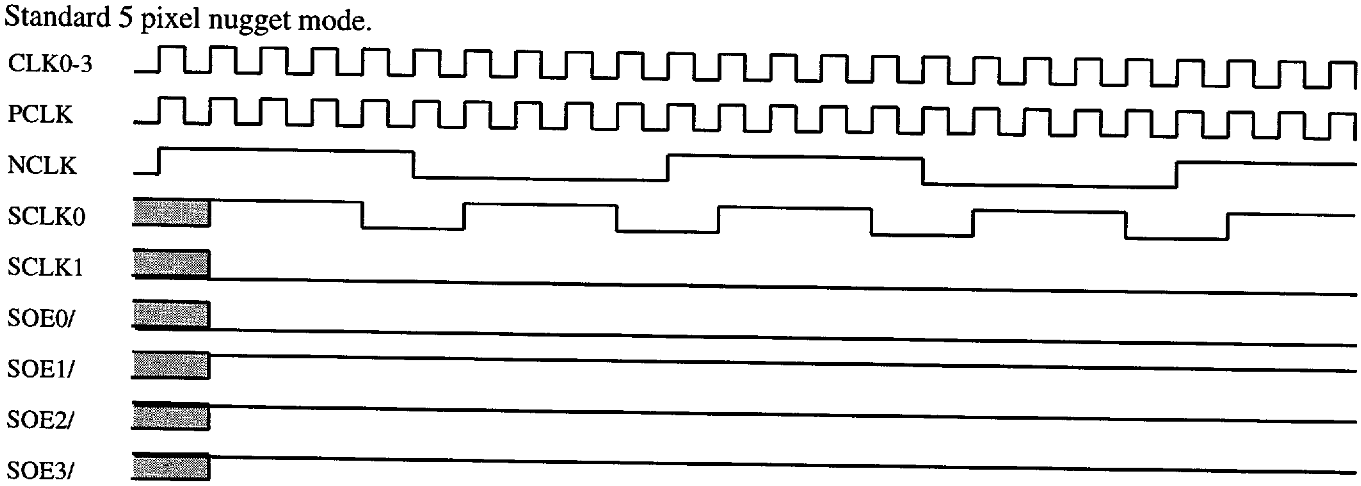
5PN=0, ILV=0, PS8=1, BANK=1

Not accessible from 82C480.



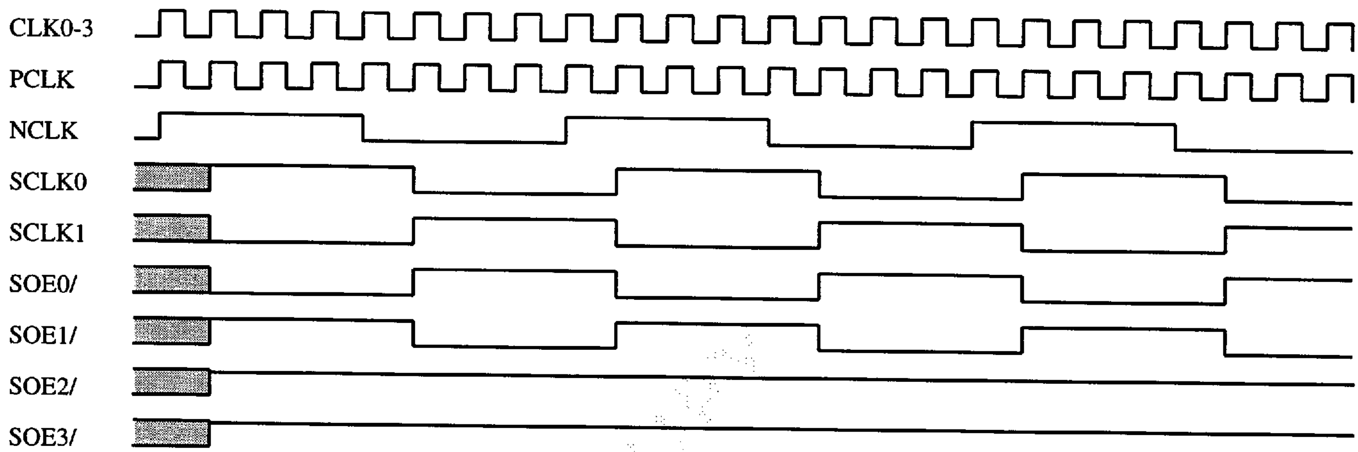
5PN=1, ILV=0, PS8=0, BANK=0

Standard 5 pixel nugget mode.



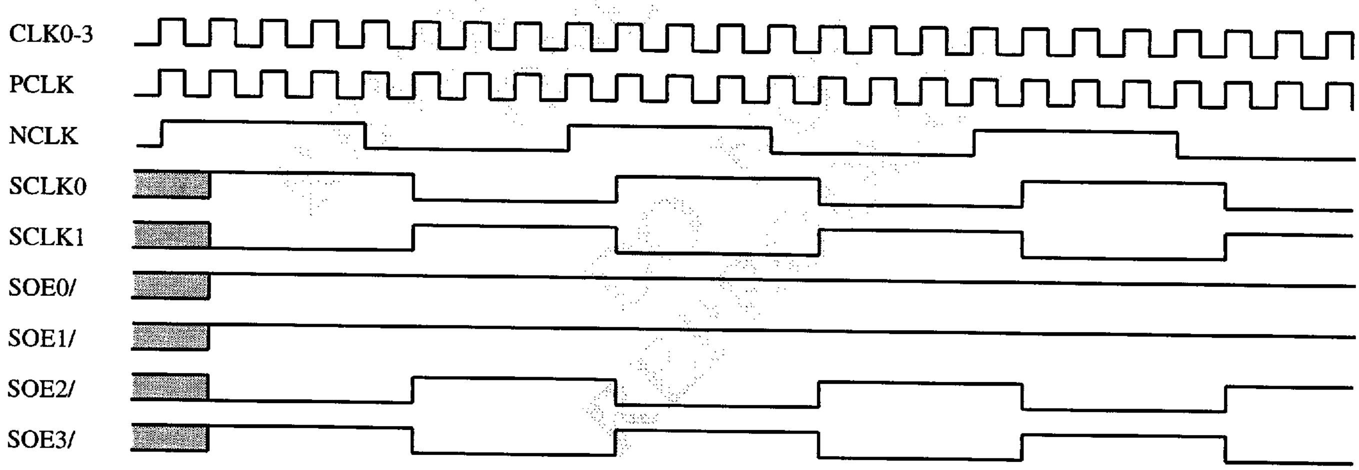
5PN=0, ILV=1, PS8=0, BANK=0

Standard 2 bank mode (Horizontal interleaving). Also, used in 4 bank configurations.



5PN=0, ILV=1, PS8=0, BANK=1

Verticaly interleaved with the previous mode in 4 bank configurations



2098116 0011318 327

PAGE(S) INTENTIONALLY BLANK

2098116 0011319 263

82B484 Electrical Specifications

82B484 ABSOLUTE MAXIMUM CONDITIONS

Symbol	Parameter	Min	Max	Units
P_D	Power Dissipation	–	1.0	W
V_{CC}	Supply Voltage	–0.5	7.0	V
V_I	Input Voltage	–0.5	V_{CC}+0.5	V
V_O	Output Voltage	–0.5	V_{CC}+0.5	V
T_{OP}	Operating Temperature (Ambient)	–25	85	°C
T_{STG}	Storage Temperature	–40	125	°C

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Normal Operating Conditions.

82B484 NORMAL OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	4.5	5.5	V
T_A	Ambient Temperature	0	70	°C

82B484 DC CHARACTERISTICS

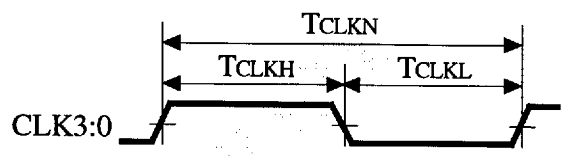
All output pins are tristated when RESET=1.
All input and output voltages are TTL compatible.

Symbol	Parameter	Notes	Min	Max	Units
I_{IH}	High Input Current	V_I = 2.7V, VCC = 5.5V	–	20	uA
I_{IL}	Low Input Current	V_I = 0.4V, VCC = 5.5V (AFOUT)	–	–600	uA
		V_I = 0.4V, VCC = 5.5V (all other inputs)	–	–20	uA
I_{OZ}	Output Leakage	V_I = 2.7V, VCC = 5.5V	–	±20	uA
V_{IH}	Input High Voltage	I_{IH} = 20uA (CLK3:0	2.8	VCC+0.5	V
		I_{IH} = 20uA (all other pins)	2.0	VCC+0.5	V
V_{IL}	Input Low Voltage	I_{IL} = –20uA	–0.5	0.8	V
V_{OH}	Output High Voltage	I_{OH} = 1 mA (all pins)	2.5	–	V
V_{OL}	Output Low Voltage	I_{OL} = 16mA (SCLK1:0)	–	0.5	V
		I_{OL} = 8mA (all others)			

82B484 AC CHARACTERISTICS (under normal operating conditions)*
($T_A = 0° C$ to $70° C$, $V_{CC} = 5V \pm 5\%$)

82B484 Video Clock Timing

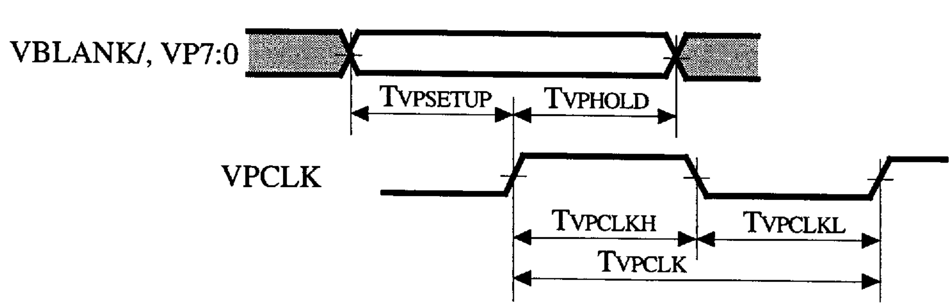
Symbol	Parameter	Min	Max	Units
T_{CLKN}	Clock Cycle Time, CLK3:0	12.5	–	nS
T_{CLKH}	Clock High Time, CLK3:0 ($V_{IH} = 2.8V$)	4	–	nS
T_{CLKL}	Clock Low Time, CLK3:0 ($V_{IL} = 0.8V$)	4	–	nS



82B484 Video Clock Cycle

82B484 VGA Pass-Through Timing

Symbol	Parameter	Min	Max	Units
T_{VPCLK}	VGA Clock Cycle Time (65MHz Maximum)	15	–	nS
T_{VPCLKH}	VGA Clock High Time	4	–	nS
T_{VPCLKL}	VGA Clock Low Time	4	–	nS
$T_{VPSETUP}$	Setup Time: VP7:0, VBLANK/ to VGA Clock	3	–	nS
T_{VPHOLD}	Hold Time: VP7:0, VBLANK/ from VGA Clock	3	–	nS



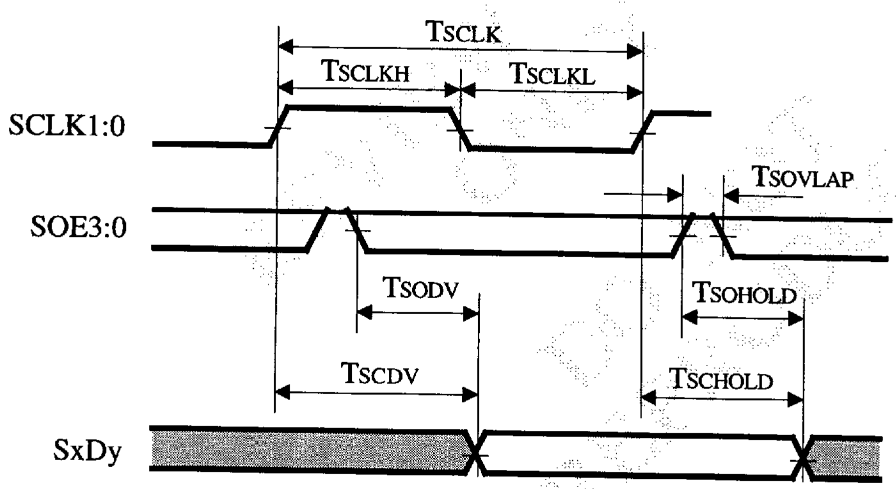
82B484 Pass-Through Timing

* AC parameters normal conditions are $V_{IH} = 2.0V$, $V_{IL} = 0.8V$, 50pF load capacitance.

82B484 Serial Data Timing

Symbol	Parameter	Min	Max	Units
T_{SCLK}	Serial Clock Cycle Time	50	–	nS
T_{SCLKH}	Serial Clock High Time	20	–	nS
T_{SCLKL}	Serial Clock Low Time	22	–	nS
T_{SCDV}	Serial Clock to Serial Data Valid	–	$T_{SCLK} - 12$*	nS
	Psuedo 8 - Plane Mode	–	$T_{SCLK} - 16$	nS
T_{SODV}	Serial Output Enable to Serial Data Valid	–	$T_{SCLK} - 16$	nS
	Psuedo 8 - Plane Mode	–	$T_{SCLK} - 20$	nS
T_{SCHOLD}	Serial Data Hold from SCLK High	5	–	nS
T_{SOHOLD}	Serial Data Hold from SOE High	2	–	nS
T_{SOVLAP}	Serial Output Enable Non-Overlap Time	0	–	nS

* For 80MHz Operation, 100ns VRAM's are required.



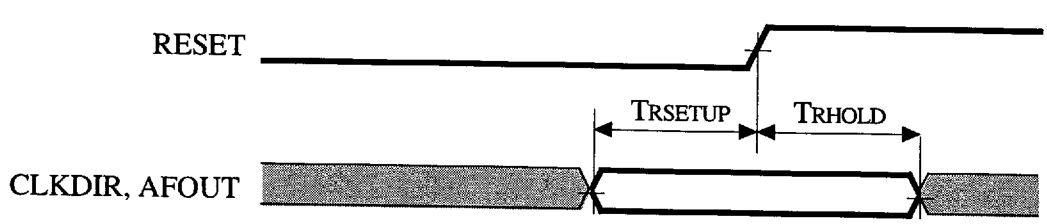
SCLK frequency compared to PCLK:

ILV	PS8	5PN=0	5PN=1
1	0	1/8	1/10
1	1	1/4	1/5
0	0	1/4	1/5
0	1	1/2	2/5

82B484 Serial Data Timing

82B484 Reset Timing (for loading programming options)

Symbol	Parameter	Min	Max	Units
T_{RSETUP}	Setup Time: AFOUT, CLKDIR to RESET	10	–	nS
T_{RHOLD}	Hold Time: AFOUT, CLKDIR from RESET	3	–	nS



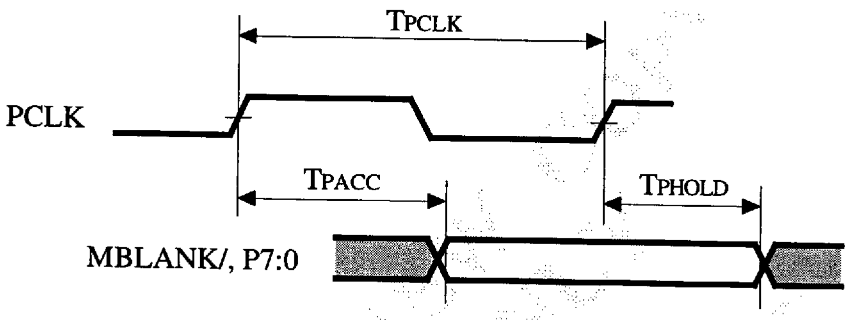
82B484 Reset Timing

2098116 0011322 858

82B484 Palette Timing

Symbol	Parameter	Note	Min	Max	Units
T_{PCLK}	Pixel Clock Cycle Time*	AF = 1	12.5	–	nS
		VGA Pass Through	15	–	nS
T_{PACC}	Access Time: P7:0, MBLANK/ from Pixel Clock*	AF = 1	–	9.5	nS
		VGA Pass Through	–	10.5	nS
T_{PHOLD}	Hold Time: P7:0, MBLANK/ from Pixel Clock*	AF = 1	3	–	nS
		VGA Pass Through	3	–	nS

* Note: High speed video outputs are tested driving a single CMOS input buffer at 80MHz. Typical load value is 15pF.

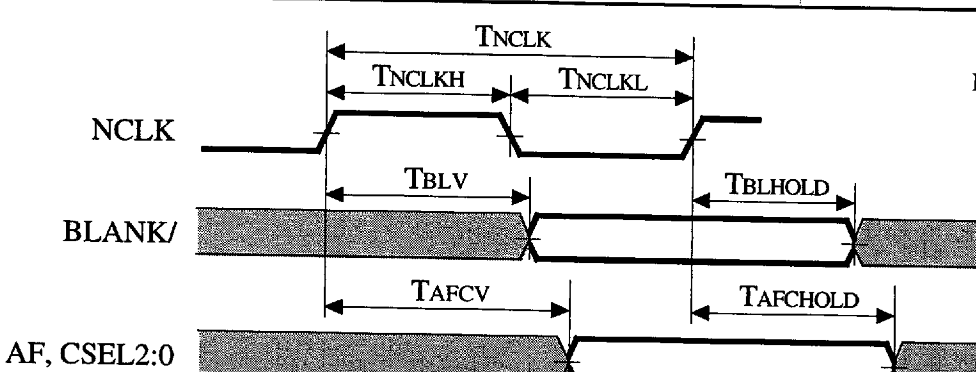


Note: PCLK frequency is derived from CLK3:0,CLKIN, or VPCLK as determined by CSEL2:0 and AFOUT.

82B484 Palette Timing

82B484 Interface Timing

Symbol	Parameter	Min	Max	Units
T_{NCLK}	Nugget Clock Cycle Time	100	–	nS
T_{NCLKH}	Nugget Clock High Time	45	–	nS
T_{NCLKL}	Nugget Clock Low Time	47	–	nS
T_{BLV}	Nugget Clock to Blank Valid	–	$4T_{PCLK} - 18$	nS
T_{AFCV}	Nugget Clock to AF, CSEL Valid	–	$4T_{PCLK} - 18$	nS
T_{BLHOLD}	Blank Hold from NCLK High	2	–	nS
$T_{AFCHOLD}$	AF, CSEL Hold from NCLK High	2	–	nS



Note: NCLK frequency is 1/8 (four-pixel nugget) or 1/10 (five-pixel nugget) PCLK frequency.

82B484 Interface Timing

82B484 Mechanical Specifications