12. REVISION UPDATES

Rev.1.1 to Rev.2.0 Updates

NO.	Rev.1.1	Rev.2.0
1	Supports DRAM 32 bits/64 bits mixed mode configuration (Page 2)	This function does not work in 5571 A version. It will be fixed in B version.
2	Supports Automatic Power Supply Control (Page 3)	This function does not work in 5571 A version. It will be fixed in B version.
3	Universal Serial Bus Controller (Page 4)	This function does not work in 5571 A version. It will be fixed in B version.
4	0.6 um CMOS Technology. (Page 4)	0.5 um CMOS technology
5	Register 50h Bit 4 Reserved (Page 21)	Do not program it.
6	Register 50h Bit 3 Write Merge (Page 21)	Recommend “1” for 66Mhz “0” for 75Mhz
7	Register 50h Bit 2 Reserved (Page 21)	Read Write Reorder for DRAM arbiter “1” for 66Mhz “0” for 75Mhz
8	Register 50h Bits 1:0 Reserved (Page 21)	These bits should be programmed to “0”.
9	Register 52h Bit6 Reserved (Page 22)	Register 52h Bit6 Turbo Read 1: for Intel Pentium ; 0: for Cyrix 6X86
10	Register 52h Bit5 Read FIFO (Page 22)	Register 52h Bit5 Reserved This bit should be always programmed to “0”
11	Register 53h Bit 5 Always Page Miss After Code Read DRAM Cycles (Page 23)	Always Page Miss After Write DRAM Cycles
12	Register 53h Bit 3 Always Page Miss After Write DRAM Cycles (Page 23)	Always Page Miss After Code Read DRAM Cycles
13	Register 54h Bits 3:2 RAS to CAS delay 00:2T, 01:3T, 10:4T, 11:Reserved (Page 24)	Recommend “01” for 66Mhz , -6 DRAM “10” for -7 DRAM

14	Register 54h Bit 0 CAS[7:0]# active low pulse width for EDO DRAM (Page 24)	This bit can only be programmed to “1” in 5571 A.
15	Register 56h MDLE delay Bits 7:4 Reserved Bits 3:0 MDLE delay (Page 24)	Bits 7:3 Reserved Bits 2:0 MDLE delay 000:0ns, 001:1ns, 010:2ns, 011:3ns, 100:4ns, 101:5ns, 110:6ns, 111:7ns Recommended value: 011
16	Register 58h DRAM timing adjustment (Page 25)	Register 58h Reserved Do not program it.
17	Register 5Ah 1: Selection…… 0: Selection……. (Page 25)	Register 5Ah Bit 1: Selection…… Bit 0: Selection……. 0: 8mA 1:16mA
18	Register 81h Bit 4 Prefetch Timing for SDRAM data to CTPFF (Page 26)	Register 81h Bit 4 Reserved This bit must be programmed to “0”.
19	Register 81h Bit 1 Enable CPU to L2/DRAM and 5571 to PCI peer to peer concurrency mode (Page 26)	Register 81h Bit 1 Reserved This bit must be programmed to “0”.
20	Register 83h Bit 5 Fast reset latency control 0:6us 1:2us (Page 28)	0:2us 1:6us
21	Register 87h Bit 6 CPU involve arbitration 0: Disable 1:Enable (recommended) (Page 28)	This bit should be programmed to “0”.
22	Register CF9 Bit 1 Enable system hardware reset (Page 37)	Reserved
23	Registers 04h , 05h Bit 1: Respond to Memory Space Accesses Bit 0: Respond to I/O Space Accesses (Page 45)	These two bits must be programmed to “1”.
24	Register 62h Bit 3 (Page 53) ...channel specified in bits [6:4]...	….channel specified in bits [2:0]…
25	Register 70h Bit 1 Built in RTC status 0: not used 1:used (Page 58)	0: used 1: not used

26	USB Register 68h Bit 6 Reserved (Page 55)	Built-in USB disable/enable 0: Disable 1:Enable This bit is only applied to 5571 B.
27	MD56/MD55/MD54 110:75MHZ 101:66MHZ 100:60MHZ 010:50MHZ (Page 86)	MD56/MD55/MD54 001:75MHZ 010:66MHZ 011:60MHZ 101:50MHZ
28	Input Leakage Current +/- 10mA (Page 87)	Input Leakage Current +/- 10 uA
29	Register 53h Bit 6 Reserved (Page 23)	Bit 6 Read after Write turn around Cycle 0: Disable 1: Enable (1 is recommended for 75MHz.)
30	Register 43h USB Host Controller Specific (Page 65)	Reserved
31	Register 4Ah Bit 5 Reserved (Page 69)	Bit 5 IDE Postwrite Cycle Selection 0: 6 PCICLK 1: 3 PCICLK