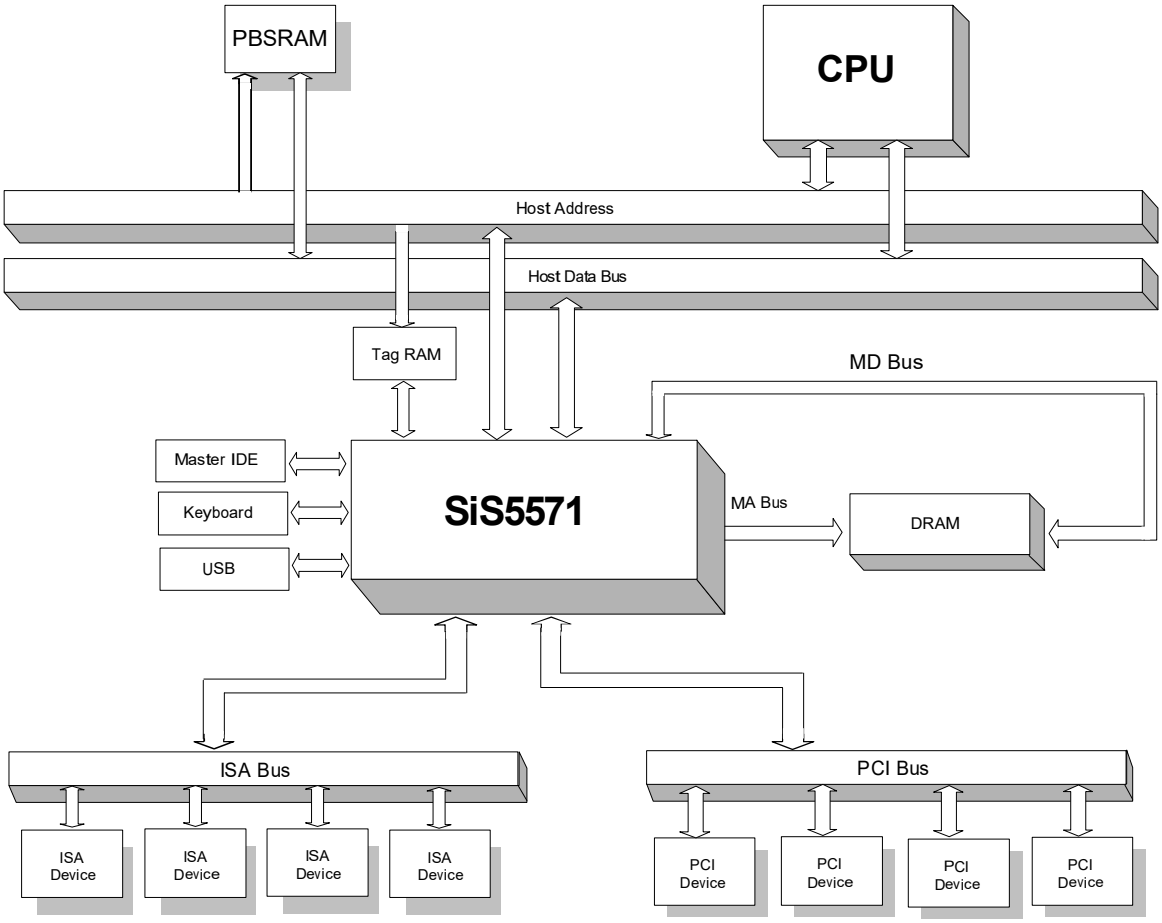
1. System Block Diagram



2. Features

- **Supports Intel Pentium CPU and other compatible CPU at 75/66/60/50MHz (external clock speed)**
- **Supports the Pipelined Address Mode of Pentium CPU**
- **Supports the Full 64-bit Pentium Processor data Bus**
- **Supports 32-bit PCI Interface**
- **Integrated Second Level (L2) Cache Controller**
  - Write Through and Write Back Cache Modes
  - 8 bits or 7 bits Tag with Direct Mapped Cache Organization
  - Integrated 16K bits Dirty Ram
  - Supports Pipelined Burst SRAM
  - Supports 256 KBytes to 512 MBytes Cache Sizes
  - Cache Read/Write Cycle of 3-1-1-1-1-1-1-1 at 66 MHz
- **Integrated DRAM Controller**
  - Supports 3 Banks of FP/EDO SIMMs, or 2 Banks of SDRAM DIMMs
  - Supports 2Mbytes to 384Mbytes of main memory
  - Supports 256K/512K/1M/2M/4M/16M x N FP/EDO/SDRAM DRAM
  - Supports 3V or 5V DRAM.
  - Supports Symmetrical and Asymmetrical DRAM.
  - Supports 32 bits/64 bits mixed mode configuration
  - Supports Concurrent Write Back for FP/EDO DRAM
  - Supports Mixed DRAM (FP/EDO/SDRAM) Technology
  - Supports CAS before RAS Refresh
  - Supports Relocation of System Management Memory
  - Programmable CAS# ,RAS#, RAMW# and MA Driving Current
  - Fully Configurable for the Characteristic of Shadow RAM (640 KBytes to 1 MBytes)
  - Supports FP DRAM 5-3-3-3(-3-3-3-3) Burst Read Cycles
  - Supports EDO DRAM 4/5-2-2-2(-2-2-2-2) Burst Read Cycles
  - Supports SDRAM 6/7-1-1-1(-2-1-1-1) Burst Read Cycles
  - Supports X-1-1-1/X-2-2-2/X-3-3-3 Burst Write Cycles
  - Supports 8 Qword Deep Buffer for Read/Write Reordering, Dword Merging and 3/2-1-1-1 Post write Cycles
  - Two Programmable Non-Cacheable Regions
  - Option to Disable Local Memory in Non-Cacheable Regions
  - Shadow RAM in Increments of 16 KBytes
- **Integrated PMU Controller**
  - Supports SMM Mode of CPU
  - Supports CPU Stop Clock

- Supports Break Switch
- Supports Modem Ring Wakeup
- Supports Automatic Power Supply Control

- **Provides High Performance PCI Arbiter.**
  - Supports 3 internal masters and 5 external PCI Masters
  - Supports Rotating Priority Mechanism
  - Hidden Arbitration Scheme Minimizes Arbitration Overhead.
  - Supports Concurrency between CPU to Memory and PCI to PCI.
- **Integrated Host-to-PCI Bridge**
  - Supports Asynchronous/Synchronous PCI Clock
  - Translates the CPU Cycles into the PCI Bus Cycles
  - Provides CPU-to-PCI Read Assembly and Write Disassembly Mechanism
  - Translates Sequential CPU-to-PCI Memory Write Cycles into PCI Burst Cycles
  - Zero Wait State Burst Cycles
  - Supports 8 DW Deep Buffer for CPU-to-PCI Posted Write Cycles
  - Supports Pipelined Process in CPU-to-PCI Access
  - Supports Advance Snooping for PCI Master Bursting
  - Maximum PCI Burst Transfer from 256 Bytes to 4 Kbytes
  - Fast back-to-back
- **Integrated Posted Write Buffers and Read Prefetch Buffers to Increase System Performance**
  - CPU-to-Memory Posted Write Buffer (CTMFF) with 8 QW Deep, Always Sustains 0 Wait Performance on CPU-to-Memory.
  - CPU-to-PCI Posted Write Buffer(CTPFF) with 8 DW Deep
  - PCI-to-Memory Posted Write Buffer(PTHFF) with 8 QW Deep, Always Streams 0 Wait Performance on PCI-to/from-Memory Access
  - PCI-to-Memory Read Prefetch Buffer(CTPFF) with 8 QW Deep
- **Built-in one 32-bit General Purpose Register**
- **Integrated PCI-to-ISA Bridge**
  - Translates PCI Bus Cycles into ISA Bus Cycles
  - Translates ISA Master or DMA Cycles into PCI Bus Cycles
  - Provides a Dword Post Buffer for PCI to ISA Memory cycles
  - Two 32 bit Prefetch/Post Buffers Enhance the DMA and ISA Master Performance
  - Fully Compliant to PCI 2.1
- **Enhanced DMA Functions**
  - 8-, 16- bit DMA Data Transfer
  - ISA compatible, and Fast Type F DMA Cycles
  - Two 8237A Compatible DMA Controllers with Seven Independent Programmable Channels

- Provides the Readability of the two 8237 Associated Registers

- **Built-in Two 8259A Interrupt Controllers**
  - 14 Independently Programmable Channels for Level- or Edge-triggered Interrupts
  - Provides the Readability of the two 8259A Associated Registers
- **Three Programmable 16-bit Counters compatible with 8254**
  - System Timer Interrupt
  - Generates Refresh Request
  - Speaker Tone Output
  - Provides the Readability of the 8254 Associated Registers
- **Built-in Keyboard Controller**
  - Hardwired Logic Provides Instant Response
  - Supports PS/2 Mouse
  - Support Hot Key "Sleep" Function
- **Built-in Real Time Clock(RTC) with 256B CMOS SRAM**
- **Fast PCI IDE Master/Slave Controller**
  - Fully Compatible with PCI Local Bus Specification V2.1
  - Supports PCI Bus Mastering
  - Plug and Play Compatible
  - Supports Scatter and Gather
  - Supports Dual Mode Operation - Native Mode and Compatibility Mode
  - Supports IDE PIO Timing Mode 0, 1, 2 of ANSI ATA Specification
  - Supports Mode 3 and Mode 4 Timing Proposal on Enhanced IDE Specification
  - Supports Multiword DMA Mode 0, 1, 2
  - Separate IDE Bus
  - Two 8x32-bit FIFO for PCI Burst Read/Write Transfers.
- **Universal Serial Bus Controller**
  - Host/Hub Controller
  - Two USB ports
- **On-Board Plug and Play Support**
  - One Steerable DMA Channel
  - One Steerable Interrupt
  - One Programmable Chip Select
- **Supports the Reroutibility of the four PCI Interrupts**
- **Supports Flash ROM**
- **480-Pin BGA Package**
- **0.56 µm CMOS Technology**

3. Functional Description

3.1 DRAM Controller

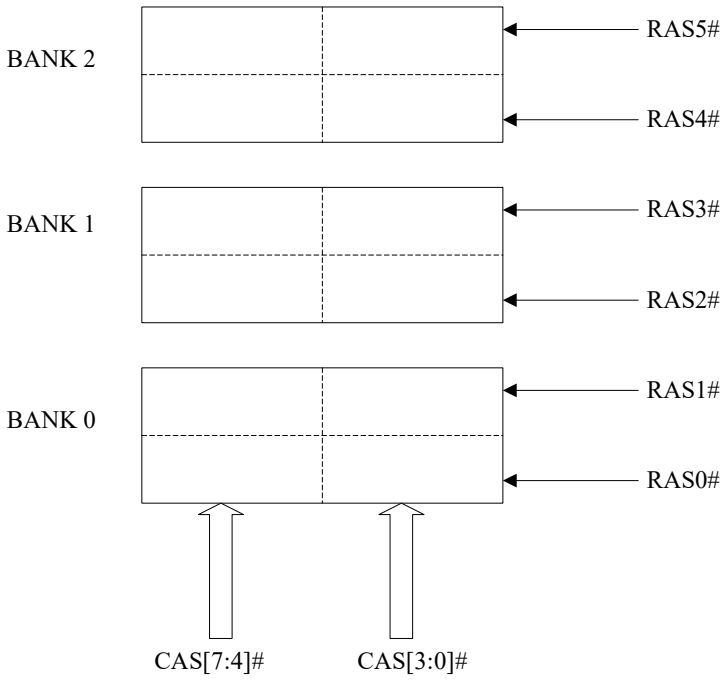
3.1.1 DRAM Type

The SiS5571 can support up to 384MBytes (3 banks) of DRAMs and each bank could be single or double sided 64 bits FP (Fast Page mode) DRAM, EDO (Extended Data Output) DRAM, and SDRAM (Synchronous DRAM) DRAM. Half populated bank(32-bit) is also supported.
The installed DRAM type can be 256K, 512k, 1M, 2M, 4M or 16M bit deep by n bit wide DRAMs, and both symmetrical and asymmetrical type DRAM are supported. It is also permissible to mix the DRAMs (FP/EDO/SDRAM) bank by bank and the corresponding DRAM timing will be switched automatically according to register settings.

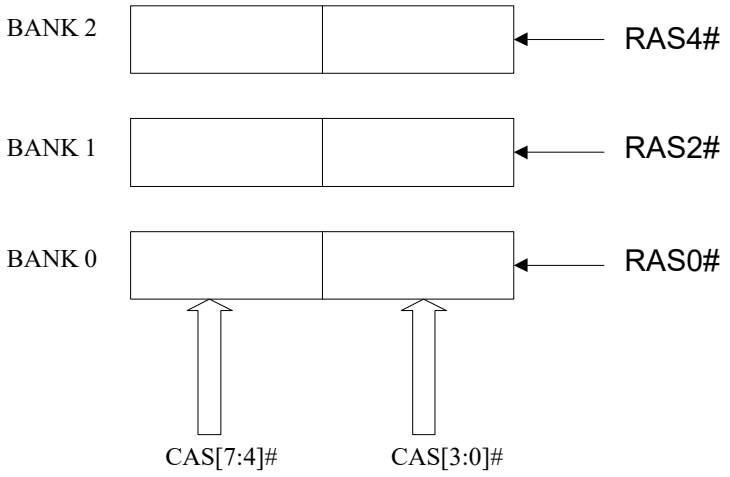
3.1.2 DRAM Configuration

The SiS5571 can support single sided or double sided DRAM modules for each bank. The basic configurations are shown as the following:

3.1.3 Double-sided DRAM:



3.1.4 Single-sided DRAM



3.1.5 DRAM Scramble Table

The DRAM scramble table contains information for memory address mapping. This table provides the translation between CPU host address and memory Row and Column address. There are two different memory address mapping: 64-bit mapping and 32-bit mapping that SiS5571 supports:

3.1.6 64-bit mapping table

a. Symmetric:

9x9(256K), 10x10(1M), 11x11(4M), 12x12(16M)

	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
CAS	HA25	HA23	HA21	HA11	HA10	HA9	HA8	HA7	HA6	HA5	HA4	HA3
RAS	HA26	HA24	HA22	HA20	HA19	HA18	H17	HA16	HA15	HA14	HA13	HA12

b. Asymmetric:

12x8(1M), 12x9(2M), 12x10(4M), 12x11(8M)/10x9(512K), 11x9(1M), 11x10(2M)

	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
CAS	HA22	HA25	HA24/ 23	HA23/ 11	HA10	HA9	HA8	HA7	HA6	HA5	HA4	HA3
RAS	HA22/ 24	HA21/ 22	HA11/ 21	HA20	HA19	HA18	H17	HA16	HA15	HA14	HA13	HA12

3.1.7 32-bit mapping table

a. Symmetric:

9x9(256K), 10x10(1M), 11x11(4M), 12x12(16M)

	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
CAS	HA25	HA23	HA21	HA10	HA4	HA9	HA8	HA7	HA6	HA5	HA3	HA2
RAS	HA24	HA22	HA20	HA11	HA19	HA18	H17	HA16	HA15	HA14	HA13	HA12

b. Asymmetric:

12x8(1M), 12x9(2M), 12x10(4M), 12x11(8M)/10x9(512K), 11x9(1M), 11x10(2M)

	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
CAS	HA21	HA24	HA23/ 22	HA22/ 10	HA4	HA9	HA8	HA7	HA6	HA5	HA3	HA2
RAS	HA21/ 23	HA20/ 21	HA10/ 20	HA11	HA19	HA18	H17	HA16	HA15	HA14	HA13	HA12

3.2 DRAM Performance

All the DRAM cycles are synchronous with the CPU clock. The following table shows the different possible speed settings that depend on different DRAM type, RAS# setting, CAS# setting, and so forth.

Cycle Type	DRAM type	66, 60 Mhz	50 Mhz	Note
Read Page Hit	EDO	4/5-2-2-2	4-2-2-2	
	FP	5-3-3-3	4-2-2-2	*1
	SDRAM	6-1-1-1	6-1-1-1	CL=2
		7-1-1-1	7-1-1-1	CL=3
Read Row miss	EDO	8/9-2-2-2/ 9-3-3-3	8/9-2-2-2/ 9-3-3-3	*2
	FP	8/9-3-3-3	8/9-3-3-3	*1
	SDRAM	7-1-1-1	8-1-1-1	CL=2
		8-1-1-1	9-1-1-1	CL=3
Read Page Miss	EDO	10/101-2-2-2	9/10-2-2-2	*3
	FP	10/101-3-3-3	9/10-3-3-3	*1 *3
	SDRAM	11-1-1-1	12-1-1-1	CL=2
		12-1-1-1	13-1-1-1	CL=3
Back-to-Back Burst Read Page Hit	EDO	4/5-2-2-2-2-2-2-2...	4-2-2-2-2-2-2-2...	
	FP	5-3-3-3-3-3-3-3...	4-2-2-2-2-2-2-2...	
	SDRAM	6-1-1-1-2-1-1-1...	6-1-1-1-2-1-1-1...	CL=2
		7-1-1-1-3-1-1-1...	7-1-1-1-3-1-1-1...	CL=3
Posted Write	EDO/FP/SDRAM	3-1-1-1	3-1-1-1	
Write Retire Rate (Buffer to DRAM)	EDO	2-2-2/3-3-3	2-2-2/3-3-3	
	FP	3-3-3	2-2-2/3-3-3	*1

	SDRAM	1-1-1/2-2-2	1-1-1/2-2-2	CL=2
		1-1-1/2-2-2	1-1-1/2-2-2	CL=3

Write Page Hit	EDO	2	2	
	FP	2	2	
	SDRAM	2	2	CL=2
		2	2	CL=3
Write Row Miss	EDO	9	9	
	FP	5	5	
	SDRAM	4	4	CL=2
		4	4	CL=3
Write Page Miss	EDO	7	6	
	FP	7	6	
	SDRAM	7	7	CL=2
		7	7	CL=3

*1 X-4-4-4 is for both CAS pulse width and CAS precharge time are 2 CPU clocks.
*2 It is for RAS to CAS time of 3 CPU clocks.
*3 It is for RAS pre-charge time of 4 CPU clocks, RAS to CAS time of 3 CPU clocks.

3.3 CPU to DRAM Posted Write FIFOs

There is a built-in CPU to Memory posted write buffer with 8 QWord deep (CTMFF). All the write access to DRAM will be buffered. For the CPU read miss / Line fill cycles, the write-back data from the second level cache will be buffered first, and right after the data had been posted write into the FIFO, CPU can performs the read operation by the memory controller starting to read data from DRAMs. The buffered data are then written to DRAM whenever no any other read DRAM request comes. With this concurrent write back policy, many wait states are eliminated. If there comes a bunch of continuous DRAM write cycles, some ones will be pending if the CTMFF is full.

3.4 32-bit (Half-Populated) DRAM Access

For the read access, there will be either single or burst read cycle to access the DRAM which depends on the cacheability of the cycle. If the current DRAM configuration is half-populated bank, then the SiS5571 will assert 8 consecutive cycles to access DRAM for the burst cycle. For the single cycle that only accesses DRAM within a DWord, the SiS5571 will only issue one cycle to access DRAM. For the single cycle that accesses one Qword or cross DWord boundary, the SiS5571 will issue two consecutive cycles to access DRAM.

3.5 Arbiter

The arbiter is the interface between the DRAM controller and the host which can access DRAMs. In addition to pass or translate the information from outside to DRAM controller, arbiter is also responsible for which master has higher priority to access DRAMs. The arbiter treats different DRAM access request as DRAM master, and that makes there be 5 masters which are trying to access DRAMs by sending their request to the arbiter. After one of them get the grant from the arbiter, it owns DRAM bus and begins to do memory data tranction.
The masters are: CPU read request, PCI master, Posted write FIFO write request, and Refresh request. The order of these masters shown above also stands for their priority to access memory.

3.6 Refresh cycle

The refresh cycle will occur every 15.6 us. It is timed by a counter of 14Mhz input. The CAS[7:0]# will be asserted at the same time, and the RAS[5:0]# are asserted sequentially.

3.7 PCI bridge

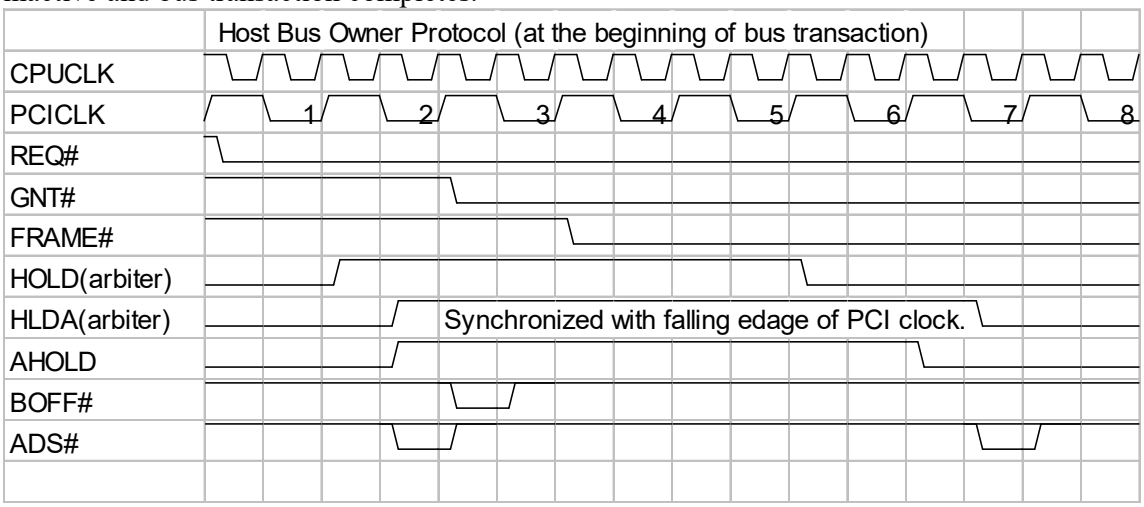
SiS5571 is able to operate at both asynchronous and synchronous PCI clocks. Synchronous mode is provided for those synchronous system to improve the overall system performance.
While in the PCI master write cycles, post-write is always performed. And function of Write Merge with CPU-to-DRAM post-write buffer is incorporated to eliminate the penalty of snooping write-back. On the other hand, prefetch is enabled for master read cycles by default, and such function could be disabled optionally. And, Direct-Read from CPU-to-DRAM post-write buffer is implemented to eliminate the overhead of snooping writ-back also.
In addition to Write-Merge and Direct-Read, Snoop-Ahead also hides the overhead of inquiry cycles for master to main memory cycles. These key functions, Write-Merge, Direct-Read and Snoop-Ahead, achieve the purpose of zero wait for PCI burst transfer.
The post-write and prefetch buffers are both 16 Double-Word deep FIFOs .

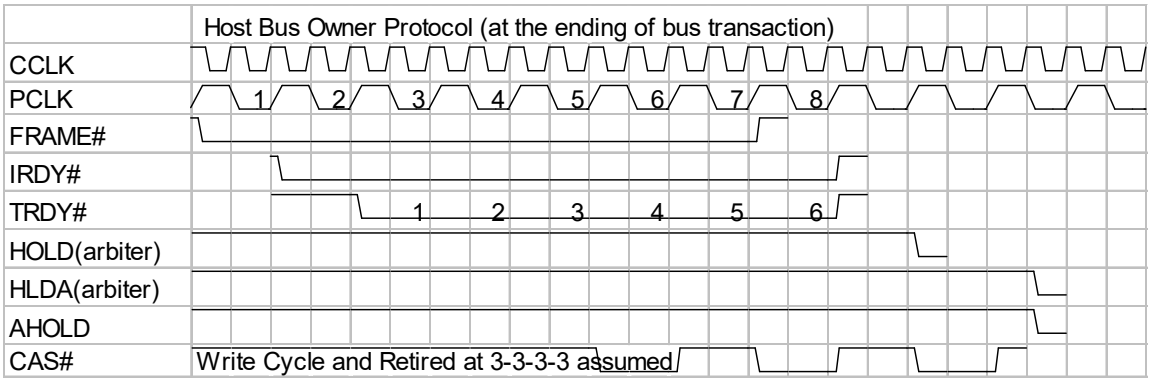
3.8 Snooping Control

In order to maintain the cache consistency while PCI master accesses to main memory, SiS5571 performs inquiry cycle to snoop L1 and L2 caches before PCI masters really read from or write to memory. For the purpose of snooping, AHOLD is asserted to force the Pentium-like processors to float its address bus as soon as PCI master requests the PCI bus. Such host bus hold mechanism is completed by an AHOLD/BOFF# process and will be depicted later. Since the inquiry cycle is the major penalty for PCI master cycles, SiS5571 builds in a high performance snoop-ahead mechanism to incorporate the zero wait requirement of PCI bus transactions.
The main idea of "snoop-ahead" is to do memory operations and inquiry cycle simultaneously. For example, when transferring the Ln line of data, SiS5571 also performs the Ln+1 line of inquiry cycle in the mean while.

3.9 AHOLD/BOFF# Process and Arbiter Interface

In order to perform inquiry cycles, SiS5571 uses AHOLD to hold address bus of Pentium-like CPUs. While PCI master asserts REQ#, SiS5571 will drive AHOLD firstly. And, if PCI master operates a peer-to-peer transaction, SiS5571 will deasserts AHOLD to permit CPU to do memory cycles concurrently. Otherwise, SiS5571 retains AHOLD signal until REQ# is inactive and bus transaction completes.





3.10 Target Initiated Termination

In general, SiS5571 is capable to complete all the requests to access main memory from PCI masters until master terminates the transaction actively. Sometimes, as SiS5571 is unable to respond or is unable to burst, it will initiate to terminate bus transactions and STOP# will be issued by doing Retry or Disconnect.

3.10.1 Target Retry

SiS 5571 may operate Target Retry for one of two reasons:

1. Whenever a PCI master tries to access main memory and SiS 5571 is locked previously by another agent, Target Retry will be signaled.
2. Once SiS 5571 can‘t meet the requirement of target initial latency, Target Retry is used and no data is transferred.

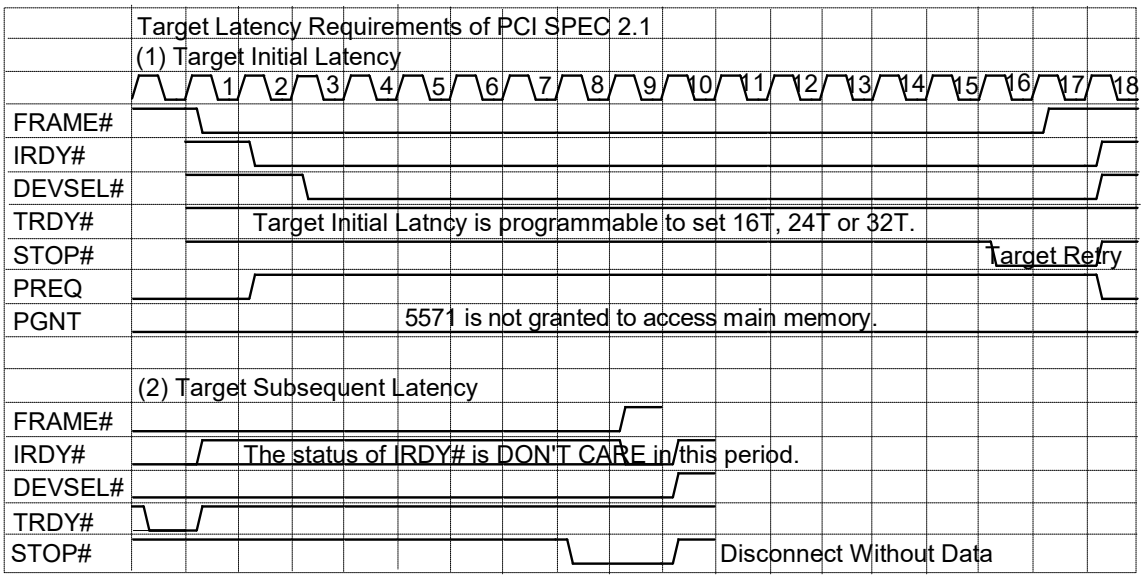
3.10.2 Disconnect With Data

In some situations, such as the burst crosses a resource boundary or a resource conflict, SiS5571 might be temporarily unable to continue bursting, and, therefore, SiS5571 concludes an active termination.

1. SiS5571 supports PCI burst transfers, the bursting length can be 256 bytes, 512 bytes, 1K bytes, 2K bytes, or 4K bytes. A burst will be terminated by doing Disconnect if the transfer goes across the programmed bursting length. In this way, at most 128 cache lines of data can be uninterruptedly transferred no matter what the status they are in L1 and L2. One reason for the constraint is that page miss may occur only once at the beginning of the entire bursting transaction since the maximum bursting length is always within the page size in any of the used DRAM.
2. If advanced snoop function is disabled, PCI transaction will not cross the cache boundary and also causes a Disconnect operation. Since the heavy overhead of inquiry cycles is not preventable, and SiS5571 can‘t keep bursting transfer.

3.10.3 Disconnect Without Data

If Target Subsequent Latency timer expires, it causes SiS 5571 to assert STOP# by doing Disconnect operation.



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3.11 DATA Flow

The major two data paths are PCI->PTHFF->DRAM and DRAM->CTPFF->PCI for PCI master write DRAM cycles and read DRAM cycles, respectively. For cache system, if an inquiry cycle hits Pipeline Burst SRAM, SiS5571 would read from L2 directly, but write DRAM and L2 simultaneously.

Based on snooping result, there are additional data path that SiS5571 should perform.

Table Data Flow Based on Snooping Result

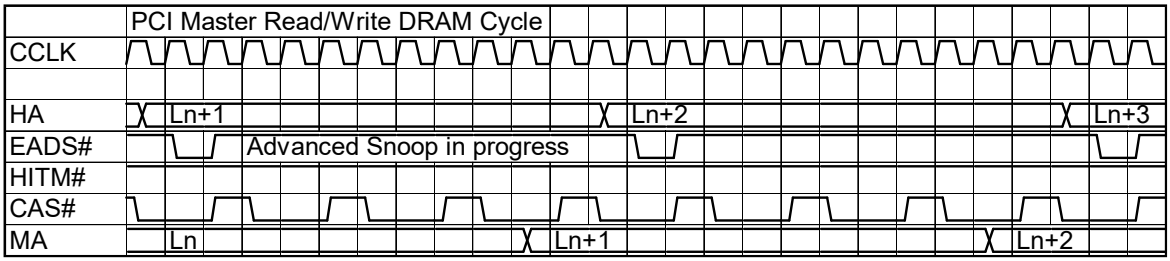
PCI Master Read Memory Cycle			
Result of Snoop		Data Flow	Operation
Status of L1	Status of L2		
Miss or Unmodified	Miss or None	DRAM -> CTPFF -> PCI	Read DRAM
	Hit and Not Dirty	DRAM -> CTPFF -> PCI	Read DRAM
	Hit and Dirty	L2 -> CTPFF -> PCI	Read L2
Hit Modified	Miss or None	L1 -> CTMFF & CTPFF CTPFF -> PCI	Direct Read
	Hit, Dirty or Not	L1 -> L2 & CTPFF CTPFF -> PCI	Direct Read

PCI Master Write Memory Cycle			
Result of Snoop		Data Flow	PSL Operation
Status of L1	Status of L2		
Miss or Unmodified	Miss or None	PCI -> PTHFF -> DRAM	Write DRAM
	Hit, Dirty or Not	PCI -> PTHFF -> L2&DRAM	Write DRAM&L2
	Miss or None	L1 -> CTMFF PTHFF & CTMFF -> DRAM	Write Merge

Hit Modified	Hit, Dirty or Not	L1 -> L2 PCI -> PTHFF -> L2&DRAM	Write DRAM&L2

3.12 PCI Master Read/Write DRAM Cycle

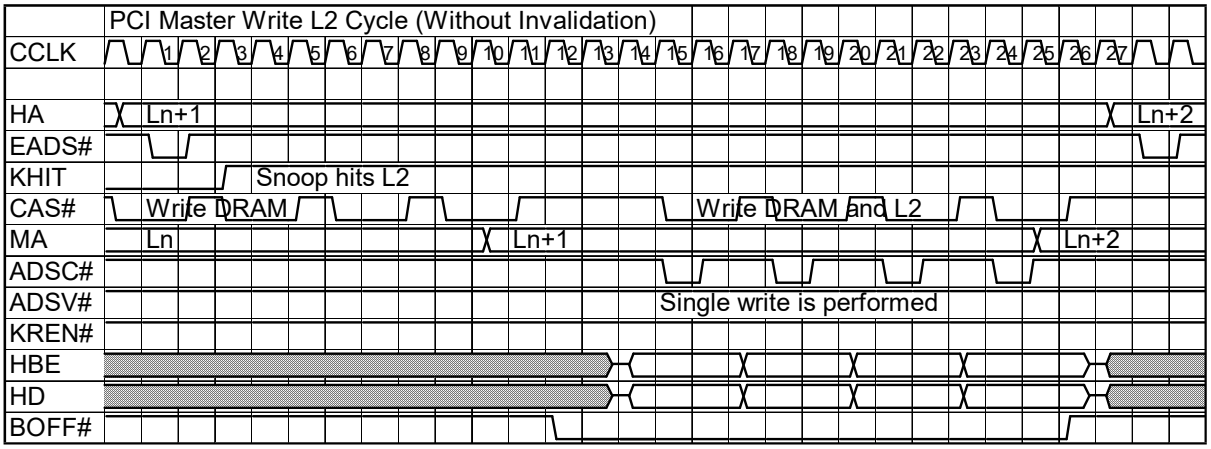
If inquiry cycle hits neither L1 nor L2, SiS5571 could perform prefetching/retiring operation and inquiry cycles simultaneously.



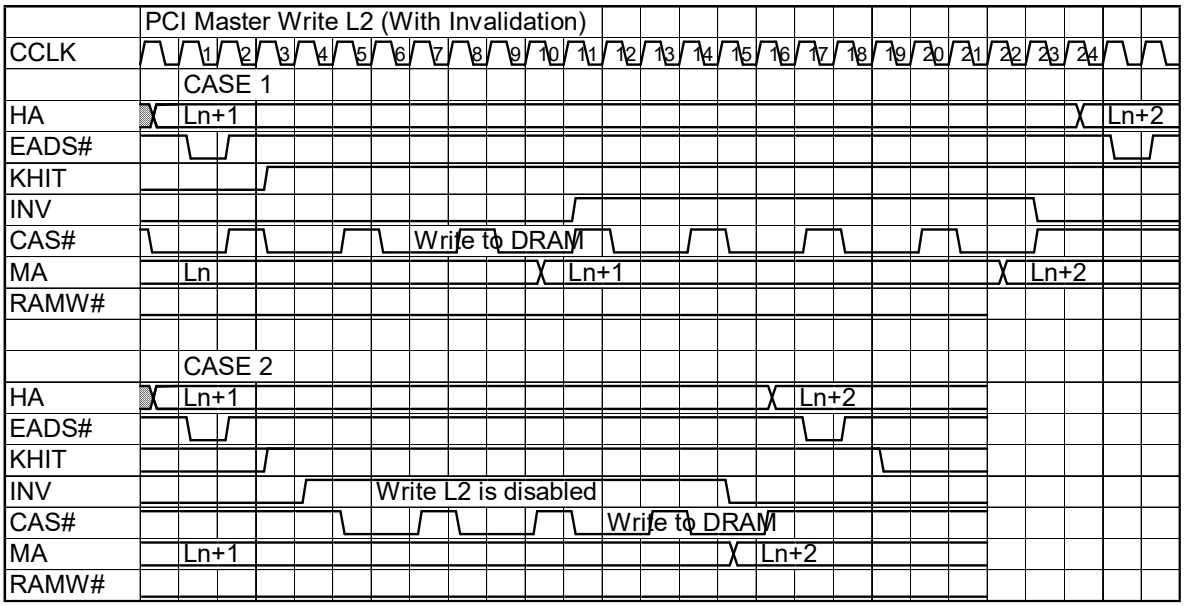
3.12.1 PCI Master Write L2 and DRAM Cycles

(1) Without Invalidation

For the purpose of writing L2, PSL must drive the HBE and HD bus. Then, BOFF# is asserted to force CPU floats the host bus. And to retain the correct address on HA, advanced snoop is temporally suspended.



(2) With Invalidation



3.12.2 PCI Arbiter

Introduction

The main function of PCI arbiter takes charge of the PCI bus ownership assignment. Theis PCI arbiter supports at most 8 external PCI masters. Note that one PCI master is reserved for SIO. The arbitration operation is applied to these 8 masters and CPU.

The arbitration scheme ~~which we design~~ is done at two layers. CPU has the highest priority, i.e., CPU will be the PCI bus owner if there is a request from PMR. If there is no request from PMR, rotational priority scheme will be applied to these masters.

Arbitration Algorithm

PCI Masters (Agent 0~6, SIO) Requests

Figure.1 shows the arbitration tree in arbiter design. Whenever a PCI cycle occurs, priority status will be changed. The order for master 0-7 to own PCI bus is 4 -> 0->SIO->2->5->1->6->3->4.....

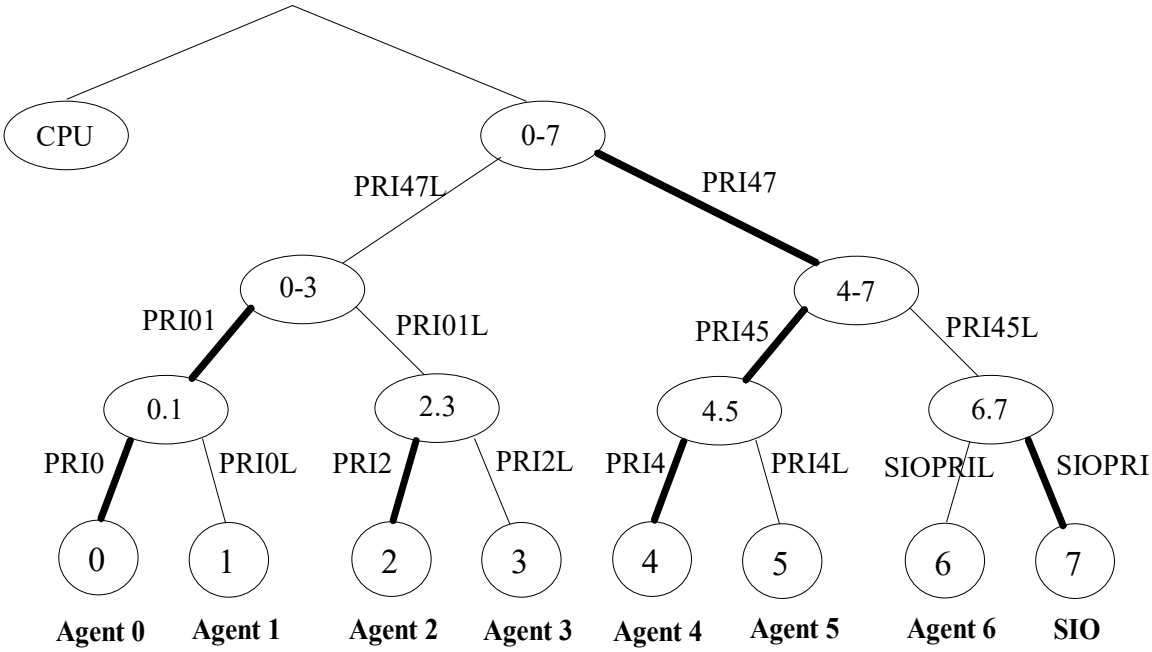


Figure 3.1~~1~~1 Arbitration Tree

CPU Request

~~In our previous design, CPU will be constantly held if PCI masters continuously deliver requests to the arbiter. To address this problem in 5571, we derived~~ A~~a~~ timer-based algorithm is used to reserve PCI bandwidth for CPU. Three timers (PGT, MLT and CIT) are included in the host bridge for this purpose.

Whenever the PCI bus is owned by any PCI device other than host bridge, PCI grant timer (PGT) starts to count. After the timer is expired, the host bridge asserts its request signal to ask for gaining the control of PCI bus. Since the host bridge has the highest priority, PCI arbiter grants the bus to the host bridge as soon as possible after it receives the request from the host bridge.

Once the host bridge get a chance to start a transaction on PCI bus, its master latency timer (MLT) begins to count. After MLT is expired, the host bridge deasserts its request signal to inform the arbiter that the host bridge no more needs the PCI bus. If there is any other PCI decive that asks for the bus, arbiter grants the bus to the device and Cpu is held again.

Whenever there are no requests from all PCI devices, the arbiter parks the bus on the host bridge. The ratio MLT/PGT approximately guarantees the minimum PCI bandwidth allocated to host bridge when CPU and PCI masters are contending for system resources, but it doesn't constrain CPU's highest utilization of PCI bus because of our bus parking policy.

To prevent the host bridge from capturing PCI bus too long while CPU actually has nothing to do at all, the third timer, CPU idle timer (CIT) is included in our design. CIT starts to count when the host bridge get a chance to start a transaction on PCI bus, but is reloaded with its initial value whenever the host bus leaves idle state. CIT actually keeps track on how long the

CPU is in idle state. After CIT is expired, the host bridge deasserts its request signal just in the same manner as the case of MLT's expiration.
PGT is a 16-bit timer. MLT and CIT are both 8-bit timers. All of the initial values of the three timers are programmalbe and can be tuned according to the nature of the application. Although CIT & MLT are both 8-bit timers, the initial value of CIT is typically programmed much smaller than MLT.

PCI peer-to-peer access concurrent with CPU to L2/DRAM access

With this feature, a transaction initiated by a PCI master targeting a PCI target won't hold CPU. The CPU can still access L2 cache, system memory and PCI post-write buffers when PCI peer-to-peer activities are undergoing. With the enlarged 8 Dword deep PCI post-write buffers, it takes longer for CPU to halt while PCI peer-to-peer accesses are taking place.

Arbitration Parking

When no agent is currently using or requesting the bus, the arbiter will grant the bus ownership to PMR.

CPU to PCI Bridge

The CPU to PCI bridge forwards the CPU cycles not targeting the local memory to the PCI bus, In the case of a 64-bit CPU request or a misaligned 32-bit CPU request, the bridge takes the duty of read assembly and write disassembly control, A 8 level post-write buffer is implemented to improve the performance of CPU to PCI memory write and CPU to Idle data port write. Except for on-board memroy wirte cycles, and cycles frowarded to the PCI bus will be suspended until the post-write buffer is empty. For memory write cycles toward PCI or I/O write cycles towards IDE data port, the CPU data are pushed into the post write buffer if it is not full. The push rate for a double word is 3 CPU clocks. The pushed data are, at later time, written to the PCI bus. If the addresses of consecutive written data are in double word incremental sequence and they are targeting memory space, they will be transferred to the PCI bus ina burst manner.
The bridge provides a mechanism for converting standard I/O cycles on the CPU bus to configuration cycles on the PCI bus. Configuration Mechanism#1 in PCI Specification is used to do the cycle conversion.
The bridge always intercepts the first interrupt acknowledge cycle from CPU bus, and forwards the second interrupt acknowledge cycle onto the PCI bus.
The bridge is designed to be able to handle asynchronous clock relationship between CPU and PCI. However, in order to enhance the performance of the bridge when PCI clock is lagging CPU clock by 2~4 ns, an optional synchronous mode is provided. The synchronous mode can averagely save two extra CPU clocks for a signle nonpost cycle.

4. Power Management Unit (PMU)

The function of PMU is to provide power management functions for the system to meet Green PC requirement. The main methodology of PMU is to generate SMI#, STPCLK# and FLUSH# to CPU for different situations.

4.1 Block Diagram

PMU block can be divided into several sub-blocks as shown in Fig.4.1. Events Catching Logic is responsible for recording the events that request SMI#. Time Base generation logic is to generate the clock for timer. Timers are responsible for timeout reporting. SMI generation Logic is for SMI# generation. STPCLK# generation Logic is for STPCLK generation. FLUSH# generation Logic is for FLUSH# generation.

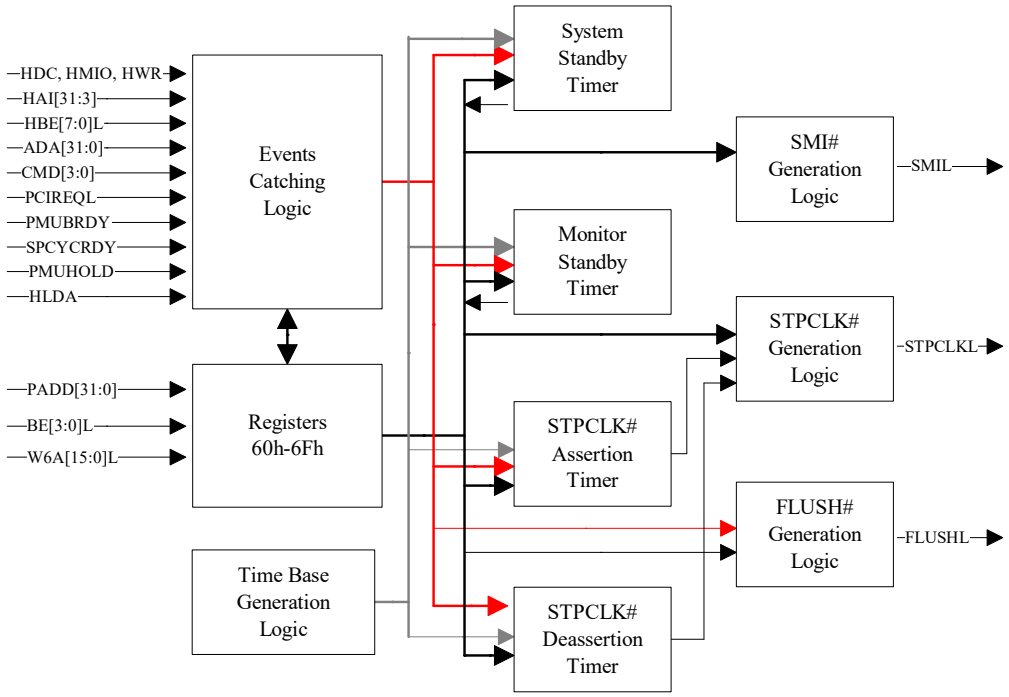


Figure 4.1~~1~~1 PMU Block Diagram

4.2 Time Base Generation Logic

All the clocks used in PMU timers are derived from 14.318 MHZ and 1.2 MHZ clocks. To support different time slots, ~~we use~~ frequency divider is used~~to obtain the clock we require~~. The time slots ~~we support~~ are divided in two classes. One is for monitor standby timer and the other is for system standby timer. The former includes 6.6sec, 0.84sec, 13.3ms and 1.6ms

programmability while the latter includes 9 sec, 1.1 sec, 70ms and 8.85ms programmability. ~~Besides, we provide CPU clock for timer in test mode.~~

4.3 Timer

There are three kinds of timer defined in PMU. One is for monitor activity, another is for system activity and the other is for STPCLK# behavior generation. In order to save monitor power dissapation, ~~we~~ provide monitor standby timer ~~to~~ detects if there is any monitor-related activity. If there is any activity, monitor standby timer will be reloaded. Otherwise, monitor standby timer will continueously count down. If it count to zero, it will report timeout event. Sytem standby timer has the same operation as monitor standby timer. STPCLK# assertion/deassertion timer is to toggle STPCLK# signal in Throttling mode.

4.4 Event Catching Logic

4.4.1 System Sleep Events

The timeout of system timer will request SMI# to enter Sleep state. If throttling mode is enabled, PMU will enter throttling mode. Otherwise, if STPCLK# mode is enabled, PMU will enter sleep mode. If both modes are disabled, PMU remains wakeup.

4.4.2 System Wakeup events

The following events will wakeup system from Standby state to Normal state.
Software Wakeup
RING#
IRQ 1-15, NMI (via Wakeup1)
INIT
PCI or ISA master request

4.4.3 Monitor Timeout event

If monitor timer expires, SMI# will be generated to request turn-off monitor power.

4.4.4 Monitor Wakeup Events

The following shows the events that can wakeup monitor from Standby to Normal state.
IRQ1-15,NMI (via Wakeup0)
PCI master, ISA master activity
Ring Activity

4.4.5 SMI Sources

The following shows the sources to generate SMI request.
System Standby SMI
System Wakeup SMI
Throttling Wakeup SMI
Monitor Standby SMI

Monitor Wakeup SMI
Ring SMI
Keyboard Port SMI
Primary Hard Disk Port SMI
Secondary Hard Disk Port SMI
Primary Serial Port SMI
Secondary Serial Port SMI
Parallel Port SMI
APM SMI
Break Switch SMI
10-bit Programmable Port SMI
16-bit Programmable Port SMI
IRQ SMI
USB SMI

4.5 Output generation Logic

4.5.1 SMI# generation

When there is any event to request entering sleep/throttling/wakeup state, SMI# will be issued. When SMI# is recognized by CPU, SMI routine will handle the operation of state transition.

4.5.2 STPCLK# generation

STPCLK# generation is initialized by SMI routine by writing Reg. 93 bit 3 to '1'. The behavior of STPCLK# is dependent on the configuration register setting, i.e., non-throttling or throttling.

4.5.3 FLUSH# generation

FLUSH# is generated for DeTurbo mode. By issuing FLUSH#, CPU will write back all modified cachelines in the data cache and invalidate both internal code and data caches. Flush Acknowledge special cycle will be driven once flush operation is completed. Hence, CPU performance can be degraded.

4.6 Operation of Power Management

There are three states in PMU, i.e., Wakeup state, Sleep state and Throttling state. In wakeup state, system wakes up from sleep or throttling state. In sleep state, STPCLK# will always asserted until exiting Sleep state. In throttling state, STPCLK# will be asserted and deasserted periodically.
Once CPU recognizes a STPCLK# interrupt, CPU will perform the following:
1. Wait for all instructions being executed to complete.
2. Flush the instruction pipeline of any instructions waiting to be executed.
3. Wait for all pending bus cycles to complete and EWBE# to go active.

4. Drive a special bus cycle(stop grant bus cycle) to indicate that the clock is being stopped. Stop grant bus cycle is decoded as follows: M/IO#=0, D/C#=0, W/R#=1, Address Bus=00000010H (A4=1), BE7#-BE0#=11111011, Data bus=undefined.
5. Enter low power mode.

The rising edge of STPCLK# indicates that CPU can return to program execution at the instruction following the interrupted instruction

4.7 Hardware Limitation

If STPCLK# is configured as Throttling mode. There is a possibility for SMI to break Configuration Register Access. To elaborate, there are two steps to access Configuration registers. The first step is to program I/O port CF8 and the second one is to program I/O port CFC. If SMI routine begins to be executed between the two steps by CPU. There is possibity for PMU to cause mal-function.
The recommended solution for this problem is to read the CF8 content before executing other code in SMI routine and write back the content to CF8 before exiting SMI routine. During simulation, I observed that exiting SMI routine will issue a I/O write cycle with address CF8, data 0000. If this cycle exists in real pentium processor, a more complex SMI routine might be considered, i.e., tell wakeup events from other events....

4.8 Automatic Power Controller

Function Description:
An ATX power supply and built-in RTC are needed to make this funtion work. This power supply has a control signal ONCTL# and two set of VCC named VCC5V and AUX5V. When power is applied,then AUX5V exists but VCC5V does not until ONCTL# goes low. APC controls the signal ONCTL# to turn on or turn off VCC5V. APC has four main functions as list below.

Function 1: A button switch may power up or off system. This function is enabled in the default and can not be disabled by software method unless external RTC is trapped or pin SWITCH is connected to a pull-down resistor. A botton switch issues a high pulse which should last minumum 62.5ms. When VCC5V does not exist, a botton switch indicates a power-on system request. When VCC5V exists, a botton switch indicates a power-off system request.

Function 2: A software method can power system off. Sytem can be powered off by programming configuration register 6A bit 7,6 to '11'. This function is disabled in the default.

Function 3: A ring can power the system up. When VCC5V does not exist, issuing a ring can power system up. Some settings about RING in configuration register 6A bit 5:2 should be programmed properly before VCC5V is off. The ring pulse should last minumum 62.5ms. This function is disabled in the default.

Function 4: An alarm can power the system up.Before power is off, program configuration register 69 and 6A, and RTC ALARM bytes (address are 01h,03h,05h) properly. It is not necessarry to set AIE bit in register B of RTC. Once time and date accord

with the settings, APC will automaticlly power up the system. This function is disabled in the default.

Configuration register 6A bit 6 only controls function 2,3,4. The settings of configration register 69,6A will be kept after system power off but will be reset to default values after system power on.

5. Register Description

5.1 Memory/PCI bridge regsisters:

Register 00h Vendor ID - low byte

Bits 7:0 39h

Register 01h Vendor ID - high byte

Bits 7:0 10h

Register 02h Device ID - low byte

Bits 7:0 71h

Register 03h Device ID - high byte

Bits 7:0 55h

Register 04h Command - low byte

Bits 7:2 01h

Bit 1 MEMACC: Control a device's response to memory space accesses
0: Disable the device response
1: Allow the device response, state after PCIRST# is 0

Bit 0 1

Register 05h Command - high byte

Bits 7:2 00h

Bit 1 Fast Back-to-Back Enable

Bit 0 00h

Register 06h Status - Low Byte

Bits 7:0 00h

Register 07h Status - High Byte (default = 02h)

Bit 7 Detected Parity Error. This bit is always 0 since 5571 does not support parity checking on the PCI bus.

Bit 6 Reserved

Bit 5 Received Master Abort.
This bit is set by 5571 whenever it terminates a transaction with master abort. This bit is cleared by writing a 1 to it.

Bit 4 Received Target Abort.
This bit is set by 5571 whenever it terminates a transaction with target abort. This bit is cleared by writing a 1 to it.

Bit 3 Signaled Target Abort.

This bit is always 0 since 5571 will not terminate a transaction with target abort.

Bits 2:1 **DEVSEL# Timing DEVT.**
The two bits define the timing to assert DEVSEL#. 5571 always asserts DEVSEL# in medium timing.

Bit 0 **Reserved**

Register 08h Revision Identification.

Bits 7:0 **00h**

Register 09h Class ID

Bits 7:0 **00h**

Register 0Ah

Bits 7:0 **00h**

Register 0Bh

Bits 7:0 **06h**

Register 0Ch Cache Line Size

Bits 7:0 **00h**

Register 0Dh Master latency timer (default - 00h)

Bits 7:0 **R_MLTB[7:0]**
Master latency timer
Unit: PCLK

Register 0Eh Header Type

Bits 7:0 **00h (read only)**

Register 0Fh BIST

Bits 7:0 **00h (read only)**

Register 50h Host Interface and DRAM arbiter (default = 00h)

Bit 7 **NA# enable : pipeline address mode**
0: Disable ~~enable~~
1: E~~disable~~nable

Bit 6 **NA# asserted on All Single Write Cycle**
0: Enable (when using internal dirty SRAM) ~~disable~~
1: D~~enable (when using internal dirty SRAM)~~isable

Bit 5 **Pipeline burst SRAM back to back read timing**
0: 3-1-1-1-1-1-1-1
1: 3-1-1-1-2-1-1-1

Bit 4 **Reserved. Do not program it.**

Bit 3 **Write Merge Enable to enhance performance**
0: Disable. Recommended for 75MHz.
1: Enable. Recommended for 66MHz.

Bit 2 ~~**Reserved; this bit is programmed to 0.**~~**Read Write Reorder for DRAM arbiter**
0: Disable. Recommended for 75MHz.
1: Enable. Recommended for 66MHz.

Bit 1:0 **Reserved; this bit should be~~is~~ programmed to 0.**

~~**Bit 0 Reserved; this bit is programmed to 0.**~~

Register 51h CACHE (default = 00h)

Bit 7 **When no L2 exists, this bit should be programmed to 0.**
0: No L2 Cache
1: L2 Cache Exists

Bit 6 **L2 Cache Enable**
0: Disable
1: Enable

Bits 5:4 **L2 Cache Size**
00: R~~r~~eserved
01: 256K (default)
10: 512K
11: Reserved ~~1M~~

Bit 3 **L2 Cache WT/WB Policy**
0: Write Through Mode
1: Write Back Mode (default)

Bit 2 **L2 Cache Burst Addressing mode**
0: Toggle Mode
1: Linear Mode

Bit 1 **L2 Cache Tag Size Selection**
0: 7 bits : TA7 is dirty bit
1: 8 bits : using internal dirty SRAM

Bit 0 **L2 Cache Sizing Enable**
0: Normal Operation
1: Cache sizing mode

Register 52h (default = 00h)

Bit 7 **CPU L1 Cache Write Back Mode Enable**
0: Disable
1: Enable

Bit 6 **Turbo Read~~Reserved~~**

~~This bit is programmed to 0.~~0: For Cyrix 6x86
1: For Intel Pentium

Bit 5 **~~Read FIFO Enable~~Reserved**
~~0: Disable~~
~~1: Enable~~This bit should be always programmed to be "0".

Bit 4 **SRAM Type**
0: Pipelined Burst SRAM
1: Reserved

Bit 3 **Reserved**
This bit should be programmed to 0.

Bit 2 **Reserved**
This bit ~~i~~should~~s~~ be programmed to 0.

Bit 1 **~~REFTEST : DRAM refresh test mode~~ Reserved**

Bit 0 **~~SRAMTEST : SRAM test mode~~ Reserved**
~~0: Exit~~
~~1: Test~~

Register 53h DRAM (default = 00h)

Bit~~s~~ 7~~:6~~ **DRAM read leadoff time.**
0~~0~~: 5T
~~01: Reserved~~
1~~0~~: 4T

Bit 6 **Read after Write turn around cycle**
0: Disable
1: Enable~~11: Reserved~~

Bit 5 **Always Page Miss After ~~Code Read~~ Write DRAM Cycles**
0: Disable
1: Enable

Bit 4 **Always Page Miss After Data Read DRAM Cycles**
0: Disable
1: Enable

Bit 3 **Always Page Miss After ~~Write~~ Code Read DRAM Cycles**
0: Disable
1: Enable

Bits 2:1 **Refresh cycle time**
00: 15.6 us
01: 62.4 us
10: 124.8 us
11: 187.2 us

Bit 0 **Reserved**

Register 54h FP/EDO (default = 54h)

Bits 7:6 RAS pulse width when refresh
00: 3T
01: 4T
10: 5T
11: 6T

Bits 5:4 RAS precharge time
00: 2T
01: 3T
10: 4T
11: Reserved

Bits 3:2 RAS to CAS delay
00: 2T
01: 3T, for 66MHZ. -6 DRAM
10: 4T, for -7 DRAM
11: Reserved

Bit 1 CAS[7:0]# active Low pulse width for FP DRAM
0: 2T
1: 1T

Bit 0 ~~CAS[7:0]# active low pulse width for EDO DRAM~~This bit can only be programmed to "1".
~~0: 2T~~
~~1: 1T~~

Register 55h (default = 00h)

Bit 7 RAMW# assertion timing
0: normal
1: faster 1T

Bit 6 EDO test mode
0: Normal mode
1: Test mode (for DRAM sizing)

Bit 5 EDO Back-to-Back Timing
0: 3T
1: 2T

Bits 4:3 Reserved

Register 56h MDLE delay

Bits 7:3 Reserved

Bits 2:0 MDLE Delay

000 : 0 ns	001 : 1 ns
010 : 2 ns	011 : 3 ns

100 : 4 ns 101 : 5 ns
110 : 6 ns 111 : 7 ns
NOTE: Recommended value: 011

Register 57h SDRAM

Bit 7 **R_PRCH:Precharge Command**
0: Disable
1: Enable
(After the cycle completes, this bit will be cleared automatically.)

Bit 6 **R_MRS:Mode Register Set Command**
0: Disable
1: Enable

Bit 5 **R_SCBR: for SDRAM sizing Refresh Command**
0: Disable
1: Enable
(After the cycle completes, this bit will be cleared automatically.)

Bit 4 **CAS Latency**
0: 2T
1: 3T

Bit 3 **SDRAM write retire rate**
0: X-2-2-2
1: X-1-1-1

Bits 2:0 **Reserved**

Register 58h **Reserved. Do not program it.~~DRAM timing adjustment~~**

~~**Bits 7:4 CAS# Delay**~~

~~**Bits 3:0 MDLE Delay**~~

~~0000 : No delay 0001 : delay 1 ns~~
~~0010 : delay 2 ns 0011 : delay 3 ns~~
~~0100 : delay 4 ns 0101 : delay 5 ns~~
~~0110 : delay 6 ns 0111 : delay 7 ns~~
~~1000 : delay 8 ns 1001 : delay 9 ns~~
~~1010 : delay 10 ns 1011 : delay 11 ns~~
~~1100 : delay 12 ns 1101 : delay 13 ns~~
~~1110 : delay 14 ns 1111 : delay 15 ns~~

Register 59h Buffer strength and current rating (default = 00h)

Bit 7 **Selection of RAS[5:0]# Current Rating**

Bit 6 **Selection of CAS[7:0]# Current Rating**

Bit 5 **Selection of MA[11:2] Current Rating**

Bit 4 **Selection of MA[1:0]A Current Rating**

Bit 3 **Selection of MA[1:0]B Current Rating**

Bit 2 **Selection of RAMWA# Current Rating**

Bit 1 **Selection of RAMWB# Current Rating**

Bit 0 **Selection of the above Buffer Strength**

Current rating

0: 8mA

1: 16mA

Buffer strength

0: 5V

1: 3.3V

Register 5Ah

Bit 7:2 **Reserved**

Bit 1: Selection of AD[31:0] Current Rating

0: 8mA

1: 16mA

Bit 0: Selection of FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, PAR, C/BE[3:0]# and GNT[4:0]# Current Rating

0: 8mA

1: 16mA

Register 5Bh:5Fh

Bits 7:0 **Reserved**

Register 80h PCI master characteristics

Bits 7:5 **Maximum burstable address range in PCI master accessing main memory when 32-bit DRAM organization is employed with 256K or 512K type DRAM maximum burstable range reduces to 2KB only because the physical page size is 2KB in this situation. Thus, never program these bits to 4KB in 32 bit DRAM orgranization.**

000: 256B

001: 512B

010: 1KB

011: 2KB

100: 4KB

others: reserved

Bit 4 **TRDY# assertion timing in PCI master read cycle**

0: Assert TRDY# after prefetching two QWs

1: Assert TRDY# after prefetching one Qws

Bit 3 **Advanced snoop in PCI master write cycle**
0: Disable
1: Enable

Bit 2 **Advanced snoop in PCI master read cycle**
0: Disable
1: Enable

Bit 1 **PCI bus using synchronous mode**
0: Disable (default)
1: Enable

Bit 0 **Reserved**

Register 81h

Bit 7 **The timing for 5571 to prefetch FP DRAM data to CTPFF (CPU to PCI FIFO).**
0: 1 CPUCLK delay from the assertion of CAS# (recommended in 50Mhz)
1: 2 CPUCLK delay from the assertion of CAS# (recommended in 60/66Mhz)

Bit 6 **The timing for 5571 to prefetch EDO DRAM data to CTPFF**
0: 1 CPUCLK delay from the assertion of CAS# (recommended in 50Mhz)
1: 2 CPUCLK delay from the assertion of CAS# (recommended in 60/66Mhz)

Bit 5 **Reserved**

Bit 4 **Reserved**
This bit must be programmed to "0". ~~The timing for 5571 to prefetch Synchronous DRAM data to CTPFF~~
~~0: 1 CPUCLK delay from the time of valid data output (default)~~
~~1: 0 at the time of valid data output~~

Bit 3 **Synchronous DRAM burst read in PCI master read cycle**
0: Disable (default)
1: Enable

Bit 2 **Enable CPU to L2/DRAM and PCI Peer-to-Peer concurrency mode**
0: Disable
1: Enable

Bit 1 **Reserved**
This bit must be programmed to "0".

~~**Enable CPU to L2/DRAM and 5571 to PCI Peer-to-Peer concurrency mode**~~
~~0: Disable~~
~~1: Enable~~

Bit 0 **Reserved**

Register 82h

Bit 7 **PCI master write main memory cycles**

0: faster (default)

1: slower

Bit 6 **PEADS timing control in PCI master to main memory cycles**

When PCI master initiating memory cycle, SiS 5571 will check ROW address on the CPU clock rising edage that PEADS is active. PEADS is expected as the first EADS# of every PCI bus transaction.

0: faster (default)

1: slower

Bit 5 **Enhanced performance for the *Memory Write and Invalidate* of PCI bus command**

0: disable (default)

1: enable

Bit 4 **Read prefetch for the *Memory Read* of PCI bus command**

The *Memory Read Multiple and Memory Read Line* of PCI bus commands always do prefetch.

0: enable (default)

1: disable

Bits 3:2 **PCI Target Bridge of SiS 5571 Initial Latency Timer**

00: disable (default)

01: 16 PCI Clocks

10: 24 PCI Clocks

11: 32 PCI Clocks

Bit 1 **PCI Target Bridge of SiS 5571 Subsequent Latency Timer**

0: disable (default)

1: enable

Bit 0 **Currently this bit should be programmed with 0**

When set, the SiS 5571 timing is adjusted to serve those bus master agents that do not follow the PCI specification to have 12ns max. propagation delay time of AD in the address phase.

Register 83h CPU to PCI characteristics (default 00)

Bit 7 **Fast gate A20 emulation**

0: Disable

1: Enable (recommanded)

Bit 6 **Fast reset emulation**

0: Disable

1: Enable (recommanded)

Bit 5 **Fast reset latency control**

0: 2us ~~6us~~

1: ~~2us~~6us

Bit 4 **Fast back-to-back function when the PCI cycle hit IDE or prefetchable area.**

Bit 3 **CPU to PCI post write rate control**
0: 4T
1: 3T (recommanded)

Bit 2 **IDE Data port post write function**
0: Disable
1: Enable (recommanded)

Bit 1 **CPU to PCI burst memory write**
0: Disable
1: Enable (recommanded)

Bit 0 **CPU to PCI post write function**
0: Disable
1: Enable (recommanded)

Register 84h

Bits 7:0 **R_PGTB[15:0] -- Low byte**
PCI Grant Timer
Unit: PCLK

Register 85h PCI grant timer

Bits 7:0 **R_PGTB[15:0] -- High byte**
Unit: PCLK

Register 86h CPU idle timer

Bits 7:0 **R_CITB[7:0]**
CPU idle timer
Unit:PCLK

Register 87h Miscellanea (default 00)

Bit 7 **CPU to PCI Bridge Synchronous Mode**
0: Disable
1: Enable

Bit 6 **This bit should be programmed to "0".~~CPU involve arbitration~~**
~~0: Disable~~
~~1: Enable (recommanded)~~

Bit 5 **The latency of ADS# to FRAME#**
0: Normal
1: Fast

Bit 4 **PGT Testing Mode**

0: Disable
1: Enable

Bit 3 **2nd Half PCI Cycle of a 64-bit Access Retried Bahavior**
0: Restart the cycle until success
1: Backoff CPU

Bits 2:0 **Reserved**

Register 8Ch~8Fh **General Purpose Register**

Bits 7:0 **Reserved**

Following two registers mainly defines the enable bits for the events monitored by System Standby timer. If any monitored event occurs during the programmed time, the System standby timer will be reloaded and starts to count down again.

Register 90h PMU control register

Bit 7 **Hard Disk Port 1 Enable**
When set, any I/O access to the Hard Disk port 1 (1F0-1F7h or 3F6h) will cause the System Standby timer be reloaded.

Bit 6 **Keyboard port Enable**
When set, any I/O access to the keyboard Ports (60h or 64h) will cause the System Standby timer be reloaded.

Bit 5 **Serial Port 1 Enable**
When set, any I/O access to the Serial Ports (3F8-3FFh or 3E8-3EFh) will cause the System Standby timer be reloaded.

Bit 4 **Serial Port 2 Enable**
When set, any I/O access to the Serial Ports (2F8-2FFh or 2E8-2EFh) will cause the System Standby timer be reloaded.

Bit 3 **Parallel Port Enable**
When set, any I/O access to the Parallel ports (278-27Fh, 378-37Fh or 3BC-3BEh) will cause the System Standby timer be reloaded.

Bit 2 **Hold Enable**
When set, any event from the ISA master or the PCI Local Master will cause the System Standby timer be reloaded.

Bit 1 **IRQ1~15, NMI**
When set, any event from the IRQ1-15 or NMI will cause the System Standby timer be reloaded.

Bit 0 **Monitor Ring event enable**
If this bit is set, an event from the RING# will cause the System Standby timer be reloaded.

Register 91h Address trap for green function

Bit 7 **Programmable 10 bit I/O Port Enable**
When set, any I/O access to the address will cause the System Standby timer be reloaded. The address is defined in Registers 96h and 97h.

Bit 6 **Programmable 16 bit I/O Port Enable**
When set, any I/O access to the address will cause the System Standby timer be reloaded. The address is defined in Registers 98h and 99h.

Bit 5 **A0000h - AFFFFh or B0000 - BFFFFh Address trap**
When set, any memory access to the address range will cause the System Standby timer to be reloaded.

Bit 4 **C0000h - C7FFFh Address trap**
When set, any memory access to the address range will cause the System Standby timer to be reloaded.

Bit 3 **3B0-3BFh, 3C0-3CFh, 3D0-3DFh Address trap**
When set, any I/O access to the I/O addresses will cause the System Standby timer to be reloaded.

Bit 2 **Secondary Drive port**
When set, any I/O access to the secondary drive port (170-17Fh, 320-32Fh, 3F7h) will reload the system standby timer.

Bits 1:0 **System Standby Timer Slot**
11 : 8.85 milli seconds
10 : 70 milli seconds
01 : 1.1 seconds
00 : 9 seconds

Register 92h

Bits 7:5 Define the events monitored by the Monitor standby timer .
Bits 4:2 Define the events to break the Monitor and System standby state.
Bits 1:0 Define the events to de-assert the STPCLK#.

Bit 7 **IRQ 1-15, NMI**
When set, any event from the IRQ1-15 or NMI will cause the Monitor standby timer be reloaded.

Bit 6 **HOLD**
When set, any event from the ISA master or the PCI local master will cause the Monitor standby timer be reloaded.

Bit 5 **Reload Monitor Timer From Ring#**
When set, Monitor standby timer will be reloaded when Ring# is asserted.

Bit 4 **IRQ 1-15, NMI**
When enabled, any event from the IRQ1-15 or NMI will bring the Monitor back to the Normal state from the Standby state.

Bit 3 **HOLD**

When enabled, any event from the ISA master or the PCI local master will bring the Monitor back to the Normal state from the Standby state.

Bit 2 **Ring Wakeup Enable**

If this bit is set, it will bring the Monitor back to the Normal state from the Standby state when Ring# is asserted.

Bit 1 **IRQ 1-15, NMI**

When enabled, any event from the IRQ1-15 or NMI will de-assert the STPCLK#.

Bit 0 **HOLD**

When enabled, any event from the ISA master or the PCI local master will de-assert the STPCLK#.

Register 93h STPCLK# and APM SMI control

Bit 7 **INIT**

When enabled, an event from the INIT will de-assert the STPCLK#.

Bit 6 **Ring Wakeup Enable**

When enabled, system will wake up from standby mode to de-assert the STPCLK# when Ring# is asserted.

Bit 5 **STPCLK# Enable**

When set, writing a '1' to bit 3 of Register 93h will cause the STPCLK# to become active. This bit can be cleared.

Bit 4 **Throttling Enable**

When set, writing a '1' to bit 3 of Register 93h will cause the STPCLK# throttling state to become active. The throttling function can be disabled by clearing this bit.

Bit 3 **STPCLK# Control**

When this bit is set, the STPCLK# will be asserted or the Throttling function will be enabled depending on bits 5 and 4. If both bits 5 and 4 are enabled, the system will do the throttling function.

Bit 2 **The function of Break SW./TURBO selection**

0: TURBO

1: BREAK#

The Break SW. disable function can be done by programming register 9Bh bit 1 to "0".

Bit 1 **APM SMI**

When Register 9Bh bit 0 is enabled, and a '1' is written to this bit, an SMI is generated. It is used by the software controlled SMI function like APM. This bit should be cleared at the end of the SMI handler.

Bit 0 **Deturbo function**

0: Disable

1: Enable

Register 94h 6x86 and Green function control

Bit 7 **6x86 SMAC access**

It must be set whenever the 6x86 CCR1 bit 2 is set and cleared if CCR1 bit 3 is cleared.

Bit 6 **6x86 MMAC access**

If set, access to address within SMM space is conducted to main memory instead of SMM area. It must be set whenever the 6x86 CCR1 bit 3 is set and cleared if CCR1 bit 3 is cleared.

In the 6x86's specification, the SMIACT will be de-asserted when MMAC is set and re-asserted after it is cleared. This allows the SMI service routine to access normal memory area instead of SMM memory area.

Bit 5 **6x86 CPU**

It should be set if the current CPU is 6x86.

Bit 4 **Break SW. Wakeup capability**

0: Enable

1: Disable

Bit 3 **Flush Function Block Mode**

It is suggested to block the FLUSH (Deturbo Mode) when the STPCLK is asserted.

0: Un-block

1: Block

Bit 2:0 **Reserved**

Register 95h Test mode control (internal use only)

Bit 7 **IRQ SMI enable.**

When set, any unmasked event defined at PCI to Isa configuration Register 72h-73h will cause the SMI to be generated.

Bit 6 **IRQ SMI status.**

This bit is set when the bit 7 of this Register is enabled and the corresponding event is active.

Bit 5

When this bit is set under throttling mode, the STPCLK will be de-asserted and SMI# is asserted if R96 bit 4 is enabled.

Bit 4 **USB SMI enable**

When this bit is set, a SMI# can be generated by USB controller.

Bit 3 **USB SMI request.**

This is an USB SMI Request start bit. When the bit 4 of this register is set and the USB controller asserts a controll signal to generated SMI#, this bit is set.

Bit 2 **Reserved**

Bits 1:0 **PMU test mode**

00: Normal operation

01: counter test mode

10: Fast test mode

Register 96h Time slot and Programmable 10-bit I/O port definition

Bits 7:6 Define the time slot of the Monitor Standby timer
00 : 6.6 seconds
01 : 0.84 seconds
10 : 13.3 milli-seconds
11 : 1.6 milli-seconds

Bits 5:3 Programmable 10-bit I/O port address mask bits
000 : No mask
001 : A0 masked
010 : A1-A0 masked
011 : A2-A0 masked
100 : A3-A0 masked
101 : A4-A0 masked
110 : A5-A0 masked
111 : A6-A0 masked

Bit 2 Reserved

Bits 1:0 Programmable 10-bit I/O port address bits A1, A0.
Bits 1:0 correspond to the address bits A1 and A0.

Register 97h programmable 10-bit I/O port address

Bits 7:0 Bits 7:0 define the programmable 10-bit I/O port address bits A[9:2].

Register 98h Programmable 16-bit I/O port

Bits 7:0 define the low byte of the Programmable 16-bit I/O port.

Following two registers define the enable status of the devices in SMM. The bits are set when the devices are in standby state and cleared when the respective devices are in normal state.

Register 99h

Bits 7:0 define the high byte of the Programmable 16-bit I/O port.

Register 9Ah

Bit 7 System Standby SMI enable
When no non-masked event occurs during the programmed duration of the system standby timer, the timer expires. If this bit is enabled, the SMI# is generated and the system enters the System Standby state.

Bit 6 Programmable 10-bit I/O port wake up SMI enable

When set, any I/O access to this port will be monitored to generate the SMI# to wake up this I/O port from the standby state to the Normal state. This bit is enabled only when the I/O port is in the Standby state.

Bit 5 **Programmable 16-bit I/O port wake up SMI enable**

When set, any I/O access to this port will be monitored to generate the SMI# to wake up this I/O port from the standby state to the Normal state. This bit is enabled only when the I/O port is in the Standby state.

Bit 4 **Parallel ports wake up SMI enable**

When set, any I/O access to the parallel ports will be monitored to generate the SMI# to wake up the parallel ports from the standby state to the Normal state. This bit is enabled only when the parallel ports are in the Standby state.

Bit 3 **Serial port 1 wake up SMI enable**

When set, any I/O access to the serial port 1 will be monitored to generate the SMI# to wake up the serial ports from the standby state to the Normal state. This bit is enabled only when the serial port 1 are in the Standby state.

Bit 2 **Serial port 2 wake up SMI enable**

When set, any I/O access to the serial port 2 will be monitored to generate the SMI# to wake up the serial ports from the standby state to the Normal state. This bit is enabled only when the serial port 2 are in the Standby state.

Bit 1 **Hard Disk port 1 SMI enable**

When set, any I/O access to the hard disk port 1 will be monitored to generate the SMI# to wake up the hard disk from the standby state to the Normal state. This bit is enabled only when the hard disk port 1 is in the Standby state.

Bit 0 **Hard Disk port 2 SMI enable**

When set, any I/O access to the hard disk port 2 will be monitored to generate the SMI# to wake up the hard disk from the standby state to the Normal state. This bit is enabled only when the hard disk port 2 is in the Standby state.

Register 9Bh

Bit 7 **Monitor Standby SMI enable**

0 : Disable

1 : Enable

When there is no access from the IRQ1-15, HOLD, Ring# and NMI during the programmed time of the Monitor Standby Timer, the timer expires. If this bit is set, an SMI is generated to bring the Monitor to the standby state.

Bit 6 **Monitor wake up SMI enable**

When set, any event from the IRQ1-15, HOLD, Ring# or NMI will be monitored to generate the SMI# to wake up the monitor from the standby state to the normal state.

Bit 5 **Throttling wake up SMI enable**

When set, any unmasked event from the NMI, INIT, IRQ1-15, Break switch, Ring# or HOLD will cause an SMI to be generated to bring the system back to the Normal state from the throttling state.

Bit 4 **System wake up SMI enable**
When set, any unmasked event from the NMI, INIT, IRQ1-15, Break switch, Ring# or HOLD will cause an SMI to be generated to bring the system back to the Normal state from the standby state.

Bit 3 **Keyboard wake up SMI enable**
When set, any I/O access to the keyboard ports will be monitored to generate the SMI# to wake up the keyboard ports from the standby state to the Normal state. This bit is enabled only when the keyboard ports are in the Standby state.

Bit 2 **Ring# SMI enable**
If this bit is set, it enables the SMI request from Ring# activity.

Bit 1 **Break Switch SMI enable**
When set, the break switch can be pressed to generate the SMI# for the system to enter the Standby state.

Bit 0 **Software SMI enable**
When set, an I/O write to bit 1 of register 93h will generate an SMI.

Following two registers define the SMI request status. If the respective SMI enable bit is set, each specific event will cause the respective bit to be set. The asserted bit should be cleared at the end of the SMI handler.

Register 9Ch

Bit 7 **System Standby SMI request**
This bit is set when the system standby timer expires.

Bit 6 **Programmable 10-bit I/O port wake up request**
This bit is set when there is an I/O access to the port.

Bit 5 **Programmable 16-bit I/O port wake up request**
This bit is set when there is an I/O access to the port.

Bit 4 **Parallel ports wake up request**
This bit is set when the parallel ports are accessed.

Bit 3 **Serial port 1 wake up request**
This bit is set when the serial port 1 are accessed.

Bit 2 **Serial port 2 wake up request**
This bit is set when the serial port 2 are accessed.

Bit 1 **Hard Disk port 1 wake up request**
This bit is set when the hard disk port 1 is accessed.

Bit 0 **Hard Disk port 2 wake up request**
This bit is set when the hard disk port 2 is accessed.

Register 9Dh

Bit 7 **Monitor Standby SMI request**
This bit is set when the Monitor Standby Timer expires. This bit should be cleared at the end of the SMI handler.

Bit 6 **Monitor wake up request**
This bit is set when there is an event from the IRQ1-15, HOLD or NMI, and the Monitor is in the standby state.

Bit 5 **Throttling wake up SMI request**
This bit is set when there is any unmasked event from the NMI, INIT, IRQ1-15, or HOLD when the system is in the throttling state.

Bit 4 **System wake up SMI request**
This bit is set when there is any unmasked event from the NMI, INIT, IRQ1-15, or HOLD when the system is in the standby state.

Bit 3 **Keyboard ports wake up request**
This bit is set when the keyboard ports are accessed.

Bit 2 **SMI request from Ring#**
This bit is set when there is Ring# activity.

Bit 1 **Break Switch SMI request**
This bit is set when the break switch is pressed.

Bit 0 **Software SMI request**
This bit is set when an I/O write to the bit 1 of register 93h and bit 0 of register is 1.

Register 9Eh STPCLK# Assertion Timer (default = 0FFh)

Bits 7:0 **This register defines the period of the STPCLK# assertion time.**
Bits[7:0] define the period of the STPCLK# assertion time when the STPCLK# enable bit is set. The timer will not start to count until the Stop Grant Special Cycle is received. The timer slot is 35 us.

Register 9Fh STPCLK# De-assertion Timer (default = 0FFh)

Bits 7:0 **This register defines the period of the STPCLK# de-assertion time.**
Bits[7:0] define the period of the STPCLK# de-assertion time when the STPCLK# enable bit is set. The timer starts to count when the STPCLK# assertion timer expires. The timer slot is 35us.
When these two registers are read, the current values are returned.

Monitor Standby timer (default = 0FFh)
It is a count-down timer and the time slot is programmable for 6.6s, 0.84s, 13.3 ms or 1.6ms. The value programmed to this register is loaded when the timer is enabled and the timer starts counting down. The timer is reloaded when an event from the IRQ1-15, HOLD or NMI occurs before the timer expires. When this register is read, the current value is returned.

Register A0h

Bits 7:0 **Define the low byte of the Monitor standby timer.**

Register A1h

Bits 7:0 Define the high byte of the Monitor standby timer.

Register A2h System Standby Timer (default = 0FFh)

Bits 7:0 The register defines the duration of the System Standby Timer.
When the System Standby Timer expires, the system enters System Standby State. If any non-masked event occurs before the timer expires, the timer is reloaded with programmed number and the timer starts counting down again.

Register A3h SMRAM access control and Power supply control (default = 00h)

Bits 7:6 R_SMRAM[1:0] : SMRAM
00: EL to EL(32K)
01: EL to AL(32K)
10: EL to BL(32K)
11: A to A(64K)

Bit 5 Reserved

Bit 4 SMRAMEN : SMRAM Access Control
1: When set, the SMRAM area can be used. This bit can be set whenever it is necessary to access the SMRAM area. It is cleared after the access is finished.
0: The SMRAM area can only be accessed during the SMI handler.

Bits 3:0 Reserved

Register CF9h — Reset control register

Bits 7:5 Reserved

Bit 4 INITEN
INIT enable
1: Drives INIT during S/W reset
0: Drives CPURST during S/W reset and INIT is inactive.

Bits 3:~~2~~0 Reserved

~~**Bit 1 RSTEN**~~
~~Enable System Hard Reset~~

~~**Bit 0 Reserved**~~

(Register 70h to register 76h define the attribute of the Shadow RAM from 640 KByte to 1 MByte. All of the registers 70h to 75h are defined as below, and each register defines the corresponding memory segment's attribute which are listed in the following table.)

Register	Defined Range	Register	Defined Range
register 70h bits 7:5	0C0000h-0C3FFFh	register 73h bits 7:5	0D8000h-0DBFFFh

register 70h bits 3:1	0C4000h-0C7FFFh	register 73h bits 3:1	0DC000h-0DFFFFh
register 71h bits 7:5	0C8000h-0CBFFFh	register 74h bits 7:5	0E0000h-0E3FFFh
register 71h bits 3:1	0CC000h-0CFFFFh	register 74h bits 3:1	0E4000h-0E7FFFh
register 72h bits 7:5	0D0000h-0D3FFFh	register 75h bits 7:5	0E8000h-0EBFFFh
register 72h bits 3:1	0D4000h-0D7FFFh	register 75h bits 3:1	0EC000h-0EFFFFh
REGC04 : register 70h		**REGC8C** : register 71h	
REGD04 : register 72h		**REGD8C** : register 73h	
REGE04 : register 74h		**REGE8C** : register 75h	
REGF : register 76h			

Register 70h~75h

Bit 7 **Read enable**
Bit 6 **L1/L2 cacheable**
Bit 5 **Write enable**
Bit 4 **Reserved**
Bit 3 **Read enable**
Bit 2 **L1/L2 cacheable**
Bit 1 **Write enable**
Bit 0 **Reserved**

Register 76h Attribute of shadow RAM for BIOS area (default = 00h)

Bit 7 **Read enable for shadow RAM of BIOS area 0F0000-0FFFFFh**
Bit 6 **L1/L2 cacheable for shadow RAM of BIOS area 0F0000-0FFFFFh**
Bit 5 **Write enable for shadow RAM of BIOS area 0F0000-0FFFFFh**
Bit 4 **Reserved**
Bit 3 **Shadow RAM enable for PCI**
Bits 2:0 **Reserved**

Register 77h Characteristics of non-cacheable area (default = 00h)

Bits 7:4 **Reserved**
Bit 3 **NCA1REG0[1] : Allocation of Non-Cacheable Area I**
0: Local DRAM
1: PCI Bus. The local DRAM is disabled.
Bit 2 **NCA1REG0[0] : Non-Cacheable Area I Enable**
0: Disable
1: Enable

Bit 1 **NCA2REG0[1] : Allocation of Non-Cacheable Area II**
0: Local DRAM
1: PCI Bus. The local DRAM is disabled.

Bit 0 **NCA2REG0[0] : Non-Cacheable Area II Enable**
0: Disable
1: Enable

Register 78h Allocation of Non-Cacheable area #1 (NCA1REG1 default = 00h)

Bits 7:5 **Size of Non-Cacheable Area I (within 384 MBytes)**

000: 64KB	100: 1MB
001:128KB	101: 2MB
010: 256KB	110: 4MB
011: 512KB	111: 8MB

Bits 4:0 **A28~A24 of Non-Cacheable Area I (within 384 Mbytes)**

Register 79h NCA1REG2 (default = 00h)

Bits 7:0 **A23~A16 of Non-Cacheable Area I (within 384 Mbytes)**

Register 7Ah Allocation of Non-Cacheable area #2 (NCA2REG1 default = 00h)

Bits 7:5 **Size of Non-Cacheable Area II (within 384 MBytes)**

000: 64KB	100: 1MB
001: 128KB	101: 2MB
010: 256KB	110: 4MB
011: 512KB	111:8MB

Bits 4:0 **A28~A24 of Non-Cacheable Area II (within 384 Mbytes)**

Register 7Bh NCA2REG2 (default = 00h)

Bits 7:0 **A23~A16 of Non-Cacheable Area II (within 384 Mbytes)**

Register 7Ch~7Fh

Bits 7:0 **Reserved**

6. PCI/ISA System I/O (PSIO)

6.1 Functional Description

As a PCI slave, PSIO responds to both I/O and memory transfers. PSIO always target-terminates after the first data phase for any bursting cycle.

The PSIO is assigned as the subtractive decoder in the Bus 0 of the PCI/ISA system by accepting all accesses not positively decoded by some other agent. In reality, the PSIO only subtractively responds to low 64K I/O or low 16M memory accesses. PSIO also positively decodes I/O addresses for internal registers, and BIOS memory space by asserting DEVSEL# on the medium timing.

As a PCI master, the PCI master bridge on behalf of DMA devices or ISA Masters starts to drive the AD bus, C/BE[3:0]# and PAR signal. When MRDC# or MWTC# is asserted, the PSIO will generate FRAME#, and IRDY# to PCI bus if the targeted memory is not on the ISA side. The valid address and command are driven during the address phase, and PAR is asserted one clock after that phase. PSIO always activated FRAME# for 2 PCLKs because it does not conduct any bursting cycle.

The ISA address decoder is used to determine the destination of ISA master or DMA devices. This decoder provides the following options as they are defined in configuration registers 48 to 4B.

a. Memory: 0-512K
b. Memory: 512K-640K
c. Memory: 640K-768K(video buffer)
d. Memory: 768K-896K in eight 16K sections(Expansion ROM)
e. Memory: 896K-960K(lower BIOS area)
f. Memory: 1M-XM-16M within which a hole can be opened. Access to the hole is not forwarded to PCI bus.
g. Memory:>16M automatically forwards to PCI.

6.1.1 ISA Bus Controller

The SiS5571 ISA Bus Interface accepts those cycles from PCI bus interface and then translates them onto the ISA bus. It also requests the PCI master bridge to generate PCI cycle on behalf of DMA or ISA master. The ISA bus interface thus contains a standard ISA Bus Controller (IBC) and a Data Buffering logic. IBC provides all the ISA control, such as ISA command generation, I/O recovery control, wait-state insertion, and data buffer steering. The PCI to/from ISA address and data bus bufferings are also all integrated in SiS5571. The SiS5571 can directly support 4 ISA slots without external data or address buffering.

Standard ISA bus refresh is requested by Counter 1, and then performed via the IBC. IBC generates the pertinent command and refreshes address to the ISA bus. Since the ISA refresh is transparent to the PCI bus and the DMA cycle, an arbiter is employed to resolve the possible conflicts among PCI cycles, refresh cycles, and DMA cycles.

6.1.2 DMA Controller

The SiS5571 contains a seven-channel DMA controller. The channel 0 to 3 is for 8-bit DMA devices while channel 5 to 7 is for 16-bit devices. The channels can also be programmed for any of the four transfer modes, which include single, demand, block, and cascade. Except in cascade mode, each of the three active transfer modes can perform three different types of transfers, which include read, write, and verify. The address generation circuitry in SiS5571 can only support 24-bit address for DMA devices.

6.1.3 Interrupt Controller

The SiS5571 provides an ISA compatible interrupt controller that incorporates the functionality of two 82C59 interrupt controllers. The two controllers are cascaded so that 14 external and two internal interrupts are supported. The master interrupt controller provides IRQ<7:0> and the slave one provides IRQ<15:8>. The two internal interrupt are used for internal functions only and are not available externally. IRQ2 is used to cascade the two controllers together and IRQ0 is used as a system timer interrupt and is tied to interval Counter 0. The remaining 14 interrupt lines are available for external system interrupts.

Priority	Label	Controller	Typical Interrupt Source
1	IRQ0	1	Timer/Counter 0 Out
2	IRQ1	1	Keyboard
3-10	IRQ2	1	Interrupt from Controller 2
3	IRQ8#	2	Real Time Clock
4	IRQ9	2	Expansion bus pin B04
5	IRQ10	2	Expansion bus pin D03
6	IRQ11	2	Expansion bus pin D04
7	IRQ12	2	Expansion bus pin D05
8	IRQ13	2	Coprocessor Error Ferr#
9	IRQ14	2	Fixed Disk Drive Controller Expansion bus pin D07
10	IRQ15	2	Expansion bus pin D06
11	IRQ3	1	Serial port 2, Expansion Bus B25
12	IRQ4	1	Serial port 1, Expansion Bus B24
13	IRQ5	1	Parallel Port 2, Expansion Bus B23
14	IRQ6	1	Diskette Controller, Expansion Bus B22
15	IRQ7	1	Parallel Port, Expansion Bus B21

In addition to the ISA features, the ability to do interrupt sharing is included. Two registers(ECLR) located at 4D0h and 4D1h are defined to allow edge or level sense selection to be made on an individual channel by channel basis instead of on a complete bank of channels. Note that the default of IRQ0, IRQ1, IRQ2, IRQ8# and IRQ13 is edge sensitive, and can not be programmed. Also, each PCI Interrupt(INTx#) can be programmed independently to route to one of the eleven ISA compatible interrupts(IRQ<7:3>, IRQ<15:14>, and IRQ<12:9>) through configuration registers 41h to 44h.

6.1.4 Timer/Counter

The SiS5571 contains 3 channel counter/timer that is equivalent to those found in the 82C54 programmable interval timer. The counters use a division of 14.318MHz OSC input as the clock source. The outputs of the timers are directed to key system functions. Counter 0 is connected to the interrupt controller IRQ0 and provides a system timer interrupt for a time-of-day, diskette time-out, or the other system timing function. Counter 1 generates a refresh-request signal and Counter 2 generates the tone for the speaker.

6.1.5 Built-in RTC

The 5571 incorporates a real-time clock and system configuration memory. The RTC combines:

- A complete time-of-day clock with alarm
- 100 year calendar
- Programmable periodic interrupt
- 14 bytes of clock and control registers and 242 bytes of lower power general purpose SRAM

The method of accessing the upper 128 bytes of CMOS SRAM is to set 45h bit 3.
The last byte of upper 128 bytes is internally used and can not be accessed.

6.1.6 Built-in PCI Master/Slave IDE

Design of the built-in PCI IDE follows the PCI Local Bus Specification and PCI IDE Controller Specification.

Both primary and secondary channel may be programmed as Native mode or Compatibility mode via the Class Code Field in the controller's Configuration Space register.

In Compatibility mode, the interrupt requests for channel 0 and channel 1 are rerouted to IRQ 14 and IRQ 15 of the built-in Interrupt Controller.

Following table illustrates the accessing methods to the I/O ports in compatibility mode:

Primary Channel:

			READ		WRITE	
PORT	IDECS1#	IDECS0#	DIOR0#	DIOR1#	DIOW0#	DIOW1#
1F0	1	0	0	1	0	1
1F1	1	0	0	1	0	1
1F2	1	0	0	1	0	1
1F3	1	0	0	1	0	1
1F4	1	0	0	1	0	1
1F5	1	0	0	1	0	1
1F6	1	0	0	1	0	1
1F7	1	0	0	1	0	1
3F6	0	1	0	1	0	1

Secondary Channel:

			READ		WRITE	
PORT	IDECS1#	IDECS0#	DIOR0#	DIOR1#	DIOW0#	DIOW1#
170	1	0	1	0	1	0
171	1	0	1	0	1	0
172	1	0	1	0	1	0
173	1	0	1	0	1	0
174	1	0	1	0	1	0
175	1	0	1	0	1	0
176	1	0	1	0	1	0
177	1	0	1	0	1	0
376	0	1	1	0	1	0

In Native mode, the interrupt requests of both channels share the same PCI interrupt pin. The interrupt pin may be rerouted to any one of eleven ISA compatible interrupts (IRQ[15:14], IRQ[12:9], and IRQ[7:3]) via programming 5571 Configuration Register 63h.

Meanwhile, accessing of the I/O ports are via the addresses programmed in Base Address Registers 10h, 14h, 18h and 1Ch in IDE configuration space.

While serving as a bus master device, the IDE controller may transfer data between IDE devices and main memory directly. By performing the DMA transfer, IDE offloads the CPU and improves system performance. Bus master DMA programming is according to the information specification "Programming Interface for Bus Master IDE Controller".

The built-in IDE controller contains PCI configuration header and registers to meet PCI specifications. The internal PCI IDE supports PCI type 0 configuration cycles of configuration mechanism #1.

Proper cycle timing is generated to fit PCI Bus speed and different modes of IDE drive. All cycle timing can be controlled by software programming.

As a slave device, IDE decodes and interprets PCI cycles and generate signals to start and terminate IDE cycles. This block responds only to cycles that belong to IDE I/O address space. It supports both 16-bit and 32-bit I/O data transfer at address 1F0/170. All other IDE registers read or write operations are 8-bit only.

There are two 8×32 bits FIFOs, which support post write and pre-fetch operations, in the internal PCI IDE. Prefetch and post write operations for each channel may be activated via Register 4B in IDE Configuration Space. The two FIFOs may operate independently.

The posted write operations can enhance the transfer rate of the PCI Bus interface to IDE interface write operation by decoupling the wait-states effect from the slower IDE side to the faster PCI Bus side.

The prefetch operations can eliminate the idle cycle of the PCI Bus side to improve read operation.

6.1.7 USB Host Controller

The SiS5571 USB Host Controller can be programmed via PCI interface. It may also generate

PCI master cycle to access system memory.
It will take the responsiblilty to manage the activitites on the USB buses attached to its ports.

The USB bus is a cable bus that supports data exchange between a host computer and a wide range of simultaneously accessible peripherals. The attached peripherals share USB bandwidth through a token scheduled protocol. The bus allows pheripherals to be attached, configured, used, and detached while the host is in operation.

To support applications and drivers in non-USB aware environment(e.g. DOS) the Host Controller provides some amount of hardware support for the emulation of a PS/2 keyboard and mouse by their USB equivalente (USB keyboard, mouse). This emulation support is provided by a set of registers that are controlled by code running in SMM.

6.2 PCI Configuration Register (PCI to ISA Bridge)

Registers 00h, 01h Vendor ID

Bits 15:0 = 1039h (Read Only)

Registers 02h, 03h Device ID

Bits 15:0 = 0008h (Read Only)

Registers 04h, 05h Command = 07h

Bits 15:4 Reserved. Read as 0's

Bit 3 Monitor Special Cycle Enable = 0

Bit 2 Behave as Bus Master Enable = 1

Bit 1 Respond to Memory Space Accesses ~~= 1~~

This bit must be programmed to "1".

Bit 0 Respond to I/O Space Accesses ~~= 1~~

This bit must be programmed to "1".

Registers 06h, 07h Status

Bits 15:14 Reserved. Read as 0's

Bit 13 Received Master-Abort

When the 5571 generates a master-abort, this bit is set to a 1. This bit is cleared to 0 by writing a 1 to this bit.

Bit 12 Received Target-Abort

When the 5571 receives a target-abort, this bit is set to a 1. Software clears this bit to 0 by writing a 1 to this bit location.

Bit 11 Reserved. Read as a 0

Bits 10:9 DEVSEL# Timing

The 5571 always generates DEVSEL# with medium timing, these two bits are always set to 01.

Bits 8:0 Reserved. Read as 0's.

Register 08h Revision ID

Bits 7:0 01h **(Read Only)**

Register 0B-09h Class Code

Bits 23:0 060100h (Read Only)

Register 0Eh Header Type

Bits 7:0 80h (Read Only)

Register 40h BIOS Control Register

Bit 7 Reserved. Read as a 0.

Bit 6 Reserved. Read as a 0.

Bit 5 Enable/Disable Delayed Transaction

0: disable

1: enable

The default value is 0 (disabled).

Bit 4 PCI Posted Write Buffer Enable

The default value is 0 (disabled).

Bits [3:0] determine how the 5571 responds to F segment, E segment, and extended segment (FFF80000-FFFDFFFF) accesses. 5571 will positively respond to extended segment access when bit 0 is set. Bit 1, combining with bits [3:2], enables 5571 to respond to E segment access.

Bit 3 Positive Decode of Upper 64K BYTE BIOS Enable.

Bit 2 BIOS Subtractive Decode Enable.

Bits [3:2]	F segment		E segment		Comment
	+	-	+	-	
00			√ *		5571 positively responds to E segment access.
01		√			5571 subtractively responds to F segment access.
10	√		√ *		5571 positively responds to E and F segment access.
11	√				5571 positively responds to F segment access.

*: enabled if bit 1 is set.

Bit 1 Lower BIOS Enable.

Bit 0 Extended BIOS Enable. (FFF80000~FFFDFFFF)

Register 41h INTA# Remapping Control Register

Bit 7 Remapping Control

When enabled, INTA#, is remapped to the PC compatible interrupt signal specified in IRQ remapping table. This bit is set to 1 after reset.

0: Enable

1: Disable

Bits 6:4 Reserved. Read as 0's.

Bits 3:0 IRQx Remapping table.

Bits	IRQx#	Bits	IRQx#	Bits	IRQx#	Bits	IRQx#
0000	reserved	0101	IRQ5	1010	IRQ10	1111	IRQ15
0001	reserved	0110	IRQ6	1011	IRQ11		
0010	reserved	0111	IRQ7	1100	IRQ12		
0011	IRQ3	1000	reserved	1101	reserved		
0100	IRQ4	1001	IRQ9	1110	IRQ14		

Register 42h INTB# Remapping Control Register

Bit 7 Remapping Control

Bits 6:4 Reserved. Read as 0's.

Bits 3:0 IRQ Remapping table.

Register 43h INTC# Remapping Control Register

Bit 7 Remapping Control

Bits 6:4 **Reserved. Read as 0's.**

Bits 3:0 **IRQ Remapping table.**

Register 44h INTD# Remapping Control Register

Bit 7 **Remapping Control**

Bits 6:4 **Reserved. Read as 0's.**

Bits 3:0 **IRQ Remapping table.**

NOTE: The difference INT[A:D]# can be remapped to the same IRQ signal, but this IRQ signal should be set to level sensitive.

Register 45h

Bits 7:6 **ISA Bus Clock Selection**

00: 7.159MHz

01: PCICLK/4

10: PCICLK/3

Bit 5 **Flash EPROM Control bit 0**

Bit 4 **Reserved**

Bit 3 **Access Upper 128 Bytes CMOS SRAM**

0: Disable

1: Enable

Bit 2 **Flash EPROM Control Bit 1**

Previous implementation on flash EPROM support limits that EPROM is flashed upon power on till bit 5 is set to 1. The new added feature will allow EPROM to be flashed anytime. Bit 2 is added and the setting of both bit 2 and bit 5 will now control the EPROM flash operation.

Bit 5	Bit 2	Operation
0	0	EPROM can be flashed
1	0	EPROM can't be flashed again
X	1	EPROM can be flashed whenever bit 5 is 0

Bit 1:0 **Reserved**

Register 46h

Bits 7:6 **16-Bit I/O Cycle Command Recovery Time**

00: 5 BUSCLK

01: 4 BUSCLK

10: 3 BUSCLK

11: 2 BUSCLK

Bits 5:4 **8-Bit I/O Cycle Command Recovery Time**

00: 8 BUSCLK

01: 5 BUSCLK

10: 4 BUSCLK

11: 3 BUSCLK

Bit 3 **ROM Cycle Wait State Selection**

0: 4 wait states

1: 1 wait state

Bits 2:0 **Reserved**

Register 47h DMA Clock and Wait State Control Register

Bits 7:6 **Reserved**

Bits 5:4 **16-Bit DMA Cycle Wait State**

00 : 1 BUSCLK

01 : 2 BUSCLK

10 : 3 BUSCLK

11 : 4 BUSCLK

Bits 3:2 **8-Bit DMA Cycle Wait State**

00 : 1 BUSCLK

01 : 2 BUSCLK

10 : 3 BUSCLK

11 : 4 BUSCLK

Bit 1 **Extended DMAMEMR# Function**

0: Assertion of DMAMEMR# is delayed by one clock cycle later than XIOR#

1: Assertion of DMAMEMR# is at the same time as XIOR#.

Bit 0 **Reserved**

This bit must be written as 1

Register 48h ISA Master/DMA Memory Cycle Control Register 1

The ISA master or DMA memory access cycles will be forwarded to PCI bus when the address fall within the programmable region defined by bits[7:4]. The base address of the programmable region is 1Mbyte, and the top addresses is programmed in 1MByte increments from 1MByte to 16MByte. All memory cycles will be forwarded to PCI bus besides the cycle fall within memory hole defined in register 4Ah and 4Bh.

Bits 7:4

Bit 7	Bit 6	Bit 5	Bit 4	Top of Memory
0	0	0	0	1 MByte
0	0	0	1	2 MByte
0	0	1	0	3 MByte
0	0	1	1	4 MByte
0	1	0	0	5 MByte
0	1	0	1	6 MByte
0	1	1	0	7 MByte
0	1	1	1	8 MByte
1	0	0	0	9 MByte

1	0	0	1	10 MByte
1	0	1	0	11 MByte
1	0	1	1	12 MByte
1	1	0	0	13 MByte
1	1	0	1	14 MByte
1	1	1	0	15 MByte
1	1	1	1	16 MByte

ISA master and DMA memory cycles to the following memory regions will be forwarded to PCI bus if they are enabled.

Bit 3 **E0000h-EFFFFh Memory Region**

0: Disable

1: Enable, the cycle is forwarded to PCI bus.

Bit 2 **A0000h-BFFFFh memory Region**

0: Disable

1: Enable, the cycle is forwarded to PCI bus.

Bit 1 **80000h-9FFFFh Memory Region**

0: Disable

1: Enable

The cycle is forwarded to PCI bus.

Bit 0 **00000h-7FFFFh Memory Region**

0: Disable

1: Enable

The cycle is forwarded to PCI bus.

Register 49h ISA Master/DMA Memory Cycle Control Register 2

ISA master and DMA memory cycles to the following memory regions will be forwarded to PCI bus if they are enabled.

Bit 7 **DC000h-DFFFFh Memory region**

0: Disable

1: Enable

Bit 6 **D8000h-DBFFFh Memory Region**

0: Disable

1: Enable

Bit 5 **D4000h-D7FFFh Memory Region**

0: Disable

1: Enable

Bit 4 **D0000h-D3FFFh Memory Region**

0: Disable

1: Enable

Bit 3 **CC000h-CFFFFh Memory Region**

0: Disable

1: Enable

Bit 2 **C8000h-CBFFFh Memory Region**

0: Disable

1: Enable

Bit 1 **C4000h-C7FFFh Memory Region**

0: Disable

1: Enable

Bit 0 **C0000h-C3FFFh Memory Region**

0: Disable

1: Enable

Register 4Ah ISA Master/DMA Memory Cycle Control Register 3

Register 4Ah and register 4Bh are used to define the ISA address hole. The ISA address hole is located between 1Mbyte and 16MByte, and sized in 64KByte increments. ISA master and DMA memory cycles fall within this hole will not be forwarded to PCI bus. Register 4Ah and 4Bh are used to define the bottom and top address of the hole respectively. The hole is located between top and bottom address, and the bottom and top address must be at or above 1MByte. If bottom address is greater than top address, the ISA address hole is disabled.

Bits 7:0 **A23~A16**

Register 4Bh ISA Master/DMA Memory Cycle Control Register 4

This register is used to define the top address of the ISA Address hole.

Bits 7:0 **A23~A16**

Registers 4Ch-4Fh

Bits 7:0 **ICW1 to ICW4 of the built-in interrupt controller (master) can be read from 4Ch to 4Fh.**

Registers 50h-53h

Bits 7:0 **ICW1 to ICW4 of the built-in interrupt controller (slave) can be read from 50h to 53h.**

Registers 54h-55h

Bits 7:0 **OCW2 to OCW3 of the built-in interrupt controller (master) can be read from 54h to 55h.**

Registers 56h-57h

Bits 7:0 **OCW2 to OCW3 of the built-in interrupt controller (slave) can be read from 56h to 57h.**

Register 58h

Bits 7:0 **Low byte of the initial count number of Counter 0 in the built-in CTC can be read from 58h.**

Register 59h

Bits 7:0 **High byte of the initial count number of Counter 0 in the built-in CTC can be read from 59h.**

Register 5Ah

Bits 7:0 **Low byte of the initial count number of Counter 1 in the built-in CTC can be read from 5Ah.**

Register 5Bh

Bits 7:0 **High byte of the initial count number of Counter 1 in the built-in CTC can be read from 5Bh.**

Register 5Ch

Bits 7:0 Low byte of the initial count number of Counter 2 in the built-in CTC can be read from 5Ch.

Register 5Dh

Bits 7:0 High byte of the initial count number of Counter 2 in the built-in CTC can be read from 5Dh.

Register 5Eh

Bits 7:0 Control word (43h) of the built-in CTC can be read from 5Eh.

Register 5Fh

Bits 7:6 Reserved
Bit 5 CTC write count pointer status for counter 2
Bit 4 CTC write count pointer status for counter 1
Bit 3 CTC write count pointer status for counter 0
Bit 2 CTC read count pointer status for counter 2
Bit 1 CTC read count pointer status for counter 1
Bit 0 CTC read count pointer status for counter 0
0: LSB
1: MSB

Register 60h

Bits 7:0 The same value as ISA port 70h.

Register 61h MIRQ Remapping Control Register

This register controls the remapping of MIRQ to the PC/AT compatible IRQ inputs of the interrupt controller. MIRQ can be remapped to any one of the 11 interrupts.

Bit 7 MIRQ Remapping Control

When enabled, MIRQ is remapped to the PC compatible interrupt signal specified in IRQ remapping table.
0: Enable
1: Disable

Bit 6 MIRQ/IRQx Sharing Control

0: Enable
1: Disable
The interrupt specified by IRQ remapping table is masked when this bit is disabled and MIRQ remapping is enabled.
When sharing and remapping are both enalbed, MIRQ will be remapped to the IRQ channel programmed via Register 60h.

While MIRQ is enalbed, the interrupt channel for ISA will automatically be masked. MIRQ, and INTA#, INTB#, INTC#, INTD# may be asserted at the same time.

Bits 5:4 Reserved. Read as zero.

Bits 3:0 Interrupt Remapping Table

This field is used to define the MIRQ remapping to one of the eleven PC compatible interrupts.

bits [3:0]	IRQ remapped	bits [3:0]	IRQ remapped
0000	Reserved	1000	Reserved
0001	Reserved	1001	IRQ9
0010	Reserved	1010	IRQ10
0011	IRQ3	1011	IRQ11
0100	IRQ4	1100	IRQ12
0101	IRQ5	1101	Reserved
0110	IRQ6	1110	IRQ14
0111	IRQ7	1111	IRQ15

Operation Rules for Rerouting Circuits:

1. If any one IDE channel is in compatibility mode, the IRQ channel mapped to that IDE channel should be assigned as the IDE IRQ channel. Nobody can share it.

   e.g.: IDE channel 0 is in compatibility mode, while channel 1 is native.

   IRQ 14 should be always used by IDE channel 0. Nobody can share it. IDE channel 1 should use DIRQ to reroute it's interrupt requests.

2. If channel n is rerouted by MIRQ: (Edge & Level trigger can be both applied)

   CASE 1: Share disable:

   Except for MIRQ, nobody can share the channel.

   MIRQ can't be rerouted to the same channel.

   CASE 2: Share enable:

   Including MIRQ, INTA#, INTB#, INTC#, INTD#, and DIRQ may be rerouted to the same channel.

   Here, ISA IRQn will be automatically masked.

3. If MIRQ is disabled:

   PCI INTA#, INTB#, INTC#, and INTD# can be rerouted to the same channel. But ISA IRQn will be automatically masked.

4. None of MIRQ, PCI interrupt pins, DIRQ are rerouted to channel n:

ISA IRQn can be enabled.

Register 62h - On-board Device DMA Control Register

This register is used to control the remapping of MDRQ~~0~~ and MDACK~~0~~# to the DREQ and DACK# signals of the 8237 DMA controller.

Bits 7:4 **Reserved**

Bit 3 **MDRQ~~0~~/MDAK~~0~~# Remapping Control**

0: Disable

1: Enable

When this bit set to 1, the MDRQ~~0~~/MDACK~~0~~# are mapped to the compatible ISA channel specified in bits[~~6~~2:~~4~~0]. When this bit set to 0, the ISA DREQ/DACK# pair is used for that channel.

Bits 2:0 **DMA Channel Remapping Table of MDRQ~~0~~/MDACK~~0~~#**

The following table is used to select the DMA channel for MDRQ~~0~~/MDACK~~0~~#

Bits[2:0]	DMA Channel
000	Channel 0
001	Channel 1
010	Channel 2
011	Channel 3
100	Disable
101	Channel 5
110	Channel 6
111	Channel 7

Register 63h - IDEIRQ Remapping Control Register

Bit 7 **IDEIRQ Remapping Control**

1: Disable

0: Enable

Bit 6:4 **Reserved. Read as zero.**

Bits 3:0 **Interrupt Remapping Table**

Bits [3:0]	remapped IRQ	Bits [3:0]	remapped IRQ
0000	Reserved	1000	Reserved
0001	Reserved	1001	IRQ9
0010	Reserved	1010	IRQ10
0011	IRQ3	1011	IRQ11
0100	IRQ4	1100	IRQ12
0101	IRQ5	1101	Reserved
0110	IRQ6	1110	IRQ14
0111	IRQ7	1111	IRQ15

Register 64h - GPIO~~GPIO0~~ Control Register

Bit 7 **GPIO~~GPIO0~~ Mode Control**
0: Output mode
1: Input mode (default)

Bit 6 **GPIO~~GPIO0~~ Input Active Level Control**
0: Active low
1: Active high

Bit 5 **GPIO~~GPIO0~~ Input Bounce-Free Control**
0: Disable
1: Enable
When this bit set to 1,the GPIO~~GPIO0~~ input goes through a de-bounce circuit.

Bit 4 **Reserved. Read as zero.**

Bits 3:0 **De-bounce Count for GPIO~~GPIO0~~ De-Bounce Circuit.**
The minimum value is 2. The timer-expire interval is calculated by the following equation: The timer-expire interval=(Count-1)x0.6s

Register 65h

Bits 7:5 **Reserved.**
These bits should be programmed to all 0s.

Bit 4 **Hot Key Status**
This bit is set when hot key is pressed and should be cleared at the end of SMI handler. This bit is meaningful only when internal KBC is used.

Bit 3: **Enable Hot Key**
0: Disable
1: Enable

Bit 2 **Reserved**

Bit 1 **SMOUT**
When register 66h bit [1:0] set to '10', programming a '1' to this bit then pin GPIO~~GPIO0~~ will drive high; programming a '0' to this bit then pin GPIO~~GPIO0~~ will drive low.

Bit 0 **GPIO~~GPIO0~~ Status**
This bit is set when GPIO~~GPIO0~~ is active and should be cleared at the end of SMI handler. This bit is meaningful only when register 64h bit 7 is set to 1.

Registers 66h,67h - GPIO~~GPIO0~~ Output Mode Control Register

A 16-bit I/O space base address defined in bit[15:2] is used to cause GPIO~~GPIO0~~ to assert "active low" signal for subtractively decoded I/O cycles generated by PCI masters that fall in the range specified by this register. This register is available only when GPIO~~GPIO0~~ is set to output mode.

Bits 15:2 **A[15:2] of GPIO~~GPIO0~~ I/O Space Base Address**

Bits 1:0 **GPIO~~GPIO0~~ I/O Space Address Mask**

00: Mask A1, A0
01: Mask A2, A1, A0
10: Enable SMOUT function
11: Mask A3, A2, A1, A0

Register 68h - USBIRQ Remapping Control Register

Bit 7 **USBIRQ Remapping Control**
0: Enable
1: Disable
~~0: Enable~~

Bit 6~~:4~~ ~~**Reserved. Read as zero.**~~**Built-in USB disable/enable**
0: Disable
1: Enable

Bit 5:4 **Reserved. Read as zero.**

Bits 3:0 **Interrupt Remapping Table**

Bits [3:0]	remapped IRQ	Bits [3:0]	remapped IRQ
0000	Reserved	1000	Reserved
0001	Reserved	1001	IRQ9
0010	Reserved	1010	IRQ10
0011	IRQ3	1011	IRQ11
0100	IRQ4	1100	IRQ12
0101	IRQ5	1101	Reserved
0110	IRQ6	1110	IRQ14
0111	IRQ7	1111	IRQ15

Register 69

Bit 7 **Automatic Power Up System On Sat**
0: Disable
1: Enable
Before enabling this function, register 6A bit 6 and register 69 bit 0 should be enabled and RTC Alarm should be programmed.

Bit 6 **Automatic Power Up System On Fri**
0: Disable
1: Enable
Before enabling this function, register 6A bit 6 and register 69 bit 0 should be enabled and RTC Alarm should be programmed.

Bit 5 **Automatic Power Up System On Thu**
0: Disable
1: Enable

Before enabling this function, register 6A bit 6 and register 69 bit 0 should be enabled and RTC Alarm should be programmed.

Bit 4 —Automatic Power Up System On Wed

0: Disable

1: Enable

Before enabling this function, register 6A bit 6 and register 69 bit 0 should be enabled and RTC Alarm should be programmed.

Bbit 3 —Automatic Power Up System On Tue

0: Disable

1: Enable

Before enabling this function, register 6A bit 6 and register 69 bit 0 should be enabled and RTC Alarm should be programmed.

bit 2 —Automatic Power Up System On Mon

0: Disable

1: Enable

Before enabling this function, register 6A bit 6 and register 69 bit 0 should be enabled and RTC Alarm should be programmed.

Bit 1 —Automatic Power Up System On Sun

0: Disable

1: Enable

Before enabling this function, register 6A bit 6 and register 69 bit 0 should be enabled and RTC Alarm should be programmed.

Bit 0 —Automatic Power Up System Control

0: Disable

1: Enable

Before enabling this function, register 6A bit 6 should be enabled.

Register 6A

Bit 7 —Power Off System Control

Before enabling this function, register 6A bit 6 should be enabled. Once writing a '1' to this bit, system will be power off.

Bit 6 —Power Control Function

0: Disable

1: Enable

When enabling this bit, functions of automatic power up system, power off system and a ring leads to power up system may work.

Bit 5— A Ring# Leads To Power Up System Control

0 : Disable

1 : Enable

Before enabling this function, register 6A bit 6 should be enabled.

Bit 4 —Ring# Input Active Level Control

0: Active high

1: Active low

Bit 3 **ECCEN**

Bit 2 **RINGDIS**

ECCEN	RINGDIS	MDRQ/RING#/~~PD7~~
1	1	RING#
1	0	MDRQ
0	1	Reserve~~PD7~~
0	0	Reserved

Bits 1:0 **Reserved. These bits should be programmed to 0s.**

Register 6Bh

Bits 7:0 **Reserved. These bits should be programmed to all 0s.**

Register 6Ch

Bits 7:2 **Reserved. These bits should be programmed to all 0s.**

Bit 1 **Enable/Disable The Reading Of All Base Registers In DMA Controller.**

0: Disable.

1: Enable.

Bit 0 **Reserved.**

This bit should be programmed to 0.

Register 6Dh

Bits 7:0 **Reserved.**

Register 6Eh Software-Controlled Interrupt Request, Channels 7-0

Bit 7 **Interrupt Channel 7**

Bit 6 **Interrupt Channel 6**

Bit 5 **Interrupt Channel 5**

Bit 4 **Interrupt Channel 4**

Bit 3 **Interrupt Channel 3**

Bit 2 **Interrupt Channel 2**

Bit 1 **Interrupt Channel 1**

Bit 0 **Interrupt Channel 0**

Writing a 1 to these bits will cause the corresponding interrupt requests to be outstanding. This register defaults to all 0s.

Register 6Fh Software-Controlled Interrupt Request, channels 15-8

Bit 7 **Interrupt Channel 15**

Bit 6 **Interrupt Channel 14**

Bit 5 **Interrupt Channel 13**

Bit 4 **Interrupt Channel 12**

Bit 3 **Interrupt Channel 11**

Bit 2 **Interrupt Channel 10**

Bit 1 **Interrupt Channel 9**

Bit 0 **Interrupt Channel 8**

Writing a 1 to these bits will cause the corresponding interrupt requests to be outstanding.

Register 70h

Bit 7 **Enable/Disable the prefetch/postwrite of the ISA master and DMA controller**

0: Disable.

1: Enable.

Bit 6 **Enable/Disable IOR# and MEMR# cycles extended by 1/2 BCLK**

0: Disable

1: Enable.

Bit 5 **Reserved. This bit should be programmed to 0**

Bit 4 **Enable/Disable keyboard lock**

0: Disable.

1: Enable.

When this bit is set to 0, the keyboard lock is disabled and pin ~~10~~AH26 can be used as ~~GPIO0~~MDACK#. When this bit is set to 1, pin ~~10~~AH26 is used as the keyboard lock.

Bit 3 **Hardware trap status for keyboard controller**

0: the external keyboard controller is used.

1: the internal keyboard controller is used.

Bit 2 **Software disable PS/2 mode of the keyboard controller**

0: no effect.

1: Force the keyboard controller to disable the PS/2 mode regardless of the result of the hardware trap, ie. IRQ12 is available.

This bit is used to disable the PS/2 mode when the hardware trap enables the PS/2 mode.

Bit 1 **Built-in RTC Status (Read Only)**

0: ~~Not~~ Uused

1: Not u~~U~~sed

When built-in RTC is used, this bit is set to 1.

Bit 0 Reserved. This bit should be programmed to 0.

Register 71h - Type-F DMA Control Register

This register is used to set which DMA channel can perform type-F DMA transfers. A 1 on any bit sets the corresponding DMA channel to perform type-F DMA transfers.

Bit 7 **DMA Channel 7**

Bit 6 **DMA Channel 6**

Bit 5 **DMA Channel 5**

Bit 4 **Reserved**

Bit 3 **DMA Channel 3**

Bit 2 **DMA Channel 2**

Bit 1 **DMA Channel 1**

Bit 0 **DMA Channel 0**

Register 72h,73h SMI Triggered By IRQ/GPIO~~GPIO0~~ Control

Bits 15:3 **Corresponds To The Mask Bits Of IRQ 15-3**

Bit 2 **Corresponds To The Mask Bit Of GPIO~~GPIO0~~**

Bit 1 **Corresponds To The Mask Bit Of IRQ1**

Bit 0 **Reserved**

When disabled, any event from the corresponding IRQ/GPIO~~GPIO0~~ will cause the system to generate SMI. This register is only meaningful when the memory/PCI configuration register 95h, bit 7 is enabled.

0: Disable (default)

1: Enable

Register 74h, 75h System Standby Timer Reload, System Standby State Exit And Throttling State Exit Control

Bits 15:3, 1 **Corresponds To The Mask Bits Of IRQ 15-3,1**

Bit 2 **Corresponds To The Mask Bit Of GPIO~~GPIO0~~**

Bit 0 **Corresponds To The Mask Bit Of NMI**

When disabled, any event from the corresponding IRQ, GPIO~~GPIO0~~ and NMI will cause the system to exit the system standby state, exit the throttling state and reload the system standby timer.

0: Disable (default)

1: Enable

Register 76h,77h Monitor Standby Timer Reload And Monitor Standby State Exit Control

Bits 15:1 **Corresponds To The Mask Bits of IRQ 15-1**

Bit 0 **Corresponds To The Mask Bit of NMI**

When disabled, any event from the corresponding IRQ/NMI will cause the system to exit the monitor standby state and reload the monitor standby timer.

0: Disable (default)

1: Enable

6.3 Non-Configuration Registers

DMA Registers

These registers can be accessed from PCI bus.

Address	Attribute	Register Name
0000h	R/W	DMA1 CH0 Base and Current Address Register
0001h	R/W	DMA1 CH0 Base and Current Count Register
0002h	R/W	DMA1 CH1 Base and Current Address Register
0003h	R/W	DMA1 CH1 Base and Current Count Register
0004h	R/W	DMA1 CH2 Base and Current Address Register
0005h	R/W	DMA1 CH2 Base and Current Count Register
0006h	R/W	DMA1 CH3 Base and Current Address Register
0007h	R/W	DMA1 CH3 Base and Current Count Register
0008h	R/W	DMA1 Status(r) Command(w) Register
0009h	WO	DMA1 Request Register
000Ah	WO	DMA1 Write Single Mask Bit
000Bh	WO	DMA1 Mode Register
000Ch	WO	DMA1 Clear Byte Pointer
000Dh	WO	DMA1 Master Clear
000Eh	WO	DMA1 Clear Mask Register
000Fh	R/W	DMA1 Write All Mask Bits(w) Mask Status Register(r)
00C0h	R/W	DMA2 CH0 Base and Current Address Register
00C2h	R/W	DMA2 CH0 Base and Current Count Register
00C4h	R/W	DMA2 CH1 Base and Current Address Register
00C6h	R/W	DMA2 CH1 Base and Current Count Register
00C8h	R/W	DMA2 CH2 Base and Current Address Register
00CAh	R/W	DMA2 CH2 Base and Current Count Register
00CCh	R/W	DMA2 CH3 Base and Current Address Register
00CEh	R/W	DMA2 CH3 Base and Current Count Register
00D0h	R/W	DMA2 Status(r) Command(w) Register
00D2h	WO	DMA2 Request Register
00D4h	WO	DMA2 Write Single Mask Bit Register
00D6h	WO	DMA2 Mode Register
00D8h	WO	DMA2 Clear Byte Pointer
00DAh	WO	DMA2 Master Clear
00DCh	WO	DMA2 Clear Mask Register
00DEh	R/W	DMA2 Write All Mask Bits(w) Mask Status Register(r)

These registers can be accessed from PCI bus or ISA bus.

Address	Attribute	Register Name
0080h	R/W	Reserved
0081h	R/W	DMA Channel 2 Low Page Register
0082h	R/W	DMA Channel 3 Low Page Register
0083h	R/W	DMA Channel 1 Low Page Register
0084h	R/W	Reserved

0085h	R/W	Reserved
0086h	R/W	Reserved
0087h	R/W	DMA Channel 0 Low Page Register
0088h	R/W	Reserved
0089h	R/W	DMA Channel 6 Low Page Register
008Ah	R/W	DMA Channel 7 Low Page Register
008Bh	R/W	DMA Channel 5 Low Page Register
008Ch	R/W	Reserved
008Dh	R/W	Reserved
008Eh	R/W	Reserved
008Fh	R/W	Refresh Low Page Register

Interrupt Controller Registers (These registers can be accessed from PCI bus or ISA bus.)

Address	Attribute	Register Name
0020h	R/W	INT 1 Base Address Register
0021h	R/W	INT 1 Mask Register
00A0h	R/W	INT 2 Base Address Register
00A1h	R/W	INT 2 Mask Register

Timer Registers (These registers can be accessed from PCI bus or ISA bus.)

Address	Attribute	Register Name
0040h	R/W	Interval Timer 1 - Counter 0
0041h	R/W	Interval Timer 1 - Counter 1
0042h	R/W	Interval Timer 1 - Counter 2
0043h	WO	Interval Timer 1 - Control Word Register

Other Registers (These registers can be accessed from PCI bus or ISA bus.)

Address	Attribute	Register Name
0061h	R/W	NMI Status Register
0070h	WO	CMOS RAM Address and NMI Mask Register
00F0h	WO	Coprocessor Error Register

Register 4D0h IRQ Edge/Level Control Register 1

Bit 7 **IRQ7**
0: Edge sensitive
1: Level sensitive

Bit 6 **IRQ6**
0: Edge sensitive
1: Level sensitive

Bit 5 **IRQ5**
0: Edge sensitive
1: Level sensitive

Bit 4 **IRQ4**
0: Edge sensitive
1: Level sensitive

Bit 3 **IRQ3**
0: Edge sensitive
1: Level sensitive

Bit 2 **IRQ2**
This bit must be set to 0. Read as 0.

Bit 1 **IRQ1**
This bit must be set to 0. Read as 0.

Bit 0 **IRQ0**
This bit must be set to 0. Read as 0.
After reset this register is set to 00h.

Register 4D1h IRQ Edge/Level Control Register 2

Bit 7 **IRQ15**
0: Edge sensitive
1: Level sensitive

Bit 6 **IRQ14**
0: Edge sensitive
1: Level sensitive

Bit 5 **IRQ13**
This bit must be set to 0. Read as 0.

Bit 4 **IRQ12**
0: Edge sensitive
1: Level sensitive

Bit 3 **IRQ11**
0: Edge sensitive
1: Level sensitive

Bit 2 **IRQ10**
0: Edge sensitive
1: Level sensitive

Bit 1 **IRQ9**
0: Edge sensitive
1: Level sensitive

Bit 0 **IRQ8**
This bit must be set to 0. Read as zero.
After reset this register is set to 00h.

6.4 USB Configuration Registers

Register 00h Vendor ID - Low Byte

Bits 7:0 39h

Register 01h Vendor ID - High Byte

Bits 7:0 10h

Register 02h Device ID - Low Byte

Bits 7:0 01h

Register 03h Device ID - High Byte

Bits 7:0 70h

Register 04h Command - Low Byte

Bit 7 **Wait Cycle Control**
0: always disabled; not supported.

Bit 6 **Parity Error Response**
1: enable
0: disable

Bit 5 **VGA Palette Snoop**
0: always disabled; not supported.

Bit 4 **Memory Write And Invalidate Enable**
0: always disabled; not supported.

Bit 3 **Special Cycle**
0: always disabled; not supported

Bit 2 **Bus Master**
1: Enable
0: Disable

Bit 1 **Memory Space**
1: Enable
0: Disable

Bit 0 **IO Space**
1: Enable
0: Disable

Register 05h Command - High Byte

Bits 7:2 **Reserved**

Bit 1 **Fast Back To Back**
0: always disabled; not supported.

Bit 0 **Serr# Enable**
1: Enable
0: Disable

Register 06h Status - Low Byte

Bit 7 **Fast Back To Back Capable**
0: Always disabled; not supported.

Bit 6 **UDF Support**
0: always disabled; not supported.

Bit 5 **66 Mhz Capable**
0 : always disabled; not supported.

Bits 4:0 **Reserved**

Register 07h Status - High Byte

Bit 7 **Detected Parity Error**
This bit is set when parity error is detected.
This bit is cleared by writing a 1 to it.

Bit 6 **Signaled System Error(SERR#)**

This bit is set when SERR# is asserted.
This bit is cleared by writing a 1 to it.

Bit 5 **Received Master Abort**
This bit is set when a master cycle is terminated by master abort.
This bit is cleared by writing a 1 to it.

Bit 4 **Received Target Abort**
This bit is set when a master cycle is terminated by target abort.
This bit is cleared by writing a 1 to it.

Bit 3 **Signaled Target Abort**
This bit is set when a target cycle is terminated by target abort.
This bit is cleared by writing a 1 to it.
0: always disabled; not supported.

Bits 2:1 **Devsel Timing**
01: Medium

Bit 0 **Data Parity Error Detected**
This bit is set when (1) PERR# is asserted.
(2) Acting as bus master.
(3) Parity error response bit is set.
This bit is cleared by writing a 1 to it.

Register 08h Revision ID

Bits 7:0 B0h

Register 0B-09h Class Code

Bits 23:0 0C0310h

Register 0Dh Latency Timer

Bits 7:0 May Be Programmed

Register 0Eh Header Type

Bits 7:0 10h : Multiple Function Device

Register 13-10h Memory Space Base Address Register

Bits 31:12 May Be Programmed
Bits 11:0 000h

Registers 17-14 IO Space Base Address Register

Bits 31:3 May Be Programmed
Bits 2:0 001b

Register 3Ch Interrupt Line

Bit 7:0 May Be Programmed

Register 3Dh Interrupt Pin

Bit 7:0 01h

Register 43Eh ~~USB Host Controller Specific~~Minimum Grant Register

Always 00h

Read Only

Register 3Fh Maximum Latency Register

Always 00h

Read Only

~~**Bit 7 0 Wait State**~~
~~1: master cycle will be 0 wait state.~~
~~0: master cycle will be 1 wait state.~~
~~**Bit 6 Enable Root Hub Port (Reset Value: 1)**~~
~~1: Enable~~
~~0: Disable~~
~~**Bit 5 Enable Root Hub Port A (Reset Value: 1)**~~
~~1: Enable~~
~~0: Disable~~
~~**Bit 4 Enable Root Hub Port B (Reset Value: 1)**~~
~~1: Enable~~
~~0: Disable~~
~~**Bit 3 Test Mode For Frame Number Counter & Transfer Size Counter**~~
~~1: Enable~~
~~0: Disable~~
~~**Bit 2:0 Reserved**~~

6.216.5 PCI IDE Configuration Registers

Register 00, 01h - Vendor ID

Bits 15:0 1039h(Read Only)

Register 02, 03h - Device ID

Bits 15:0 557~~1~~13h~~(Read Only)~~

Register 04h - Command low byte

Bits 7:3 These bits are hardwired to 0.

Bit 2 **Bus Master Enable**

When set, the Bus master function is enabled. It is disabled by default.

Bit 1 **Memory Space Enable**

This bit is disabled by default. Read only.

Bit 0 **I/O Space Enable**

When enabled, the built-in IDE will respond to any access of the IDE legacy ports in the compatibilty mode, or to any access of the IDE relocatable ports in the native mode. Also, any access to the PCI bus master IDE registers are allowed. This bit is zero(disabled) on reset.

Register 05h - Command high byte

Bits 7:0 00h(Read Only)

Register 06h - Status low byte

Bits 7:6 These bits are hardwired to zero.

Bit 5 **This is a reserved bit, and is recommend to program 0.**

Bits 4:0 **These bits are hardwired to zero.**

Register 07h - Status high byte

Bits 7:6 **These bits are hardwired to zero.**

Bit 5 **Master Abort Asserted**

This bit is set when a PCI bus master IDE transaction is terminated by master abort. While this bit is set, IDE will issue an interrupt request. This bit can be cleared by writing a 1 to it.

Bit 4 **Received Target Abort**

The bit is set whenever PCI bus master IDE transaction is terminated with target abort.

Bit 3 **Signaled Target Abort.**

The bit will be asserted when IDE terminates a transaction with target abort.

Bits 2:1 **DEVSEL# Timing DEVT.**

These two bits define the timing of asserting DEVSEL#. The built-in IDE always asserts DEVSEL# in fast timing, and thus the two bits are hardwired to 0 per PCI Spec.

Bit 0 **Reserved, Read as "0".**

Register 08h - Revision Identification

Bits 7:0 **C0h(Read Only)**

Register 09h - Programming Interface Byte

Bit 7 **Master IDE Device**

This bit is hardwird to one to indicate that the built-in IDE is capable of supporting bus master function.

Bit 6 **IDE Channel Status Reporting Bit**

While the bit is enabled, bits 5 and 4 can be queried to determine the status of IDE controller. (The default value is '1', which means enabled.)

Bit 5 ~~**IDE Primary Channel Enable Bit**~~**Reserved**

~~This bit can be read or written. BIOS and OS code can change this bit as follows:~~

~~If a '1' is written and read back, then the device has been enabled.~~

~~If a '1' is written and a '0' is read back, then the device stays disabled.~~

~~If a '0' is written and read back, then the device has been disabled.~~

~~If a '0' is written abd a '1' is read back, then the device stays enabled.~~

~~The default value of the bit is '1', which means enabled.~~

Bit 4 ~~**IDE Secondary Channel Enable Bit**~~**Reserved**

~~This bit can be read or written. BIOS and OS code can change this bit as follows:~~

~~If a '1' is written and read back, then the device has been enabled.~~

~~If a '1' is written and a '0' is read back, then the device stays disabled.~~

~~If a '0' is written and read back, then the device has been disabled.~~

~~If a '0' is written abd a '1' is read back, then the device stays enabled.~~

~~The default value of the bit is '1', which means enabled.~~

Bit 3 **Secondary IDE Programmable Indicator**

When the bit is programmed as '1', it means that the primary channel can be programmed to operate in compatible or native mode. When the bit is programmed as '0', the mode is fixed and is determined by the value of bit 2. This bit should be programmed as '1' during the BIOS boot up procedures.

Bit 2 **Secondary IDE Operating Mode**

This bit defines the mode that the secondary IDE channel is operating in. Zero corrsponds to 'compatibility' while one means native PCI mode. By default, the bit is 0 and is programmable.

Bit 1 **Primary IDE Programmable Indicator**

When the bit is programmed as '1', it means that the primary channel can be programmed to operate in compatible or native mode. When the bit is programmed as '0', the mode is fixed and is determined by the value of bit 0. This bit should be programmed as '1' during the BIOS boot up procedures.

Bit 0 **Primary IDE Operating Mode**

This bit defines the mode that the primary IDE channel is operating in. Zero corrsponds to 'compatibility' whie one means native PCI mode. The powerup state for this bit is 0, and can be set if native mode is expected.

Register 0Ah - Subclass ID

Bits 7:0 01h

Register 0Bh - Class ID

Bits 7:0 01h

Register 0Ch - Cache Line Size

Bits 7:0 00h

Register 0Dh- Latency Timer

Bits 7:0 Programmable (from 0 to 255). The default value is 0.

Register 0Eh - Header Type

Bits 7:0 80h

Register 0Fh - BIST

Bits 7:0 00h

Register 10, 11, 12, 13h Primary Channel Base Address Register

Register 14, 15, 16, 17h Primary Channel Base Address Register

Register 18, 19, 1A, 1Bh Secondary Channel Base Address Register

Register 1C, 1D, 1E, 1Fh Secondary Channel Base Address Register

In the native mode, these four registers define the IDE base address for each of the two IDE devices in both the primary and secondary channels respectively. In the compatible mode, the four registers can still be programmed and read out, but it does not affect the IDE address decoding.

Register 20, 21, 22, 23h Bus Master IDE Control Register Base Address

Offset Register	Register Access
00h	Bus Master IDE Command Register (Primary)
01h	Reserved
02h	Bus Master IDE Status Register(Primary)
03h	Reserved
04-07h	Bus Master IDE PRD (*) Table Pointer (Primary)
08h	Bus Master IDE Command Register (Secondary)
09h	Reserved
0Ah	Bus Master IDE Status Register (Secondary)
0Bh	Reserved
0C-0Fh	Bus Master IDE PRD (*) Table Pointer (Secondary)

*PRD: Physical Region Descriptor

Register 24 to 2Bh These bits are hardwired to zero

Register 2C, 2Dh, 2E, 2Fh Reserved. Read as"0".

Register 30, 31, 32, 33h Expansion ROM Base Address

These four byte registers are recommended not to be programmed.

The following 10 registers define the speed of accessing IDE data and command registers. The four most significant bits of each Recovery Time Control byte are hardwired to zero, and the rest is R/W programmable with the following definition.

Recovery Time Control

Bits 3:0 Recovery Time

0000	12 PCICLK	0001	1 PCICLK
0010	2 PCICLK	0011	3 PCICLK
0100	4 PCICLK	0101	5 PCICLK
0110	6 PCICLK	0111	7 PCICLK
1000	8 PCICLK	1001	9 PCICLK
1010	10 PCICLK	1011	11 PCICLK
1100	13 PCICLK	1101	14 PCICLK
1110	15 PCICLK	1111	15 PCICLK

The five most significant bits of each Active Time Control byte are hardwired to zero, and the rest is R/W programmable with the following definition.

Active Time Control

Bits 2:0	**Active Time**
000	8 PCICLK
001	1 PCICLK
010	2 PCICLK
011	3 PCICLK
100	4 PCICLK
101	5 PCICLK
110	6 PCICLK
111	12 PCICLK

Register 40h IDE Primary Channel/Master Drive Data Recovery Time Control.

Register 41h IDE Primary Channel/Master Drive DataActive Time Control.

Register 42h IDE Primary Channel/Slave Drive Data Recovery Time Control.

Register 43h IDE Primary Channel/Slave Drive Data Active Time Control

Register 44h IDE Secondary Channel/Master Drive Data Recovery Time Control.

Register 45h IDE Secondary Channel/Master Drive Data Active Time Control

Register 46h IDE Secondary Channel/Slave Drive Data Recovery Time Control.

Register 47h IDE Secondary Channel/Slave Drive Data Active Time Control

Register 48h IDE Command Recovery Time Control

Register 49h IDE Command Active Time Control

Register 4Ah IDE General Control Register 0

Bit 7 **Enable\disable burst mode. (1: Enable; default value = 0)**

Bits 6~~:~~ 4 **Reserved. (Programmed as '0'.)**

Bit 5 **Postwrite cycle selection**

0: 6 PCICLK

1: 3 PCICLK

Bit 3 **Bus Master Speed Control**

~~When set as~~

0: PCI Request asserted while there are 20 bytes in FIFO.

1: PCI Request asserted while there are 16 bytes in FIFO.

~~The default value is '0'.~~

Bit 2 **IDE Secondary Channel Enable Bit**

This bit can be read or written. BIOS and OS code can change this bit as follows:

If a '1' is written and read back, then the device has been enabled.

If a '1' is written and a '0' is read back, then the device stays disabled.

If a '0' is written and read back, then the device has been disabled.

If a '0' is written abd a '1' is read back, then the device stays enabled.

The default value of the bit is '1', which means enabled.

Bit 1 **IDE Primary Channel Enable Bit**

This bit can be read or written. BIOS and OS code can change this bit as follows:

If a '1' is written and read back, then the device has been enabled.

If a '1' is written and a '0' is read back, then the device stays disabled.

If a '0' is written and read back, then the device has been disabled.

If a '0' is written abd a '1' is read back, then the device stays enabled.

The default value of the bit is '1', which means enabled.

~~**Bit 2 Enable Delay Transaction.**~~
~~0: Disabled. (default)~~
~~1: Enabled.~~

Bits ~~1:~~0 ~~Reserved. (Programmed as '0'.)~~Enable Delay Transaction
0: Disabled (default)
1: Enabled

Register 4Bh IDE General Control register 1

Bit 7 **Enable Postwrite of the Slave Drive in Secondary Channel.**
0: Disabled. (default)
1: Enabled.

Bit 6 **Enable Postwrite of the Master Drive in Secondary Channel.**
0: Disabled. (default)
1: Enabled.

Bit 5 **Enable Postwrite of the Slave Drive in Primary Channel.**
0: Disabled. (default)
1: Enabled.

Bit 4 **Enable Postwrite of the Master Drive in Primary Channel.**
0: Disabled. (default)
1: Enabled.

Bit 3 **Enable Prefetch of the Slave Drive in Secondary Channel.**
0: Disabled. (default)
1: Enabled.

Bit 2 **Enable Prefetch of the Master Drive in Secondary Channel.**
0: Disabled. (default)
1: Enabled.

Bit 1 **Enable Prefetch of the Slave Drive in Primary Channel.**
0: Disabled. (default)
1: Enabled.

Bit 1 **Enable Prefetch of the Master Drive in Primary Channel.**
0: Disabled. (default)
1: Enabled.

(Following two 16-bit wide registers define the prefetching length of each IDE channel respectively.)

Register 4Ch Prefetch Count of Primary Channel (Low Byte)

Register 4Dh Prefetch Count of Primary Channel (High Byte)

Register 4Eh Prefetch Count of Secondary Channel (Low Byte)

Register 4Fh Prefetch Count of Secondary Channel (High Byte)

~~6.21.1~~6.5.1 PCI Bus Master IDE Registers

The PCI Bus master IDE Registers use 16 bytes of I/O Space. These registers can be accessed through I/O R/W to the address defined in the Bus Master IDE register Base Address in the Configuration space. The definition of each register is described below.

Bus Master IDE Command Register

Bits 7:4 **Reserved. Return 0 on reads.**

Bit 3 **Read or Write Control.**

This bit defines the R/W control of the bus master transfer. When set to zero, PCI bus master reads are conducted. When set to one, PCI bus master writes are conducted.

Bits 2:1 **Reserved.**

Bit 0 **Start/Stop Bus Master**

The 5571 builtin IDE Controller enables its bus master operation whenever it detects this bit changing from a zero to a one. The operation can be halted by writing a zero to this bit.

Bus Master IDE Status Register

Bit 7 **Simplex Only**

This bit is hardwired to zero to indicate that only one bus master channel can be operated at a time.

Bit 6 **Drive 1 DMA Capable**

This R/W bit can be set by BIOS or driver to indicate that drvie 1 for this channel is capable of DMA transfers.

Bit 5 **Drive 0 DMA Capable**

This R/W bit can be set by BIOS or driver to indicate that drvie 0 for this channel is capable of DMA transfers.

Bits 4:3 **Reserved. Return 0 on reads**

Bit 2 **Interrupt**

The bit is set by the rising edge of the IDE interrupt line to indicate that all data transferred from the drive is visible in the system memory. Writing a '1' to this bit can reset it.

Bit 1 **Error**

This bit is set when the IDE controller encounters an error during data transferring to/from memory.

Bit 0 **Bus Master IDE Device Active**

This bit is set when the start bit in the command register is set. It can be cleared when the last transfer of a region is perfomred, or the start bit is reset.

PRD Table Pointer Register

This 32-bit register contains address pointing to the starting address of the PRD table.

Bits 31:2 **Base Address of the PRD Table**

Bits 1:0 Reserved

7. Pin Assignment and Description

7.1 Pin Assignment

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	
A	GND (OVSS)	MD58	MD55	MD52	MD49	MD45	MD41	MD37	MD33	MD29	MD25	MD21	MD17	MD12	MD8	MD4	TA7	TA2	ADSC#	HD0	HD4	HD8	HD13	HD17	HD21	HD24	HD26	HD27	HD28	A
B	MD61	GND (OVSS)	MD56	MD53	MD50	MD46	MD42	MD38	MD34	MD30	MD26	MD22	MD18	MD13	MD9	MD5	MD0	TA3	ADSV#	KOE#	HD3	HD7	HD12	HD16	HD20	HD23	HD25	HD29	HD30	B
C	MD62	MD63	MD57	MD54	MD51	MD47	MD43	MD39	MD35	MD31	MD27	MD23	MD19	MD14	MD10	MD6	MD1	TA4	TAGWE#	CS1#	HD2	HD6	HD11	HD15	HD19	HD22	HD31	HD32	HD33	C
D	MA0A	MA1A	MA0B	MA1B	MA2	MD48	MD44	MD40	MD36	MD32	MD28	MD24	MD20	MD15	MD11	MD7	MD2	TA5	TA0	BWE#	HD1	HD5	HD10	HD14	HD18	HD34	HD35	HD36	HD37	D
E	MA3	MA4	MA5	MA6	GND (OVSS)	GND (DVSS)	VCC35 (OVCC)	GND (OVSS)	VCC35 (OVCC)	MD60	MD59	GND (OVSS)	VCC35 (OVCC)	MD16	GND (OVSS)	VCC5 (DVDD)	MD3	TA6	TA1	GWE#	GND (OVSS)	VCC3 (OVDD)	HD9	GND (DVSS)	GND (OVSS)	HD38	HD39	HD40	HD41	E
F	MA7	MA8	MA9	MA10	VCC35 (OVCC)	F	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	F	HD42	HD43	HD44	HD45	HD46	F
G	MA11	RAMWA#	RAMWB#	CAS0 /DQM0#	GND (OVSS)	G																		G	HD47	HD48	HD49	HD50	HD51	G
H	CAS1 /DQM1#	CAS2 /DQM2#	CAS3 /DQM3#	CAS4 /DQM4#	GND (OVSS)	H																		H	HD52	HD53	HD54	HD55	HD56	H
J	CAS5 /DQM5#	CAS6 /DQM6#	CAS7 /DQM7#	SRAS~~0~~1#	VCC35 (OVCC)	J																		J	GND (OVSS)	HD57	HD58	HD59	HD60	J
K	RAS1 /CS1#	RAS2 /CS2#	RAS3 /CS3#	RAS4 /SRAS~~0~~1#	RAS5 /SCAS~~1~~0#	K																		K	VCC3 (OVDD)	HD61	HD62	HD63	HA31	K
L	RAS0#	SCAS~~1~~0#	ID0	ID1	ID2	L																		L	HA30	HA29	HA28	HA27	HA26	L
M	ID3	ID4	ID5	ID6	ID7	M						GND	GND	GND	GND	GND	GND	GND						M	HA25	HA24	HA23	HA22	HA21	M
N	ID8	ID9	ID10	ID11	ID12	N						GND	GND	GND	GND	GND	GND	GND						N	HA20	HA19	HA18	HA17	HA16	N
P	ID13	ID14	ID15	ICS0#	GND (OVSS)	P						GND	GND	GND	GND	GND	GND	GND						P	HA15	HA14	HA13	HA12	HA11	P
R	ICS1#	DIOR0#	DIOR1#	DIOW0#	VCC5 (DVDD)	R						GND	GND	GND	GND	GND	GND	GND						R	GND (OVSS)	HA10	HA9	HA8	HA7	R
T	DIOW1#	DIO-CHRDY	DDREQ0	DDREQ1	DDACK0#	T						GND	GND	GND	GND	GND	GND	GND						T	VCC5 (DVCC)	HA6	HA5	HA4	HA3	T
U	DDACK1#	DIRQ0 /IRQ14	DIRQ1 /IRQ15	DSA0	DSA1	U						GND	GND	GND	GND	GND	GND	GND						U	HBE7#	HBE6#	HBE5#	HBE4#	HBE3#	U
V	PCICLK	DSA2	C/BE0#	C/BE1#	VCC5 (OVCC)	V						GND	GND	GND	GND	GND	GND	GND						V	VCC3 (OVDD)	HBE2#	HBE1#	HBE0#	CPUCLK	V
W	C/BE2#	C/BE3#	AD0	AD1	GND (OVSS)	W																		W	INIT	CPURST	NMI	INTR	STPCLK	W
Y	AD2	AD3	AD4	AD5	AD6	Y																		Y	A20M#	SMIACT#	SMI#	IGNNE#	FERR#	Y
AA	AD7	AD8	AD9	AD10	AD11	AA																		AA	GND (OVSS)	HITM#	EADS#	FLUSH#	HLOCK#	AA
AB	AD12	AD13	AD14	AD15	VCC5 (OVCC)	AB																		AB	AHOLD	BOFF#	NA#	KEN# /INV	CACHE#	AB
AC	AD16	AD17	AD18	AD19	GND (OVSS)	AC																		AC	BRDY#	W/R#	D/C#	M/IO#	ADS#	AC
AD	AD20	AD21	AD22	AD23	GND (OVSS)	AD	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	AD	USBCLK	UV0-	UV~~0~~1+	UV1-	UV~~1~~0+	AD
AE	AD24	AD25	AD26	AD27	GND (DVSS)	INTB#	GND (OVSS)	ZWS#	DRQ1	VCC5 (OVCC)	DACK3	SA1	GND (OVSS)	SA10	VCC5 (DVDD)	GND (OVSS)	LA20	SD1	VCC5 (OVCC)	SD10	SD15	VCC5 (DVSS)	IO16#	GND (OVSS)	GND (DVSS)	KBCLK /PD3	MDRQ# /RING#	ONCTL# /RTCALE	SWITCH	AE
AF	AD28	AD29	AD30	AD31	TRDY#	INTA#	MWDC#	SMWTC#	DRQ0	DRQ6	DACK2#	SA0	SA5	SA9	SA14	SA18	LA19	SD0	SD5	SD9	SD14	IRQ6	IRQ12	CHRDY	MR16#	IRQ9	KBDAT	PMDAT	PSRSTB#	AF
AG	PAR	SERR#	PREQ0#	PGNT4#	IRDY#	PLOCK#	MRDC#	SMRDC#	EOP	DRQ5	DACK1#	DACK7#	SA4	SA8	SA13	SA17	LA18	LA23	SD4	SD8	SD13	IRQ5	IRQ11	AEN	BALE	MIRQ – /~~SINT~~	RSTDRV	PMCLK	PWRGD	AG
AH	PREQ1#	PREQ2#	PGNT1#	PGNT3#	FRAME#	DEVSEL#	INTD#	IOWC#	SBHE#	DRQ3	DACK0#	DACK6#	SA3	SA7	SA12	SA16	LA17	LA22	SD3	SD7	SD12	IRQ4	IRQ10	M16#~~14 MHZ~~	IOCHK#	MDACK# /KLOCK#	ROM-KBSC#	SPEAK	RTCVDD	AH
AJ	PREQ3#	PREQ4#	PGNT0#	PGNT2#	PCIRST#	STOP#	INTC#	IORC#	RFH#	DRQ2	DRQ7	DACK5#	SA2	SA6	SA11	SA15	SA19	LA21	SD2	SD6	SD11	IRQ7	IRQ3	~~14MHZ M16#~~	BCLK	TURBO# /BREAK#	GPIO	OSCI /IRQ8#	OSCO /RTCCS#	AJ
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	

7.2 Pin Description

BALL	NAME	TYPE ATTR	DESCRIPTION
AG29	PWRGD	IN 5V	Power Good is a power on reset and push button reset input.
W26	CPURST	OUT 3V	Reset CPU is an active high output to reset the CPU.
W25	INIT	OUT 3V	The Initialization output forces the CPU to begin execution in a known state. The CPU state after INIT is the same as the state after CPURST except that the internal caches, model specific registers, and floating point registers retain the values they had prior to INIT.
V29	CPUCLK	CLK 3V	Host clock. Primary clock input to drive the part.
AC29	ADS#	IN 3V	Address Status is driven by the CPU to indicate the start of a CPU bus cycle.
AC28	M/IO#	IN 3V	Memory I/O definition is an input to indicate an I/O cycle when low, or a memory cycle when high.
AC27	D/C#	IN 3V	Data/Code is used to indicate whether the current cycle is a data or code access.
AC26	W/R#	IN 3V	Write/Read from the CPU indicates whether the current cycle is a write or read access.
AC25	BRDY#	OUT 3V	Burst Ready indicates that data presented are valid during a burst cycle.
AB29	CACHE#	IN 3V	The Cache pin indicates an L1 internally cacheable read cycle or a burst write-back cycle. If this pin is driven inactive during a read cycle, the CPU will not cache the returned data, regardless of the state of the KEN# pin.
AB28	KEN#/ INV	OUT 3V	This function as both the KEN# signal during CPU read cycles, and the INV signal during L1 snoop cycles. During CPU cycles, KEN/INV is normally low. KEN#/INV will be driven high during the 1st BRDY# or NA# assertion of a non-L1-cacheable CPU read. KEN#/INV is driven high(low) during the EADS# assertion of a PCI master DRAM write(read) snoop cycle.
AB27	NA#	OUT 3V	The 5571 always asserts NA# no matter the burst, or pipelined burst SRAMs are used.

AB26	BOFF#	OUT 3V	The 5571 asserts BOFF# to stop the current CPU cycle.
AB25	AHOLD	OUT 3V	The 5571 asserts AHOLD when a PCI master is performing a cycle to DRAM. AHOLD is held for the duration of PCI burst transfer. The 5571 negates AHOLD when the completion of PCI to DRAM read or write cycles complete and during PCI peer transfers.
AA29	HLOCK#	IN 3V	When HLOCK# asserted by CPUCLK, 5571 grants this is a CPU locked cycle.
AA28	FLUSH#	OUT 3V	It is used to slow down the system in deturbo mode.
AA27	EADS#	OUT 3V	The EADS# is driven to indicate that a valid external address has been driven to the CPU address pins to be used for an inquire cycle.
AA26	HITM#	IN 3V	Hit Modified indicates the snoop cycle hits a modified line in the L1 cache of the CPU.
Y29	FERR#	IN 3V	Floating point error from the CPU. It is driven active when a floating point error occurs.
Y28	IGNNE#	OUT 3V	IGNNE# is normally in high impedance state, and is asserted to inform CPU to ignore a numeric error. A resistor connected to 3.3V is required to maintain a correct voltage level to CPU.
Y27	SMI#	OUT 3V	System Management Interrupt is used to indicate the occurrence of system management events. It is connected directly to the CPU SMI# input.
Y26	SMIACT#	IN 3V	The SMIACT# pin is used as the SMI acknowledgment input from the CPU to indicate that the SMI# is being acknowledged and the processor is operating in System Management Mode(SMM).
Y25	A20M#	OUT 3V	A20 Mask is the fast A20GATE output to the CPU. It remains high during power up and CPU reset period. It forces A20 to go low when active.
W29	STPCLK	OUT 3V	Stop Clock indicates a stop clock request to the CPU.
W28	INTR	OUT 3V	Interrupt goes high whenever a valid interrupt request is asserted.
W27	NMI	OUT 3V	Non-maskable interrupt is rising edge trigger signal to the CPU and is generated to invoke a non-maskable interrupt. Normally, this signal is low. It goes high state when a non-maskable interrupt source comes up.

U25, U26, U27, U28, U29, V26, V27, V28	HBE[7:0]#	I/O 3V	CPU Byte Enables indicate which byte lanes on the CPU data bus carry valid data during the current bus cycle. HBE7# indicates that the most significant byte of the data bus is valid while HBE0# indicates that the least significant byte of the data bus is valid.
K29, L25, L26, L27, L28, L29, M25, M26, M27, M28, M29, N25, N26, N27, N28, N29, P25, P26, P27, P28, P29, R26, R27, R28, R29, T26, T27, T28, T29	HA[31:3]	I/O 3V	The CPU Address is driven by the CPU during CPU bus cycles. The 5571 forwards it to either the DRAM or the PCI bus depending on the address range. The address bus is driven by the 5571 during bus master cycles.

K28, K27, K26, J29, J28, J27, J26, H29, H28, H27, H26, H25, G29, G28, G27, G26, G25, F29, F28, F27, F26, F25, E29, E28, E27, E26, D29, D28, D27, D26, C29, C28, C27, B29, B28, A29, A28, A27, B27, A26, B26, C26, A25, B25, C25, D25, A24, B24, C24, D24, A23, B23, C23, D23, E23, A22, B22, C22, D22, A21, B21, C21, D21, A20	HD63	I/O 3V	CPU data bus.
B20	KOE#	OUT 3V	Cache Read Enable for standard SRAM, or Cache Output Enable for burst and pipelined burst SRAM.
C20	CS1#	OUT 3V	A L2 cache consisting of burst SRAMs will power up, if necessary, and perform an access if this signal is asserted when ADSC# is asserted. A L2 cache consisting of burst SRAMs will power down if this signal is negated when ADSC# is asserted. When CS1# is negated a L2 cache consisting of burst SRAMs ignores ADS#. If CS1# is asserts when ADS# is asserted a L2 cache consisting burst SRAMs will power up, if necessary, and perform an access.

E20	GWE#	OUT 3V	Global-write Enable. GWE# asserted causes a QWORD to be written into the L2. It is used for L2 line fills.
D20	BWE#	OUT 3V	Byte-write Enable. When GWE#=1, the assertion of BWE# causes the byte lanes that are enabled via the CPU's HBE[7:0]# signals to be written into the L2, if they are powered up.
A19	ADSC#	OUT 3V	Cache address strobe for burst and pipelined burst SRAM.
B19	ADSV#	OUT 3V	Cache address advance for burst and pipelined burst DRAM.
C19	TAGWE#	OUT 5V	TAG RAM write enable output.
A17, E18, D18, C18, B18, A18, E19, D19	TA[7:0]	I/O 3V/5V	TAG RAM data bus lines. The voltage level must be the same as DRAM voltage level.
C2, C1, B1,E10,E11, A2, C3, B3, A3, C4, B4, A4, C5, B5, A5, D6, C6, B6, A6, D7, C7, B7, A7, D8, C8, B8, A8, D9, C9, B9, A9, D10, C10, B10, A10, D11, C11, B11, A11, D12, C12, B12, A12, D13, C13, B13, A13, E14, D14, C14, B14, A14, D15, C15, B15, A15, D16, C16, B16, A16, E17, D17, C17, B17	MD[63:0]	I/O 3V/5V	Memory data bus.
D1, D3	MA0[A:B]	OUT 3V/5V	Memory address 0. Two copies are provided for loading purposes.

D2, D4	MA1[A:B]	OUT 3V/5V	Memory address 1. Two copies are provided for loading purposes.
G1, F4, F3, F2, F1, E4, E3, E2, E1, D5	MA[11:2]	OUT 3V/5V	Memory address 11-2 are the row and column addresses for DRAM.
G2, G3	RAMWA# RAMWB#	OUT 3V/5V	RAM Write is an active low output signal to enable local DRAM writes. Two copies are provided for loading purposes.
J3, J2, J1, H4, H3, H2, H1, G4	CAS[7:0]#/ DQM[7:0]	OUT 3V/5V	(FP/EDO)DRAM Column address strobe 7-0 for byte 7-0. SDRAM output enables during a read cycle and a byte mask during a write cycle.
K3, K2, K1, L1	RAS[3:0]#/ CS[3:0]#	OUT 3V/5V	(FP/EDO)DRAM Row address strobe 3-0 for DRAM banks 1-0. SDRAM chip select. These pins activate the SDRAM and accept any command when it is low.
K4	RAS4#/ SRAS~~0~~1#	OUT 3V/5V	(FP/EDO)DRAM Row address strobe 3-0 for DRAM banks 2. SDRAM Row address strobe. It latch row address on the positive edge of the clock with SRAS[0:1]# low. These signals enable row access and precharge.
K5	RAS5#/ SCAS~~0~~1#	OUT 3V/5V	(FP/EDO)DRAM Row address strobe 3-0 for DRAM banks 2. SDRAM Column address strobe. It latch column address on the positive edge of the clock with SCAS[0:1]# low. These signals enable column access.
J4	SRAS~~1~~0#	OUT 3V/5V	SDRAM Row address strobe. Two copies are provided for loading purposes.
L2	SCAS~~1~~0#	OUT 3V/5V	SDRAM Column address strobe. Two copies are provided for loading purposes.
AJ5	PCIRST#	OUT 5V	The PCI Reset forces the PCI devices to a known state.
V1	PCICLK	CLK 5V	The PCICLK input provides the fundamental timing and the internal operating frequency for the 5571. It runs at the same frequency and skew of the PCI local bus.
W2,W1, V4,V3	C/BE[3:0]#	I/O 5V	PCI Bus Command and Byte Enables define the PCI command during the address phase of a PCI cycle, and the PCI byte enables during the data phases. C/BE[3:0]# are outputs when the 5571 is a PCI bus master and inputs when it is a PCI slave.

AF4, AF3, AF2, AF1, AE4, AE3, AE2, AE1, AD4, AD3, AD2, AD1, AC4, AC3, AC2, AC1, AB4, AB3, AB2, AB1, AA5, AA4, AA3, AA2, AA1, Y5, Y4, Y3, Y2, Y1, W4, W3,	AD[31:0]	I/O 5V	PCI Address /Data Bus *In address phase:* 1. When the 5571 is a PCI bus master, AD[31:0] are output signals. 2. When the 5571 is a PCI target, AD[31:0] are input signals. *In data phase:* 1. When the 5571 is a target of a memory read/write cycle, AD[31:0] are floating. 2. When the 5571 is a target of a configuration or an I/O cycle, AD[31:0] are output signals in a read cycle, and input signals in a write cycle.
AG1	PAR	I/O 5V	Parity is an even parity generated across AD[31:0] and C/BE[3:0]#.
AH5	FRAME#	I/O 5V	FRAME# is an output when the 5571 is a PCI bus master. The 5571 drives FRAME# to indicate the beginning and duration of an access. When the 5571 is a PCI slave, FRAME# is an input signal.
AG5	IRDY#	I/O 5V	IRDY# is an output when the 5571 is a PCI bus master. The assertion of IRDY# indicates the current PCI bus master's ability to complete the current data phase of the transaction. For a read cycle, IRDY# indicates that the PCI bus master is prepared to accept the read data on the following rising edge of the PCI clock. For a write cycle, IRDY# indicates that the bus master has driven valid data on the PCI bus. When the 5571 is a PCI slave, IRDY# is an input.
AF5	TRDY#	I/O 5V	TRDY# is an output when the 5571 is a PCI slave. The assertion of TRDY# indicates the target agent's ability to complete the current data phase of the transaction. For a read cycle, TRDY# indicates that the target has driven valid data onto the PCI bus. For a write cycle, TRDY# indicates that the target is prepared to accept data from the PCI bus. When the 5571 is a PCI master, it is an input.
AJ6	STOP#	I/O 5V	STOP# indicates that the bus master must start terminating its current PCI bus cycle at the next clock edge and release control of the PCI bus. STOP# is used for disconnect, retry, and target-abort sequences on the PCI bus.

AH6	DEVSEL#	I/O 5V	The 5571 drives DEVSEL# based on the DRAM address range being accessed by a PCI bus master or if the current configuration cycle is to the 5571. As an input it indicates if any device has responded to current PCI bus cycle initiated by the 5571.
AG6	PLOCK#	IN 5V	PCI Lock indicates an exclusive bus operation that may require multiple transactions to complete. When PLOCK# is sampled asserted at the beginning of a PCI cycle, the 5571 considers itself a locked resource and remains in the locked state until PLOCK# is sampled negated on a new PCI cycle.
AJ1, AH2, AH1, AG3	PREQ[3:0]#	IN 5V	PCI Bus Request is used to indicate to the PCI bus arbiter that an agent requires use of the PCI bus.
AH4, AJ4, AH3, AJ3	PGNT[3:0]#	OUT 5V	PCI Bus Grant indicates to an agent that access to the PCI bus has been granted.
AJ2	PREQ4#/	IN 5V	This pin is used as PREQ4#.
AG4	PGNT4#/	OUT 5V	This pin is used as PGNT4#.
AF6, AE6, AJ7, AH7	INT[A:D]#	IN 5V	PCI Interrupt A to Interrupt D
AG2	SERR#	IN 5V	SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, the 5571 generates a non-maskable interrupt to the CPU.
P3, P2, P1, N5, N4, N3, N2, N1, M5, M4, M3, M2, M1, L5, L4, L3	ID[15:0]	I/O 5V	IDE data bus.
R1, P4	ICS[1:0]#	OUT 5V	IDE chip select signals.
R3, R2	DIOR[1:0]#	OUT 5V	IDE I/O read cycle command.
T1, R4	DIOW[1:0]#	OUT 5V	IDE I/O write cycle command
T2	DIOCHRDY	IN 5V	IDE I/O channel ready signal.
T4, T3	DDREQ1 DDREQ0	IN 5V	IDE DMA request signals.
U1, T5	DDACK1# DDACK0#	OUT 5V	IDE DMA acknowledge signals.

U3, U2	DIRQ[1:0]/ IRQ[15:14]	IN 5V	IDE interrupt request signals. These are the synchronous interrupt request inputs to the 8259 controller.
V2, U5, U4	DSA[2:0]	OUT 5V	IDE address [2:0].
AHJ24	14MHz	OUT 5V	It is the buffered input of the external 14.318MHz oscillator.
AG27	RSTDRV	OUT 5V	This signal asserts during a hard reset and during power-up to reset ISA bus devices.
AJ25	BCLK	OUT 5V	ISA bus clock, for ISA bus controller, ISA bus interfaces and the DMA controller. It can be programmed to derive from the SYSCLK or from the 14MHz clock.
AE23	IO16#	IN 5V	16-bit I/O chip select indicates that the AT bus cycle is a 16-bit I/O transfer when asserted or an 8-bit I/O transfer when it is negated.
AJH24	M16#	IN 5V	16-bit memory chip select indicates a 16-bit memory transfer when asserted or an 8-bit memory transfer when it is negated.
AG24	AEN	OUT 5V	Address Enable is driven high on the ISA bus to indicate the address lines are valid in DMA or ISA master cycles. It is low otherwise.
AF24	CHRDY	I/O 5V	I/O channel ready is normally high. It can be pulled low by the slow devices on the AT bus to add wait states for the ISA memory or I/O cycles. When a DMA or an ISA master accesses a target, IORDY is an output to control the wait states.
AH25	IOCHK#	IN 5V	I/O channel Check is an active low input signal which indicates that an error has taken place on the I/O bus.
AG25	BALE	OUT 5V	Bus address latch enable is used on the ISA bus to latch valid address from the CPU. Its falling edge starts the ISA command cycles.
AF25	MR16#	IN 5V	Master is an active low signal from AT bus. When active, it indicates that the ISA bus master has the control of the system. The address and control signals are all driven by the ISA bus master.
AG7	MRDC#	I/O 5V	AT bus memory read command signal is an output pin during AT/DMA/refresh cycles and is an input pin in ISA master cycles.
AF7	MWTC#	I/O 5V	AT bus memory write command signal is an output pin during AT/DMA cycles and is an input pin in ISA master cycles.

AJ8	IORC#	I/O 5V	AT bus I/O read command signal is an output pin during AT or DMA cycles and is an input pin in ISA master cycles. When low, it strobes an I/O device to place data on the data bus.
AH8	IOWC#	I/O 5V	AT bus I/O write command signal is an output pin during AT or DMA cycles and is an input pin in ISA master cycles. When low, it strobes data on the data bus into a selected I/O device.
AG8	SMRDC#	OUT 5V	AT bus memory read. It instructs the memory devices to drive data onto the data bus. It is active only when the memory being accessed is within the lowest 1MB.
AF8	SMWTC#	OUT 5V	AT bus memory write. It instructs the memory devices to store the data presented on the data bus. It is active only when the memory being accessed is within the lowest 1MB.
AE8	ZWS#	IN 5V	Zero wait state is an active low signal. The system ignores the IORDY signal and terminates the AT bus cycle without additional wait state when it is asserted.
AJ9	RFH#	I/O 5V	Refresh signal is used to initiate a refresh cycle. This signal is an input in ISA bus master cycles and is an output in other cycles.
AH9	SBHE#	I/O 5V	Byte high enable signal indicates that the high byte has valid data on the ISA 16-bit data bus. This signal is an output except during ISA master cycles.
AG9	EOP	OUT 5V	Terminal Count of DMA. A pulse is generated by the DMA controller when the terminal count (TC) of any channel reaches 1.When a TC pulse occurs, the DMA controller will terminate the service, and if auto-initialize is enabled, the base registers will be written to the current registers of that channel. The mask bit and the TC bit in the Status word will be set for the currently active channel unless the channel is programmed for auto-initialize. In that case, the mask bit remains clear.
AE21, AF21, AG21, AH21, AJ21, AE20, AF20, AG20, AH20, AJ20, AF19, AG19, AH19, AJ19, AE18, AF18	SD[15:0]	I/O 5V	System Data Bus are directly connected to the ISA slots.

AJ17, AF16, AG16, AH16, AJ16, AF15, AG15, AH15, AJ15, AE14, AF14, AG14, AH14, AJ14, AF13, AG13, AH13, AJ13, AE12, AF12	SA[19:0]	I/O 5V	System address. They are inputs when an external bus master is in control and are outputs at all other times.
AG18, AH18, AJ18, AE17, AF17, AG17, AH17	LA[23:17]	I/O 5V	Latched system address. They are inputs when an external bus master is in control and are outputs at all other times.
AJ23, AH22, AG22, AF22, AJ22, AF26, AH23, AG23, AF23	IRQ[3:7], IRQ[9:12]	IN 5V	These are the synchronous interrupt request inputs to the 8259 controller.
AF9, AE9, AJ10, AH10, AG10, AF10, AJ11	DRQ[0:3], DRQ[5:7]	IN 5V	DMA Request inputs are used by external devices to indicate when they need service from the internal DMA controllers.
AH11, AG11, AF11, AE11, AJ12, AH12, AG12	DACK[0:3]#, DACK[5:7]#	OUT 5V	DMA acknowledge output are used by external devices to indicate when they need service from the internal DMA controllers.
AH27	ROMKBSC#	OUT 5V	Keyboard or System ROM Chip Select. When asserted, it means the keyboard or ROM is to be accessed. Also, a high logic trapped on the PCICLK rising shows the support of the external super I/O.
AH28	SPKR	OUT 5V	Speaker is the output for the speaker.
AF27	KBDAT/ IRQ1	I/O 5V	When the internal KBC is enabled, this pin is used as the keyboard data. Otherwise, it is the IRQ1 signal use for external KBC.

AJ26	TURBO/ BREAK#	I/O 5V	When this signal be programmed as TURBO. This pin is used to slow down the system by connecting it to ground. When this signal be programmed as BREAK#. A signal from the break switch will cause the system enters the standby state. The pulse width of the BREAK# must greater than 4 CPUCLK.
AH26	MDACK#/ KLOCK#	I/O 5V	The pin is the motherboard DMA acknowledge signal associated with the MDRQ# when Reg 70h bit4=0.~~.~~ ~~And~~ T~~t~~his pin can used as the keyboard lock signal if internal KBC is enabled and Reg 70h bit4=1.~~.~~
AG26	MIRQ~~/ SINT~~	I/O 5V	This pin ~~can be~~is used as motherboard interrupt request. ~~This pin can also be used as the serial interrupt pin.~~
AE26	KBCLK	I/O 5V	When the internal KBC is enabled, this pin is used as the keyboard clcok.
AJ27	GPIO	I/O 5V	~~GPIO: General purpose I/O.~~Reg.66h bits 1:0=10, it can be either active low or high by programming Reg.65h.
AG28	PMCLK	I/O 5V	When internal KBC is enabled, it can be served as PS2 mouse clock.
AF28	PMDAT	I/O 5V	When in input mode, it functions as PSMDAT if PS/2 mouse is enabled.
AE27	MDRQ#/ RING#/	I/O 5V	The pin is the motherboard DMA request signal associated with the MDACK#. And it can be programmed as MODEM ring in function. When enable, detection of RING# pulse or pulse train activates the ONCTL# pin. The pulse must be 62.5ms at least, and only one pulse in a sec. Engineering note: Input is blocked to reduce leakage current when either the APC‘s ring event is disabled or the APC is powered by RTCVDD.
AE29	SWITCH	IN 5V	Power On/Off switch. Indicated a Switch On/Off request. When Vdd does not exist, a low to high transition on this pin indicates a Switch off event. The pin has an internal pull-down of 50K (normal), a schmitt-trigger input buffer and a debounce protection of at least 14ms.

AE28	ONCTL#/ RTCALE	OUT 5V	Power ON/OFF control. This open-drain output, powerd by the RTC supply, signals the main power supply that power should be turned on. When using external RTC: The signal is used to latch the address from the SD bus when CPU accesses RTC.
AH29	RTCVDD	IN 5V	Power for RTC internal RTC.
AJ28	OSCI/ IRQ8#	IN 5V	When using internal RTC: This pin is used as the time base of the built-in RTC. This signal should be connected to 32.768 KHz crystal or oscillator input. When using external RTC: This pin is used as IRQ8#, which is the asynchronous interrupt request input to the 8259 controller.
AJ29	OSCO/ RTCCS#	OUT 5V	When using internal RTC: this pin should be connected the other end of the 32.768 KHz crystal or left connected if an oscillator is used. When using external RTC: This pin is used as chip select of RTC. It combine with IOR# and IOW# to generate RTCRD# and RTCWR#, that are used to store the data presented on the XD bus when CPU accesses the RTC.
AF29	PSRSTB#	IN 5V	When using internal RTC: This signal is used as PSRSTB# (power strobe). PSRSTB# establishes the condition of the control register in RTC when power is first applied to the device.
AD25	UCLK	CLK 5V	the USB clock source.
AD29~~7~~, AD26	UV0+, UV0-	I/O 3V	When USB function port 0. These two pins are used as the differential inputs of the USB port 0.
AD27~~9,~~ AD28	UV1+, UV1-	I/O 3V	When USB function port 1. These two pins are used as the differential inputs of the USB port 1.
E16, T25, AE15, AE22, R5	VCC5	PWR DVDD	+5V DC power.
V5, AB5, AE10, AE19	VCC5	PWR OVDD	+5V DC power.
F5, J5, E13, E9, E7	VCC35	PWR OVDD	3V or 5V DC power. Connected to 5V for 5V DRAM. Connected to 3V for 3V DRAM.
V25, K25, E22	VCC3	PWR OVDD	+5V DC power
E24, AE25, AE5, E6	GND	PWR DVSS	Ground.

E5, G5, H5, P5, W5, AC5, AD5, AE7, AE13, AE16, AE24, AA25, R25, J25, E25, E21, E15, E12, E8, B2, A1	GND	PWR OVSS	Ground.

8. HardwWare Trap

The following is a summary of all the power on options that are loaded into the PSIO based on the voltage level presented on the respective strapping at the rising edge of PCIRST#.

Pin No	Symbol	Description
C2	MD63	Internal PS/2 mouse enable/disable Pull-up : Enable internal PS/2 mouse ~~Once builtin PS/2 is employed, pin PMCLK/PD5 is PMCLK and pin PMDAT/PD6 is PMDAT, otherwise it is PD5 and PD6.~~
C1	MD62	Internal/External KBC Select: Pull-up: Internal KBC is enabled. Pull-down: Internal KBC is disabled. Once builtin KBC is employed, pin KBDAT/IRQ1 is KBDAT ~~and pin KBCLK/PD3 is KBCLK~~, otherwise it is IRQ1 ~~and PD3~~.
B1	MD61	Pull-up: Enable ROM cycle to be conducted in zero wait state ~~for backward compatibility purpose~~.
B4	MD53	Pulled low: enable internal PLL circuit for optimizing timing.
C4, A3, B3	MD54,55,56	Chipset will sense these pins to understand bus frequency, then to adjust internal timing.
AF29	PSRSTB#	Connect to battery‘s power strobe: Select internal RTC. Pull-down: Select external RTC.

Note:

1. MD57, MD59, MD60 should be pulled low for normal function, otherwise chipset will enter internal test mode.

2.

MD56	MD55	MD54	Frequency
0	0	1	75MHz
0	1	0	66MHz
0	1	1	60MHz
1	0	1	50MHz

9. DC Characteristics

Table 9-1 DC Characteristics

Ta= 0 - 70°C, Gnd= 0V, Vcc5= 5V+5%, Vcc3=3.3V+5%, Vcc35=3.3/5V+5%

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL1}	Input Low Voltage	-0.3	0.8	V	Note 1, V_{CC3}=3.3V +5%
V_{IH1}	Input High Voltage	2.2	V_{CC3}+0.3	V	Note 1
V_{IL2}	Input Low Voltage	-0.3	0.8	V	Note 2
V_{IH2}	Input High Voltage	2.2	V_{CC5}+0.3	V	Note 2
V_{T1-}	Schmitt Trigger Threshold Voltage Falling Edge	1.6		V	Note 3
V_{T1+}	Schmitt Trigger Threshold Voltage Rising Edge	3.2	V		Note 3
V_{H1}	Hysteresis Voltage	0.3	1.2	V	Note 3
V_{OL1}	Output Low Voltage		0.45	V	Note 4
V_{OH1}	Output High Voltage	2.4		V	Note 4
V_{OL2}	Output Low Voltage		0.4	V	Note 5
V_{OH2}	Output High Voltage	2.0	2.4	V	Note 5
V_{OL3}	Output Low Voltage		0.4	V	Note 6
V_{OH3}	Output High Voltage	2.0	V_{CC35}	V	Note 6
I_{OL1}	Output Low Current	8		mA	Note 7
I_{OH1}	Output High Current	-8		mA	Note 7
I_{OL2}	Output Low Current	16		mA	Note 8
I_{OH2}	Output High Current	-16		mA	Note 8
I_{OL3}	Output Low Current	8,16		mA	Note 9
I_{OH3}	Output High Current	-8,-16		mA	Note 9
I_{OL4}	Output Low Current	4		mA	Note 10
I_{OH4}	Output high Current	-4		mA	Note 10
I_{IH}	Input Leakage Current		-10	µA	
I_{IL}	Input Leakage Current		+10	µA	
C_{IN}	Input Capacitance		12	pF	Fc=1 Mhz
C_{OUT}	Output Capacitance		12	pF	Fc=1 Mhz
$C_{I/O}$	I/O Capacitance		12	pF	Fc=1 Mhz

NOTE:

1. V_{IL1} and V_{IH1} are applicable to 3V input signals.

2. V_{IL2} and V_{IH2} are applicable to 5V input signals.
3. V_{T1-}, V_{T1+} and V_{H1} are applicable to PWRGD
4. V_{OL1} and V_{OH1} are applicable to 5V output signals.
5. V_{OL2} and V_{OH2} are applicable to 3V output signals.
6. V_{OL3} and V_{OH3} are applicable to 3/5 V output signals.
7. I_{OL1} and I_{OH1} are applicable to the following signals: TA[7:0], TAGWE#, AD[31:0], C/BE[3:0]#, GNT[3:0]#, STOP#, DEVSEL#, TRDY#, FRAME#, SERR#, GPIO, CPURST, IRDY#
8. I_{OL2} and I_{OH2} are applicable to the following signals: ADSC#, ADSV#, GWE#, BWE#
9. I_{OL3} and I_{OH3} are applicable to the following signals: RAS[5:0]#, CAS[7:0]#, RAMW[A:B]#, MA[11:0]#
10. I_{OL4} and I_{OH4} are applicable to the following signals: KOE#, STPCLK#, INIT, SMI#, HA[31:3], W/R#, EADS#, NA#, BRDY#, KEN#, PAR, A20M#, PCIRST#, BOFF#

9.1 AC Characteristics

Table 9-2 AC Characteristics

Sym	Parameter	Max	Unit	CL
T1	BRDY# Active delay from CPUCLK	7.0	ns	35pf
T2	BRDY# Inactive delay from CPUCLK	7.3	ns	35pf
T3	KEN# Active delay from CPUCLK	7.2	ns	35pf
T4	KEN# Inactive delay from CPUCLK	7.4	ns	35pf
T5	NA# Active delay from CPUCLK	8	ns	35pf
T6	NA# Inactive delay from CPUCLK	8.5	ns	35pf
T7	BOFF Active delay from CPUCLK	6.5	ns	35pf
T8	BOFF Inactive delay from CPUCLK	7.3	ns	35pf
T9	AHOLD Active delay from CPUCLK	7.9	ns	35pf
T10	AHOLD Inactive delay from CPUCLK	7.7	ns	35pf
T11	EADS# Active delay from CPUCLK	5.7	ns	35pf
T12	EADS# Inactive delay from CPUCLK	5.6	ns	35pf
T13	CPURST Inactive delay from CPUCLK	9.0	ns	35pf
T14	CPURST Active delay from CPUCLK	8.3	ns	35pf
T15	KOE# Active delay from CPUCLK	5.4	ns	50pf
T16	KOE# Inactive delay from CPUCLK	6.2	ns	50pf
T17	CS1# Active delay from CPUCLK	5.9	ns	50pf
T18	CS1# Inactive delay from CPUCLK	6.6	ns	50pf
T19	BWE# Active delay from CPUCLK	5.5	ns	50pf
T20	BWE# Inactive delay from CPUCLK	6.4	ns	50pf
T21	GWE# Active delay from CPUCLK	5.9	ns	50pf
T22	GWE# Inactive delay from CPUCLK	6.1	ns	50pf
T23	ADSC# Active delay from CPUCLK	7.6	ns	50pf
T24	ADSC# Inactive delay from CPUCLK	5.4	ns	50pf

T25	ADV# Active delay from CPUCLK	7.6	ns	50pf

T26	ADV# Inactive delay from CPUCLK	5.4	ns	50pf
T27	TAGWE# Active delay from CPUCLK	6.3	ns	35pf
T28	TAGWE# Inactive delay from CPUCLK	5.1	ns	35pf
T29	TA[7:0] delay from TAGWE#	1.3	ns	35pf
T30	RAS[3:0]# Active delay from CPUCLK	9.7	ns	100pf
T31	RAS[3:0]# Inactive delay from CPUCLK	10	ns	100pf
T32	RAS[5:4]# Active delay from CPUCLK	10.4	ns	100pf
T33	RAS[5:4]# Inactive delay from CPUCLK	10.7	ns	100pf
T34	SRAS1# Active delay from CPUCLK	7.9	ns	100pf
T35	SCAS1# Inactive delay from CPUCLK	7.9	ns	100pf
T36	MD[63:0] delay from CPUCLK	10.9	ns	50pf
T37	CAS[7:0]# Active delay from CPUCLK	8.1	ns	100pf
T38	CAS[7:0]# Inactive delay from CPUCLK	7.3	ns	100pf
T39	MA[11:0] Low Valid delay from CPUCLK	14.74	ns	280pf
T40	MA[11:0] High Valid delay from CPUCLK	12.7	ns	280pf
T41	RAMW[A:B]# Active delay from CPUCLK	13.7	ns	376pf
T42	RAMW[A:B]# Inactive delay from CPUCLK	14.86	ns	376pf
T43	PAR Active delay from PCICLK	11.8	ns	50pf
T44	PAR Inactive delay from PCICLK	9.4	ns	50pf
T45	STPCLK# Active delay from PCICLK	15	ns	50pf
T46	STPCLK# Inactive delay from PCICLK	15	ns	50pf
T47	SMI# rise time to CPUCLK	10	ns	35pf
T48	SMI# fall time to CPUCLK	10	ns	35pf
T49	AD[31:0], C/BE[3:0]# Active delay from PCICLK	11.4	ns	50pf
T50	AD[31:0], C/BE[3:0]# Inactive delay from PCICLK	15.2	ns	50pf
T51	FRAME# Active delay from PCICLK	15.0	ns	50pf
T52	FRAME# Inactive delay from PCICLK	16.5	ns	50pf
T53	IRDY# Active delay from PCICLK	11.1	ns	50pf
T54	IRDY# Inactive delay from PCICLK	9.0	ns	50pf
T55	TRDY# Active delay from PCICLK	12.3	ns	50pf
T56	TRDY# Inactive delay from PCICLK	8.9	ns	50pf
T57	DEVSEL# Active delay from PCICLK	11.1	ns	50pf
T58	DEVSEL# Inactive delay from PCICLK	8.6	ns	35pf
T59	STOP# Active delay from PCICLK	11.8	ns	35pf
T89	STOP# Inactive delay from PCICLK	10.1	ns	50pf
T60	INIT Active delay from CPUCLK	8.4	ns	35pf
T61	INIT Inactive delay from CPUCLK	7.0	ns	35pf
T62	PCIRST# Active delay from CPUCLK	8.5	ns	50pf
T63	PCIRST# Inactive delay from CPUCLK	5.3	ns	50pf
T64	BCLK High	63.2	ns	120pf

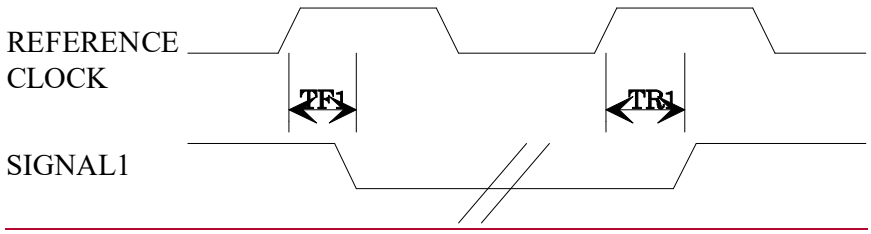
T65	BCLK Low	56.8	ns	120pf
T66	BALE active delay from BCLK	0	ns	120pf

T67	IORC#,IOWC#,MRDC#,MWTC# inactive delay from BCLK	4.5	ns	120pf
T68	M16# setup time	15	ns	
T69	M16 hold time	6	ns	
T70	IO16# setup time	19	ns	
T71	IO16# hold time	6	ns	
T72	16bit IORC#,IOWC# pulse width	1.5	BCLK	120pf
T73	8bit IORC#,IOWC# pulse width	4.5	BCLK	120pf
T74	16bit MRDC#,MWTC# pulse width	2	BCLK	120pf
T75	8 bit MRDC#,MWTC# pulse width	4.5	BCLK	120pf
T76	ROM MRDC#,MWTC# pulse width	2	BCLK	120pf
T77	SD DATA setup time to IORC#,MRDC# inactive	10	ns	120pf
T78	SD DATA hold time to IORC#,MRDC# inactive	3	ns	120pf
T79	SD valid data to IOWC#,MWTC# active	1.5	BCLK	120pf
T80	SD data hold time IOWC#,MWTC# inactive in write disassembly cycle	0.5	BCLK	120pf
T81	SD data hold time from IOWC#,MWTC# inactive in write cycle	172	ns	120pf
T82	SD valid to IOWC#,MWTC# active	160	ns	120pf
T83	SA,LA propagation delay from PCICLK in FRAME# address phase	51	ns	120pf
T84	SA0,SA1,SBHE# hold time from the negation of IORC#,IOWC#,MWTC#,MRDC#	0.5	BCLK	120pf
T85	CHRDY setup time to BCLK	15.2	ns	120pf
T86	CHRDY hold time to BCLK	14.8	ns	120pf
T87	ZWS# setup time to BCLK falling	10	ns	120pf
T88	ZWS# hold time to BCLK falling	20	ns	120pf
T89	DACK# active to IORC# active	0.5	DMACLK	35pf
T90	DACK# active to IOWC# active	1.5	DMACLK	35pf
T91	DACK# active hold from IORC# inactive	0.5	DMACLK	35pf
T92	DACK# active hold from IOWC# inactive	0.5	DMACLK	35pf
T93	AEN active to IORC# active	5.1	DMACLK	120pf
T94	AEN active to IOWC# active	6.1	DMACLK	120pf
T95	AEN inactive from IORC# inactive	3.5	DMACLK	120pf
T96	AEN inactive from IOWC# inactive	2.5	DMACLK	120pf
T97	BALE active to IORC# active	1.5	DMACLK	120pf
T98	BALE active to IOWC# active	2.5	DMACLK	120pf
T99	BALE inactive from IORC# inactive	1	DMACLK	120pf
T100	BALE inactive from IOWC# inactive	1	DMACLK	120pf

T101	LA,SA,SBHE# valid setup time to IORC#	1	DMACLK	120pf
T102	LA,SA,SBHE# valid setup time to IOWC#	2	DMACLK	120pf
T103	LA,SA,SBHE# valid hold time to IORC#	0.5	DMACLK	120pf
T104	LA,SA,SBHE# valid hold time to IOWC#	0.5	DMACLK	120pf

T105	IORC# pulse width	4	DMACLK	120pf
T106	IOWC# pulse width	2	DMACLK	120pf
T107	MRDC# pulse width	3	DMACLK	120pf
T108	MWTC# pulse width	3	DMACLK	120pf
T109	MWTC# inactive from IORC# inactive	1	ns	120pf
T110	IOWC# inactive from MRDC# inactive	1.3	ns	120pf
T111	read data valid from IORC# active	268.1	ns	120pf
T112	read data valid from IORC# inactive	121.0	ns	120pf
T113	write data valid setup to IOWC# inactive	575.2	ns	120pf
T114	write data valid hold from IOWC# inactive	16.1	ns	120pf
T115	TC active delay from IOWC# active	-3.2	ns	120pf
T116	TC active delay from IORC# active	235.7	ns	120pf
T117	TC active delay from IOWC# inactive	4.2	ns	120pf
T118	TC active delay from IORC# inactive	2.3	ns	120pf
T119	RFH# active setup to MRDC# active	2	BCLK	120pf
T120	RFH# active hold from MRDC# inactive	0.5	BCLK	120pf
T121	AEN active to RFH# active delay	7.6	ns	120pf
T122	SERR#,IOCHK# active to NMI output floating active	200	ns	
T123	INT output floating delay from IRQ active	100	ns	
T124	IRQ active pulse width	100	ns	
T125	IGNNE# active from IOWC# active for port F0H access	220	ns	
T126	IGNNE# inactive from FERR# inactive	150	ns	
T127	SPKR valid delay from 14Mhz	200	ns	
T128	RTCALE pulse width	536.5	ns	
T129	RTCALE active from IORC# active	7.5	ns	

9.2 AC Timing Diagram



TF1: Active delay for low active signals (Name with #)

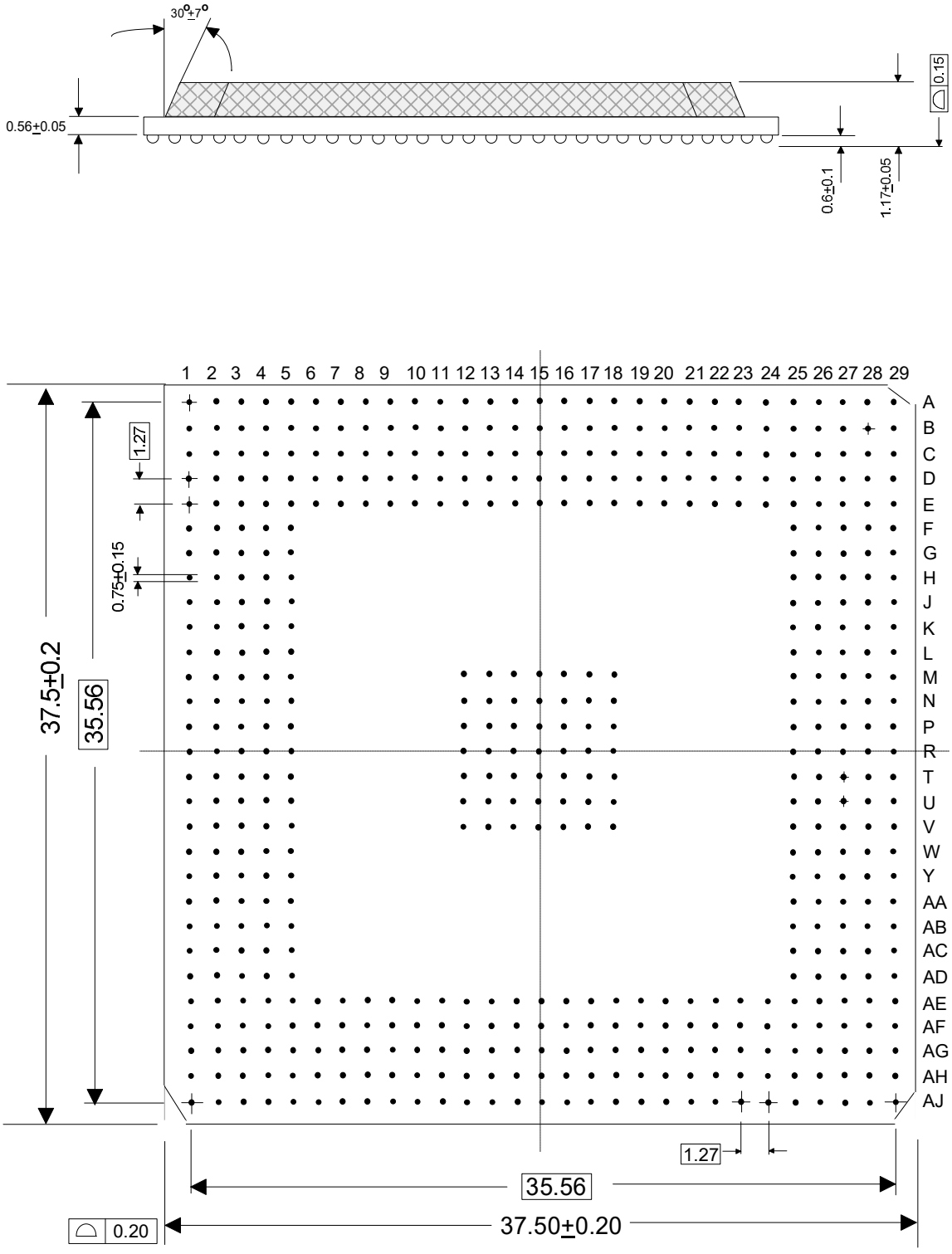
Inactive delay for high active signals (Name without #)

TR1: Inactive delay for low active signals (Name with #)

Active delay for high active signals (Name without #)

~~9.~~10. Mechanical Dimension (Top view)

(Unit: mm)


30°±7°
0.56±0.05
0.15
0.6±0.1
1.17±0.05
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29
A B C D E F G H J K L M N P R T U V W Y AA AB AC AD AE AF AG AH AJ
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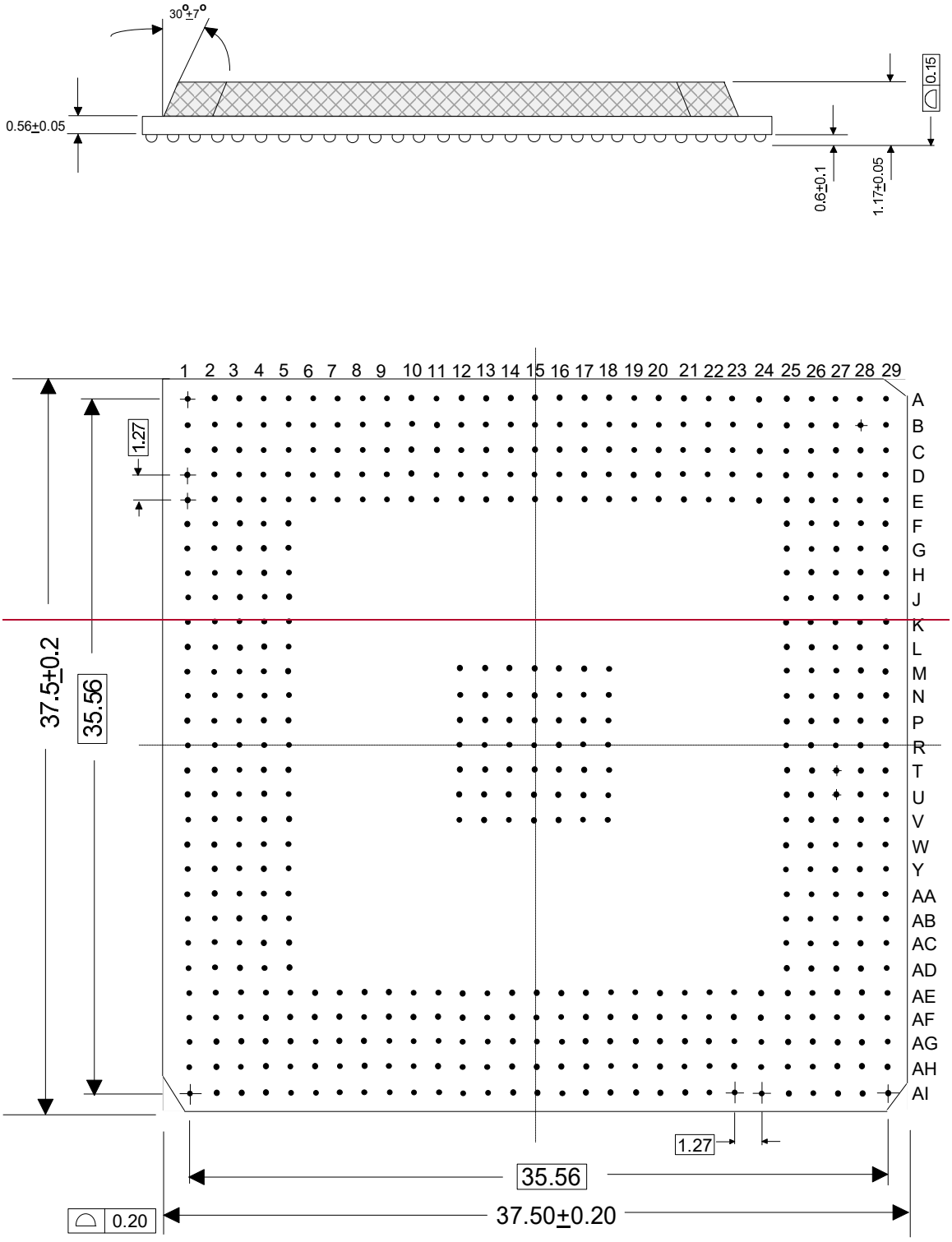
0.75±0.15
37.5±0.2
35.56
1.27
35.56
0.20
37.50±0.20


30°±7°
0.56±0.05
0.15
0.6±0.1
1.17±0.05
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29
A B C D E F G H J K L M N P R T U V W Y AA AB AC AD AE AF AG AH AI
1.27
37.5±0.2
35.56
1.27
35.56
0.20
37.50±0.20

~~10.~~11. COPYRIGHT NOTICE

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