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1. SiS5513 PCI System I/O (PSIO)

1.1. SiS5513 Overview

1.1.1. Features

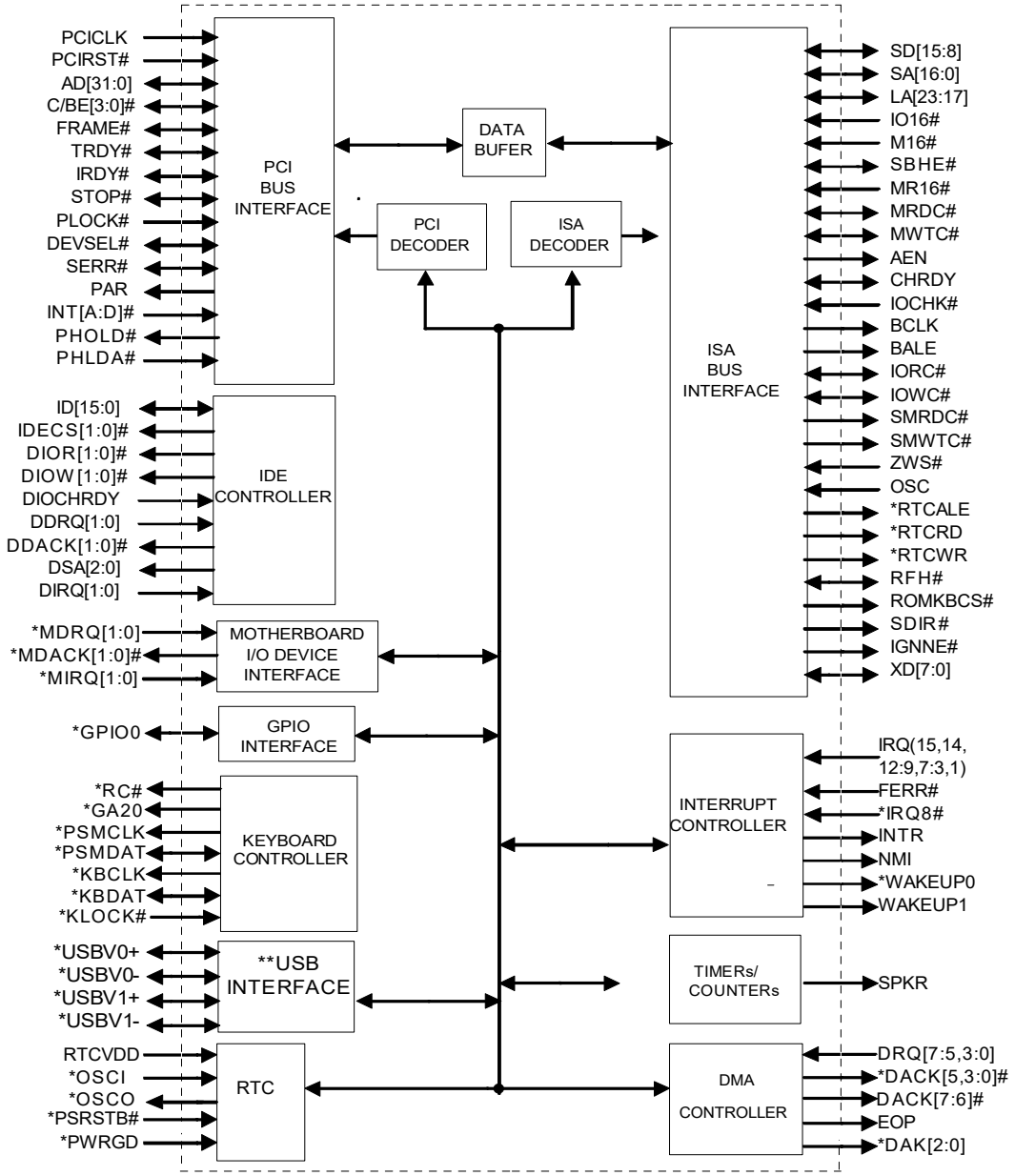
- **Integrated Bridge Between PCI Bus and ISA Bus**
  - Translates PCI Bus Cycles into ISA Bus Cycles
  - Translates ISA Master or DMA Cycles into PCI Bus Cycles
  - Provides a Dword Post Buffer for PCI to ISA Memory cycles
  - Two 32 bit Prefetch/Post Buffers Enhance the DMA and ISA Master Performance
  - Fully Compliant to PCI 2.1 (5513C)
- **Enhanced DMA Functions**
  - 8-, 16- bit DMA Data Transfer
  - ISA compatible, and Fast Type F DMA Cycles
  - Two 8237A Compatible DMA Controllers with Seven Independent Programmable Channels
  - Provides the Readability of the two 8237 Associated Registers
- **Built-in Two 8259A Interrupt Controllers**
  - 14 Independently Programmable Channels for Level- or Edge-triggered Interrupts
  - Provides the Readability of the two 8259A Associated Registers
- **Three Programmable 16-bit Counters compatible with 8254**
  - System Timer Interrupt
  - Generates Refresh Request
  - Speaker Tone Output
  - Provides the Readability of the 8254 Associated Registers
- **Built-in Keyboard Controller**
  - Hardwired Logic Provides Instant Response
  - Supports PS/2 Mouse
  - Support Hot Key "Sleep" Function
- **Built-in Real Time Clock(RTC) with 256B CMOS SRAM**
- **Fast PCI IDE Master/Slave Controller**
  - PCI Local Bus Specification V2.1 Compliance
  - Supports PCI Bus Mastering
  - Plug and Play Compatible
  - Supports Scatter and Gather
  - Supports Dual Mode Operation - Native Mode and Compatibility Mode
  - Supports IDE PIO Timing Mode 0, 1, 2 of ANSI ATA Specification
  - Supports Mode 3 and Mode 4 Timing Proposal on Enhanced IDE Specification
  - Supports Multiword DMA Mode 0, 1, 2
  - Separate IDE Bus
  - Two 8x32-bit FIFO for PCI Burst Read/Write Transfers.
- **Universal Serial Bus Controller(5513C)**
  - Host/Hub Controller
  - Two USB ports
- **On-Board Plug and Play Support**
  - Two Steerable DMA Channels
  - Two Steerable Interrupts

4.

- One Programmable Chip Select

- **Supports the Reroutibility of the four PCI Interrupts**
- **Supports Flash ROM**
- **208-Pin PQFP**
- **0.5 µm CMOS Technology**

1.1.2. Functional Block Diagram



* Multi-function pin

IRQ8#/OSCI	KBCLK/DACK5#	MDRQ0/USBV0+
RTCRD/PSRSTB#	KBDAT/DACK3#	MDRQ1/USBV0-
RTCALE/PWRGD	DAK2/DACK2#	MDACK1#/USBCLK
RTCWR/OSCO	DAK1/DACK1#	MIRQ0/USBV1+
GPIO0/KLOCK#	DAK0/DACK0#	MIRQ1/USBV1-
WAKEUP0/PSMDAT/MDRQ0	IRQ1/PSMCLK	DACK6#/MIRQ0/GA20
IRQ12/MDRQ0	DACK7#/MIRQ1/RC#	

** Built-in in future version.

Figure 1.1 SiS5513 Functional Block Diagram

1.2. Functional Description

The SiS5513 is a highly integrated PCI/ISA system I/O (PSIO) device that integrates all the necessary system control logic used in PCI/ISA specific applications.
The SiS5513 consists of
1. A PCI bridge that translates PCI cycles onto ISA bus
2. ISA master/DMA device cycles onto PCI bus
3. A seven-channel programmable DMA Controller
4. Sixteen-level programmable interrupt controller
5. A programmable timer with three counters
6. A built-in RTC with 256 bytes CMOS SRAM
7. A on-board Plug and Play port
8. A built-in PCI master/slave IDE interface.

In 5513B, the ISA compatible keyboard controller is also implemented with the enhancement of hot-key and PS/2 mouse support. Besides, two Dword buffers are employed to enhance the performance of the DMA/ISA master cycles. Also with the aid of the two Dword buffer, the fast type F DMA cycle is also supported.

The USB function will be supported in 5513C.

Since 5513 includes a PCI to ISA bridge and a PCI IDE, it naturally becomes a multi-function device. The PCI/ISA bridge is defined as a function 0 device while PCI IDE is a function 1 device. The following two examples describe how to write register XX in PCI to ISA bridge configuration space and register YY in PCI IDE configuration space.

Example 1:
```
MOV     EAX, 800010XXh
OUT     0CF8h, EAX
MOV     AL, data
OUT     0CFDh, AL
```

Example 2:
```
MOV     EAX, 800011YYh
OUT     0CF8h, EAX
MOV     AL, data
OUT     0CFDh, AL
```

1.2.1. PCI Bridge

The SiS5513 PCI bus interface provides the interface between PSIO and the PCI bus. It contains both PCI master and slave bridges to the PCI bus. When PHLDA# is asserted, the master bridge translates the ISA master, DMA cycles or PCI IDE Master cycles onto the PCI bus based on the decoding status from ISA address decoder. When PHLDA# is negated, the slave bridge accepts these cycles initiated on the PCI bus targeted to the PSIO internal registers or ISA bus , and then

4.
forwards the cycles to the ISA Bus Interface that further translates them onto the ISA Bus. The PCI address decoder provides the information on which the slave bridge depends to respond and process the cycle initiated by PCI Masters.

PCI Slave Bridge

As a PCI slave, PSIO responds to both I/O and memory transfers. PSIO always target-terminates after the first data phase for any bursting cycle.

SiS5513 always converts the single interrupt acknowledge cycle (from 5511) into two cycles that the internal 8259 pair can respond to.

The PSIO is assigned as the subtractive decoder in the Bus 0 of the SiS PCI/ISA system by accepting all accesses not positively decoded by some other agent. In reality, the PSIO only subtractively responds to low 64K I/O or low 16M memory accesses. PSIO also positively decodes I/O addresses for internal registers, and BIOS memory space by asserting DEVSEL# on the medium timing.

PCI Master Bridge

As long as PHLDA# is asserted, the PCI master bridge on behalf of DMA devices or ISA Masters starts to drive the AD bus, C/BE[3:0]# and PAR signals. When MRDC# or MWTC# is asserted, the PSIO will generate FRAME#, and IRDY# to PCI bus if the targeted memory is not on the ISA side. The valid address and command are driven during the address phase, and PAR is asserted one clock after that phase. PSIO always activated FRAME# for 2 PCLKs because it does not conduct any bursting cycle.

The ISA address decoder is used to determine the destination of ISA master or DMA devices. This decoder provides the following options as they are defined in configuration registers 48 to 4B.

a. Memory: 0-512K
b. Memory: 512K-640K
c. Memory: 640K-768K(video buffer)
d. Memory: 768K-896K in eight 16K sections(Expansion ROM)
e. Memory: 896K-960K(lower BIOS area)
f. Memory: 1M-XM-16M within which a hole can be opened. Access to the hole is not forwarded to PCI bus.
g. Memory:>16Mb automatically forwards to PCI.

1.2.2. ISA Bus Controller

The SiS5513 ISA Bus Interface accepts those cycles from PCI bus interface and then translates them onto the ISA bus. It also requests the PCI master bridge to generate PCI cycle on behalf of DMA or ISA master. The ISA bus interface thus contains a standard ISA Bus Controller and a Data Buffering logic. IBC provides all the ISA control, such as ISA command generation, I/O recovery control, wait-state insertion, and data buffer steering. The PCI to/from ISA address and data bus bufferings

4.
are also all integrated in SiS5513. The SiS5513 can directly support six ISA slots without external data or address buffering.

Standard ISA bus refresh is requested by Counter 1, and then performed via the IBC. IBC generates the pertinent command and refreshes address to the ISA bus. Since the ISA refresh is transparent to the PCI bus and the DMA cycle, an arbiter is employed to resolve the possible conflicts among PCI cycles, refresh cycles, and DMA cycles.

1.2.3. DMA Controller

The SiS5513 contains a seven-channel DMA controller. The channel 0 to 3 is for 8-bit DMA devices while channel 5 to 7 is for 16-bit devices. The channels can also be programmed for any of the four transfer modes, which include single, demand, block, and cascade. Except in cascade mode, each of the three active transfer modes can perform three different types of transfers, which include read, write, and verify. The address generation circuitry in SiS5513 can only support 24-bit address for DMA devices.

Besides, there is another function: Type F DMA. The type F DMA is composed by two parts, one is the prefetch\postwrite buffer from the ISA bus to the PCI bus and the type F DMA timing controller. We will explain these two parts separately.

Prefetch/postwrite buffer

This prefetch/postwrite buffer is used for the memory cycles of the DMA controllers and the ISA bus masters and is of two double word width. Those memory cycles that are forwarded to the PCI bus are processed by this buffer. The two-double word is further divided into two parts, each is of one double word width. These two parts act as a ring buffer and each can communicate with the PCI bus and the ISA bus independently.

The buffer is triggered by the memory commands on the ISA bus regardless of the sources of the commands. When a memory read command comes, the buffer begins to prefatch a double word from the PCI bus and then disassembles the data onto the ISA bus. At the same time, the buffer begins to prefatch anther double word from the PCI bus. Whenever one of the two double word has disassembles all its data to the ISA bus, then the buffer will prefatch another double word from the PCI bus, at the same time the buffer switch the data of the other double word to the ISA bus.

When one of the following conditions occurs, the data in the buffer is all invalidated; the address goes beyond the double word range, the following command is memory write cycle, and the bus ownership of the ISA bus changes.

When a memory write command comes, the buffer latches the data and the address, and at the same time, sets the byte enable. That is to say, the buffer performs byte\word merge during the memory write cycles. Whenever the data has filled a double word then the buffer begins to flush the double word to the PCI bus and at the same time, switches the other double of the buffer to latch the data of the following memory write cycle from the ISA bus.

4.
When one of the following conditions occurs, the data in the buffer must be flushed onto the PCI bus; the buffer is full, the address comparison fails, the following command is a memory read command, and the bus ownership of the ISA bus changes.

Type F DMA Timing Controller

The type F DMA timing controller controls the timings of the DMA commands, the DMA wait states and the DMA clock. This controller must cooperate with the prefatch/postwrite buffer described above. When the DACK of the DMA channel that is programmed to perform type F DMA transfers is active, the timing controller first switch the DMA clock from the half of the system clock to the system clock. During the transfer, the timing controller will disable the default wait state of the DMA controller, only active all the I/O commands and shorten the pulse width of the I/O commands to one system clock. The wait states are controlled by the prefetch\postwrite buffer.

1.2.4. Interrupt Controller

The SiS5513 provides an ISA compatible interrupt controller that incorporates the functionality of two 82C59 interrupt controllers. The two controllers are cascaded so that 14 external and two internal interrupts are supported. The master interrupt controller provides IRQ<7:0> and the slave one provides IRQ<15:8>. The two internal interrupt are used for internal functions only and are not available externally. IRQ2 is used to cascade the two controllers together and IRQ0 is used as a system timer interrupt and is tied to interval Counter 0. The remaining 14 interrupt lines are available for external system interrupts.

Table 1-1

Priority	Label	Controller	Typical Interrupt Source
1	IRQ0	1	Timer/Counter 0 Out
2	IRQ1	1	Keyboard
3-10	IRQ2	1	Interrupt from Controller 2
3	IRQ8#	2	Real Time Clock
4	IRQ9	2	Expansion bus pin B04
5	IRQ10	2	Expansion bus pin D03
6	IRQ11	2	Expansion bus pin D04
7	IRQ12	2	Expansion bus pin D05
8	IRQ13	2	Coprocessor Error Ferr#
9	IRQ14	2	Fixed Disk Drive Controller Expansion bus pin D07
10	IRQ15	2	Expansion bus pin D06
11	IRQ3	1	Serial port 2, Expansion Bus B25
12	IRQ4	1	Serial port 1, Expansion Bus B24
13	IRQ5	1	Parallel Port 2, Expansion Bus B23
14	IRQ6	1	Diskette Controller, Expansion Bus B22
15	IRQ7	1	Parallel Port, Expansion Bus B21

In addition to the ISA features, the ability to do interrupt sharing is included. Two registers(ECLR) located at 4D0h and 4D1h are defined to allow edge or level sense selection to be made on an

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individual channel by channel basis instead of on a complete bank of channels. Note that the default of IRQ0, IRQ1, IRQ2, IRQ8# and IRQ13 is edge sensitive, and can not be programmed. Also, each PCI Interrupt(INTx#) can be programmed independently to route to one of the eleven ISA compatible interrupts(IRQ<7:3>, IRQ<15:14>, and IRQ<12:9>) through configuration registers 41h to 44h.

1.2.5. Timer/Counter

The SiS5513 contains 3 channel counter/timer that is equivalent to those found in the 82C54 programmable interval timer. The counters use a division of 14.31818MHz OSC input as the clock source. The outputs of the timers are directed to key system functions. Counter 0 is connected to the interrupt controller IRQ0 and provides a system timer interrupt for a time-of-day, diskette time-out, or the other system timing function. Counter 1 generates a refresh-request signal and Counter 2 generates the tone for the speaker.

1.2.6. Built-in RTC

The 5513 incorporates a real-time clock and system configuration memory. The RTC combines:

- A complete time-of-day clock with alarm
- 100 year calendar
- Programmable periodic interrupt
- 14 bytes of clock and control registers and 242 bytes of lower power general purpose SRAM

The method of accessing the upper 128 bytes of CMOS SRAM is to write 50h to I/O port 22h and then setting bit 3 of I/O port 23h.

1.2.7. Built-in PCI Master/Slave IDE

Design of the built-in PCI IDE follows the PCI Local Bus Specification and PCI IDE Controller Specification.

Both primary and secondary channel may be programmed as Native mode or Compatibility mode via the Class Code Field in the controller's Configuration Space register.

In Compatibility mode, the interrupt requests for channel 0 and channel 1 are rerouted to IRQ 14 and IRQ 15 of the built-in Interrupt Controller.

Following tables illustrate the accessing methods to the I/O ports in compatibility mode:

Table 1-2 Primary Channel

			READ		WRITE	
PORT	**IDECS1#**	**IDECS0#**	**DIOR0#**	**DIOR1#**	**DIOW0#**	**DIOW1#**
1F0	1	0	0	1	0	1
1F1	1	0	0	1	0	1
1F2	1	0	0	1	0	1
1F3	1	0	0	1	0	1
1F4	1	0	0	1	0	1
1F5	1	0	0	1	0	1
1F6	1	0	0	1	0	1
1F7	1	0	0	1	0	1
3F6	0	1	0	1	0	1

Table 1-3 Secondary Channel

			READ		WRITE	
PORT	**IDECS1#**	**IDECS0#**	**DIOR0#**	**DIOR1#**	**DIOW0#**	**DIOW1#**
170	1	0	1	0	1	0
171	1	0	1	0	1	0
172	1	0	1	0	1	0
173	1	0	1	0	1	0
174	1	0	1	0	1	0
175	1	0	1	0	1	0
176	1	0	1	0	1	0
177	1	0	1	0	1	0
376	0	1	1	0	1	0

In Native mode, the interrupt requests of both channels share the same PCI interrupt pin. The interrupt pin may be rerouted to any one of eleven ISA compatible interrupts (IRQ[15:14], IRQ[12:9], and IRQ[7:3]) via programming 5513 Configuration Register 63h.

Meanwhile, accessing of the I/O ports are via the addresses programmed in Base Address Registers 10h, 14h, 18h and 1Ch in IDE configuration space.

While serving as a bus master device, the IDE controller may transfer data between IDE devices and main memory directly. By performing the DMA transfer, IDE offloads the CPU and improves system performance. Bus master DMA programming is according to the information specification "Programming Interface for Bus Master IDE Controller".

Master PIO mode, which means that PCI site is running in Master mode, while the IDE site is running in PIO mode, is also supported here. Master PIO mode for Primary Channel and Secondary Channel may be enabled via IDE configuration register 4A, bit 4 and bit 3.

4.
Under master mode, IDE controller shares the same request (PHOLD#) and acknowledge (PHLDA#) signals with PSIO via a high performance hidden arbitration scheme.

The built-in IDE controller contains PCI configuration header and registers to meet PCI specifications. The internal PCI IDE supports PCI type 0 configuration cycles of configuration mechanism #1.

Proper cycle timing is generated to fit PCI Bus speed and different modes of IDE drive. All cycle timing can be controlled by software programming.

As a slave device, IDE decodes and interprets PCI cycles and generate signals to start and terminate IDE cycles. This block responds only to cycles that belong to IDE I/O address space. It supports both 16-bit and 32-bit I/O data transfer at address 1F0/170. All other IDE registers read or write operations are 8-bit only.

There are four 8×32 bits FIFOs, which support post write and pre-fetch operations, in the internal PCI IDE. Prefetch and post write operations for each channel may be activated via Register 4B in IDE Configuration Space. The two FIFOs may operate independently.

The posted write operations can enhance the transfer rate of the PCI Bus interface to IDE interface write operation by decoupling the wait-states effect from the slower IDE side to the faster PCI Bus side.

The prefetch operations can eliminate the idle cycle of the PCI Bus side to improve read operation.

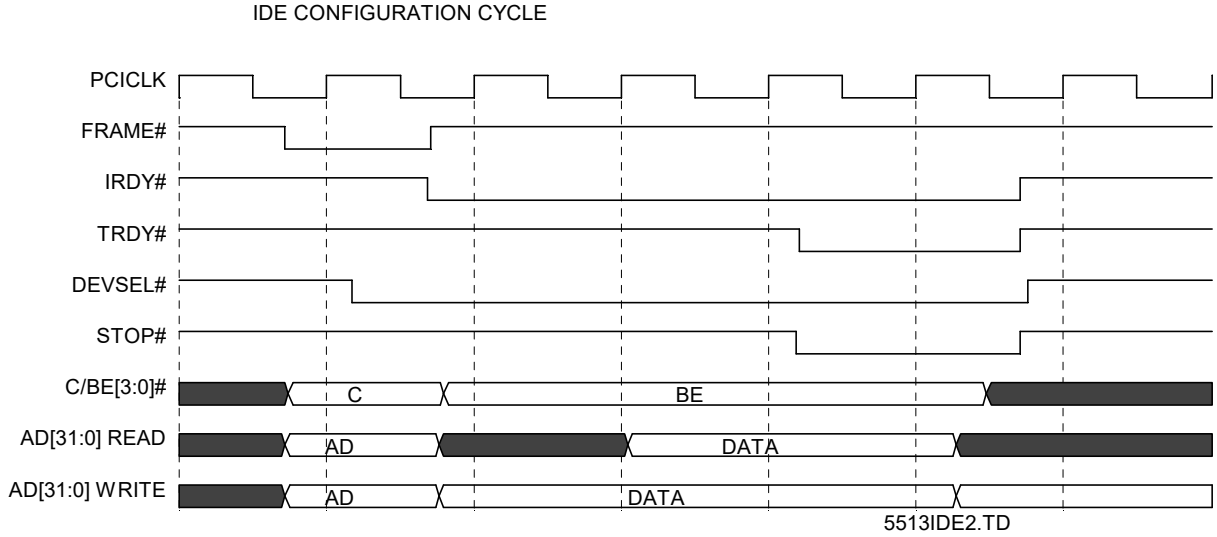

Figure 1.2

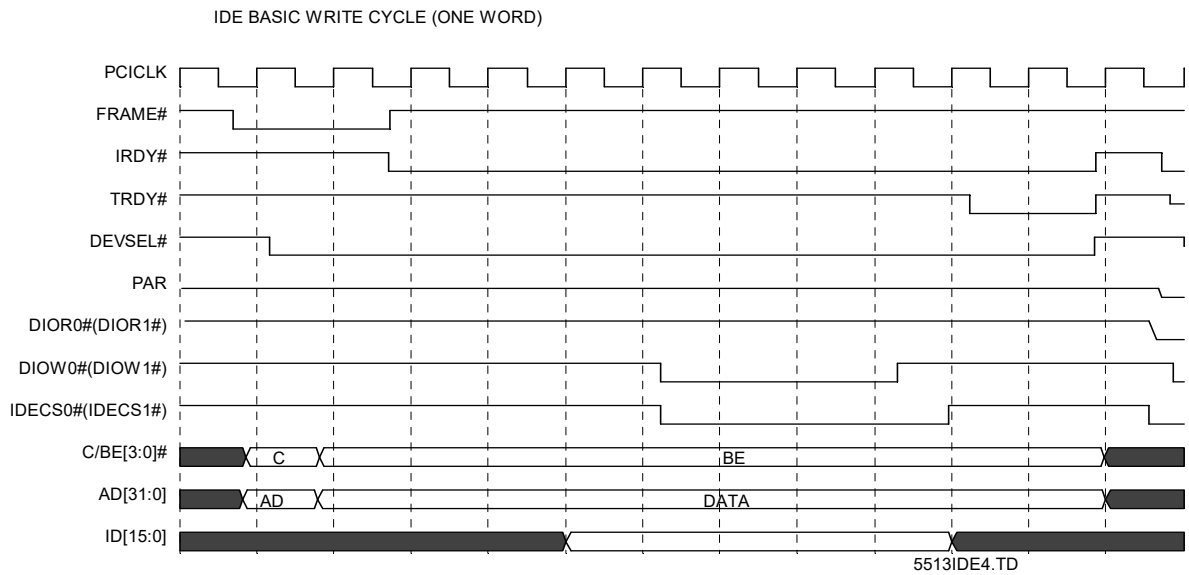

Figure 1.3

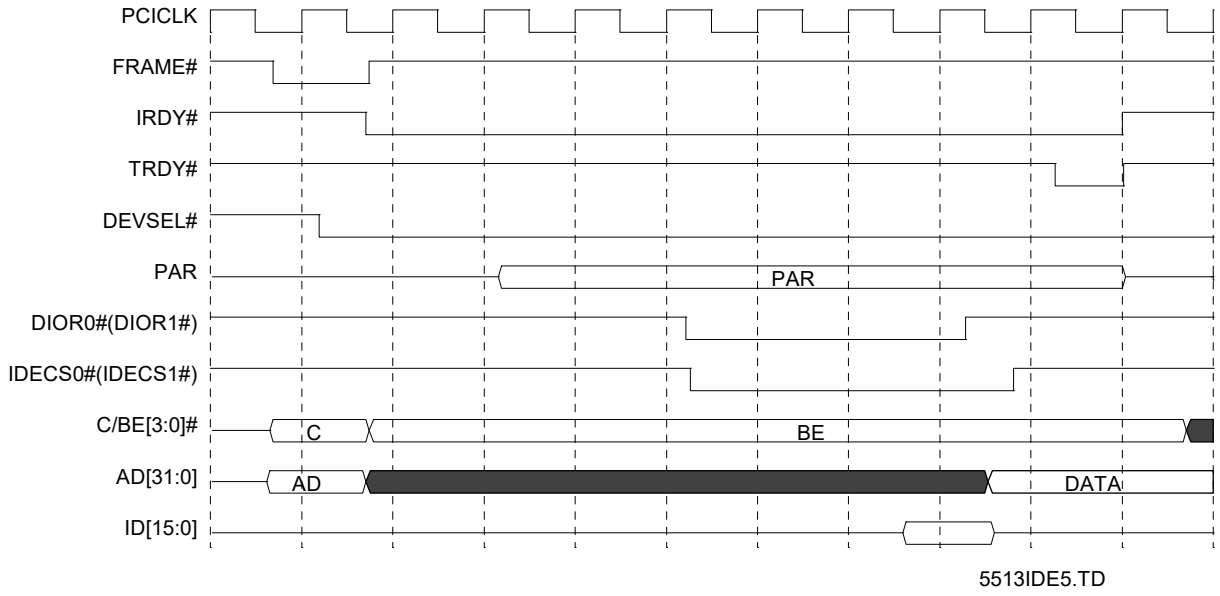

Figure 1.4

4.

IDE POST WRITE CYCLE (16-BIT I/O)

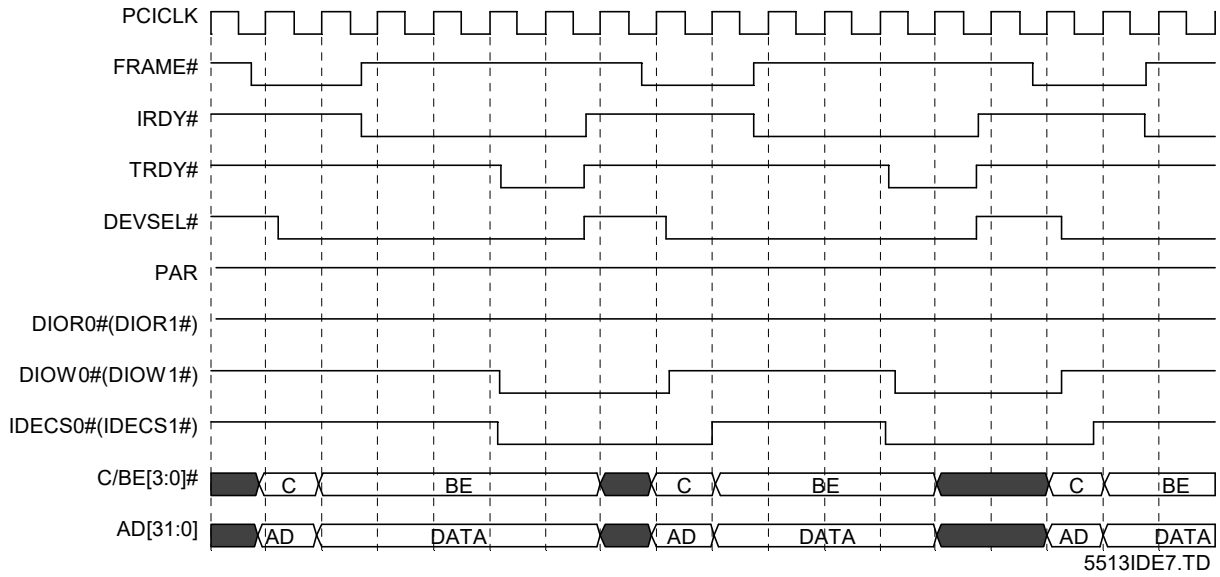

Figure 1.5

IDE PREFETCH CYCLE (32-BIT I/O)

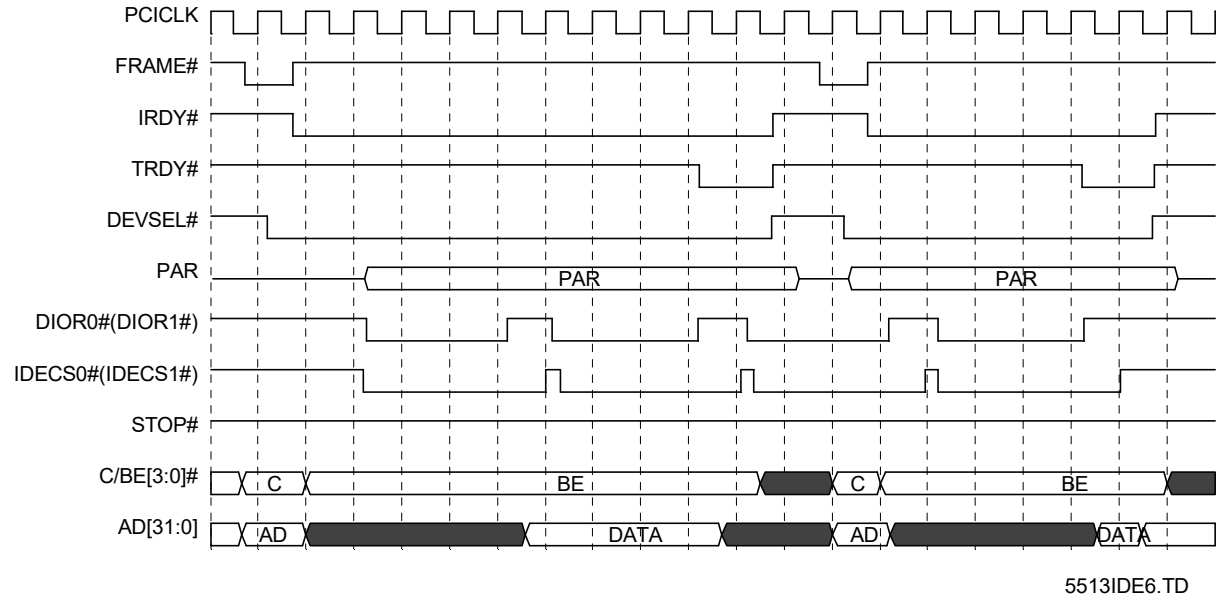

Figure 1.6

4.

PCI MASTER READ CYCLE (BYTE COUNTER = 06H, RECV = 1T, ACT = 3T)

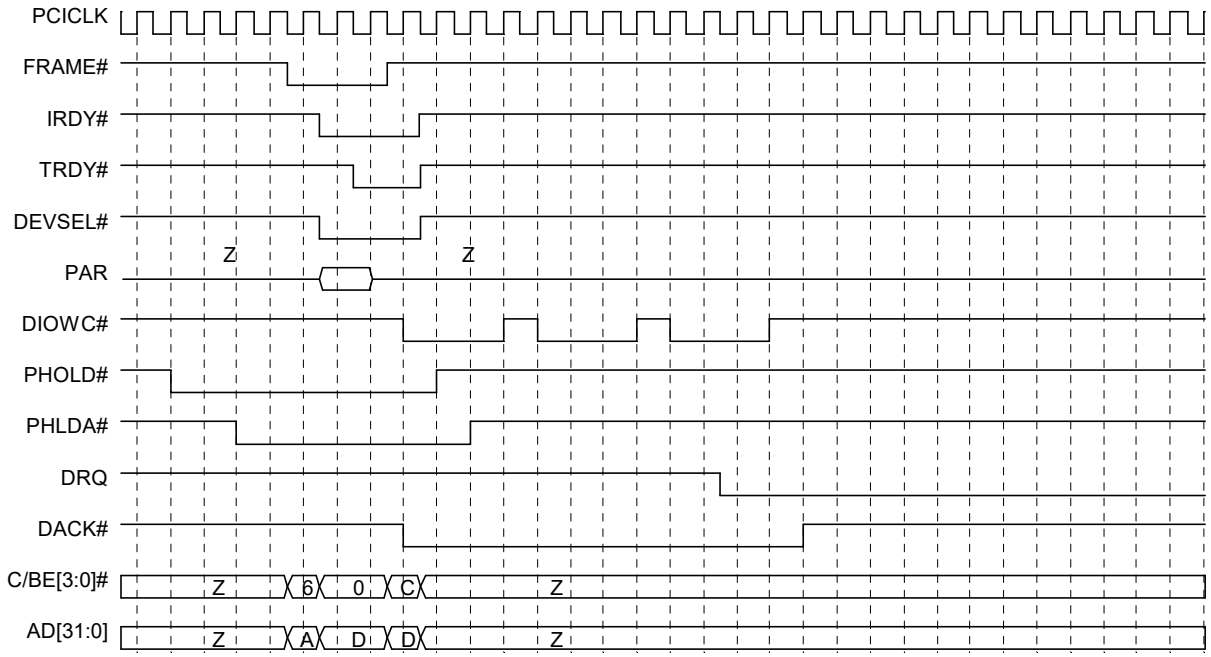

Figure 1.7

PCI MASTER WRITE CYCLE (BYTE COUNTER = 06H, RECV = 3T, ACT = 1T)

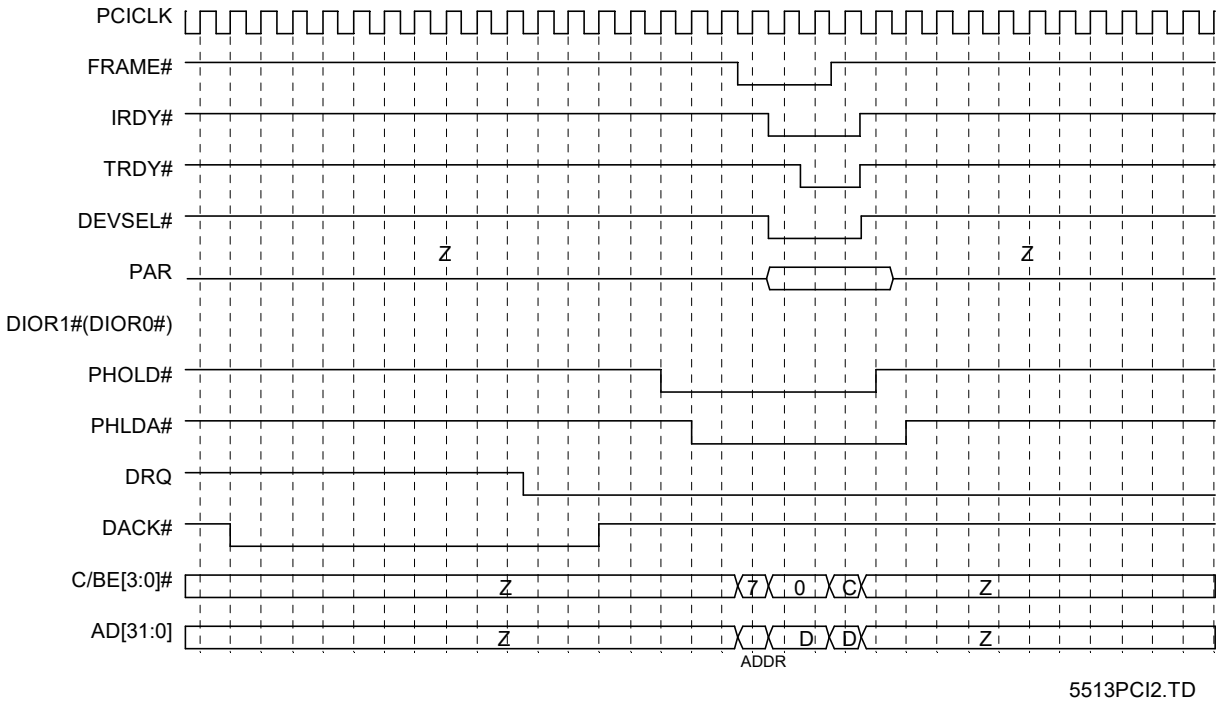

Figure 1.8

1.2.8. Built-in Keyboard Controller

The built-in KBC uses hardwired methodology instead of software implementation as the traditional 8042 keyboard BIOS. In this way, keyboard controller can have instant response to all the commands. It also has Fast Gate-20 and Fast Reset Features. Besides, the built-in KBC has a power control feature. After the [Ctrl]+[Alt]+[Backspace] hot keys are pressed, the system will enter the power saving mode. Moreover, the built-in KBC supports the industrial standard PS/2 mouse optionally.

Status Register

The status register is an 8 bits read only register located at I/O address hex 64. It has information about the state of the keyboard controller and interface. It may be read at any time.

Bit 7 **Parity Error**

0 : Odd Parity (No Parity Error)

1 : Even Parity (Parity Error)

Bit 6 **Time-out Error**

0 : No Transmission Time-out Error

1 : Transmission Time-out Error

Bit 5 **Auxiliary Output Buffer Full**

0 : Keyboard Data

1 : Mouse Data

Bit 4 **Inhibit Switch**

0 : Keyboard is Inhibited

1 : Keyboard is not Inhibited

Bit 3 **Command/Data**

0 : Data Byte. Writing to I/O 60h

1 : Command Byte. Writing to I/O 64h

Bit 2 **System Flag**

This bit may be set to 0 or 1 by writing to system flag bit in the keyboard controller's command byte. It is set to 0 after a power on reset

Bit 1 **Input Buffer Full**

0 : Input Buffer Empty

1 : Input Buffer Full. Data has been written into the buffer but the controller has not read the data

4.

Bit 0 **Output Buffer Full**

0 : Output Buffer Empty

1 : Output Buffer Full. The controller has placed data into its output buffer but the system has not yet read data

Input/Output Buffer

Input Buffer

The input buffer is an 8 bits write only register located at I/O address hex 60 or 64. Writing to address hex 60 sets a flag, that indicates a data write; writing to address hex 64 sets a flag, indicating a command write. Data written to I/O address hex 60 is sent to the keyboard, unless the keyboard controller is expecting a data byte following a controller command. Data should be written to the controller's input buffer only if the input buffer's full bit in the status register equal 0. The next command are valid keyboard controller commands.

Output Buffer

The output buffer is an 8 bits read only register at I/O address hex 60. The keyboard controller uses the output buffer to send scan codes received from the keyboard, and data bytes requested by command to the system. The output buffer should be read only when output buffer's full bit in the status register set to 1.

Commands (I/O Address 64H)

Write I/O Address 64h that is Keyboard BIOS Command:

Command	Keyboard Mode	Keyboard PS/2 Mode
00-1F	Read Internal RAM -- The controller sends value of RAM to output buffer.	
20	Read Keyboard Controller's Command Byte -- The controller sends its current Command byte to its output buffer.	
21-3F	Read Internal RAM -- The controller sends value of RAM to output buffer.	
40-5F	Write Internal RAM -- The next byte of data written to I/O 60h is placed into Internal RAM.	
60	Write Keyboard Controller's Command Byte -- The next byte of data written to I/O 60h is placed in the controller's command byte.	
	Bit — *Bit Definitions*	
	0 — Enable Keyboard Output-Buffer-Full Interrupt. Generates an interrupt when it places keyboard data into its output buffer.	
	1 — In Keyboard Mode: Reserved to 0. In Keyboard PS/2 Mode: 1 -- Enable Mouse-Buffer-Full Interrupt. Generates an interrupt when it places mouse data into its output buffer.	
	2 — 1 -- The controller generates an System Flag. The value written to this bit is placed in the system flat bit of the controller's status register.	
	3 — 1 - Disable Keyboard Lock Switch “KBLOCK”.	
	4 — 1 - Disable Keyboard. Disable the Keyboard interface by driving the 'clock' line low. Data is not sent or received.	
	5 — 1 -- Disable Mouse. Disable the mouse interface by driving the 'clock' line low. Data is not sent or received.	
	6 — 1 -- IBM Personal Computer Compatibility Mode. Convert the scan codes received from keyboard to IBM PC. This includes converting a two-byte sequence to the one-byte IBM Personal Computer format.	
	7 — 0 -- Reserved.	
61-7F	Write Internal RAM -- The next byte of data written to I/O 60h is placed into Internal RAM.	
A0	Read Internal ROM -- The controller sends value to its output buffer that end with a "0".	
A1	Read Keyboard Controller's Version - The version code result will be placed to its output buffer.	
A4	Reset Internal Register B to 0.	Test Password Installed -- The controller sends value to its output buffer: FAh -- Password installed F1h -- Password not installed
A5	Reset Internal Register B to 0.	Load Password -- The next byte of data written to I/O 60h is placed into password stream (max 16 byte) that ends with "0". The password is store in scan code format.
A6	Read Internal Register B -- The controller sends value to its output buffer.	Enable Password Security -- The keyboard data does not sends to output buffer until the keyboard data are match the password stream..
A7	Set Internal Register C to 0.	Disable Mouse Device -- This disable the mouse interface by driving the mouse clock line low.
A8	Set Internal Register C to 1.	Enable Mouse Device -- This enable the mouse interface by driving the mouse clock line float.
A9	Read Internal Register C -- The controller sends value to its output buffer.	Mouse Device Interface Test -- Test the controller's mouse clock and data line and place the result to output buffer as follows : 00 -- No error detected. 01 -- The 'Mouse Clock' line is stuck low. 02 -- The 'Mouse Clock' line is stuck high. 03 -- The 'Mouse Data' line is stuck low. 04 -- The 'Mouse Data' line is stuck high.
AA	Self-Test - This commands the controller to perform internal diagnostic tests. A hex 55 is placed in the output buffer if no errors are detected.	

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AB	Keyboard Interface Test -- This commands the controller to test the keyboard clock and data line. The test result is placed in the output buffer as follows : 00 -- No error detected. 01 -- The 'Keyboard Clock' line is stuck low. 02 -- The 'Keyboard Clock' line is stuck high. 03 -- The 'Keyboard Data' line is stuck low. 04 -- The 'Keyboard Data' line is stuck high.	
AD	Disable Keyboard Feature -- This command sets bit 4 of the controller's command byte. This disable the keyboard interface by driving the clock line low. Data will not be sent or received.	
AE	Enable Keyboard Interface -- This command clears bit 4 of command byte which release the keyboard interface	
B0	Set P10 to 0	Not Valid
B1	Set P11 to 0	Not Valid
B8	Set P10 to 1 (Default)	Not Valid
B9	Set P11 to 1 (Default)	Not Valid
C0	Read Input Port -- This command the controller to read its input port and place the data in its output buffer. This command should be used only if the output buffer is empty.	
C1	Set Port P17 to 0 & KBLOCK disable	Set Port P17 to 0 & KBLOCK disable
C2	Not Valid	Place Bit 7-4 of Input Port to status register
C3	Not Valid	Place Bit 3-0 of Input Port to status register
C7	Set Port P17 to 1	Set Prot P17 to 1
CA	Read Internal Register D -- The Internal Register will be placed into its output buffer.	
CB	Write Internal Register D -- The next byte of data written to I/O 60h is placed in the controller's Register D.	
D0	Read Output Port -- This command causes the controller to read its output port and place data in its output buffer. This command should be issued only if the output buffer is empty.	
D1	Write Output Port -- The next byte of data written to I/O 60h is placed in the controller's output port.	
D2	Not Valid	Write Keyboard Output Buffer - The next byte of data written to I/O 60h is placed in output buffer as it receive from keyboard.
D3	Not Valid	Write Mouse Output Buffer - The next byte of data written to I/O 60h is placed in output buffer as it receive from mouse.
D4	Not Valid	Write Mouse Device - The next byte of data written to I/O 60h is transmitted mouse device.
D6	Enable P17(KBLOCK) Keyboard Lock Switch (Default)	
D7	Disable P17(KBLOCK) Keyboard Lock Switch, P17 define to I/O by C1 & C7 command	
F0-FF	Pulse Output Port -- Bits 0 through 3 of controller's output port may be pulsed low for approximately 6us. Bits 0 through 3 of this command indicate which bits are to be pulsed. A 0 indicates that the bit should be pulsed, and a 1 indicate the bit should not be modified.	

1.2.9. Timing Diagram

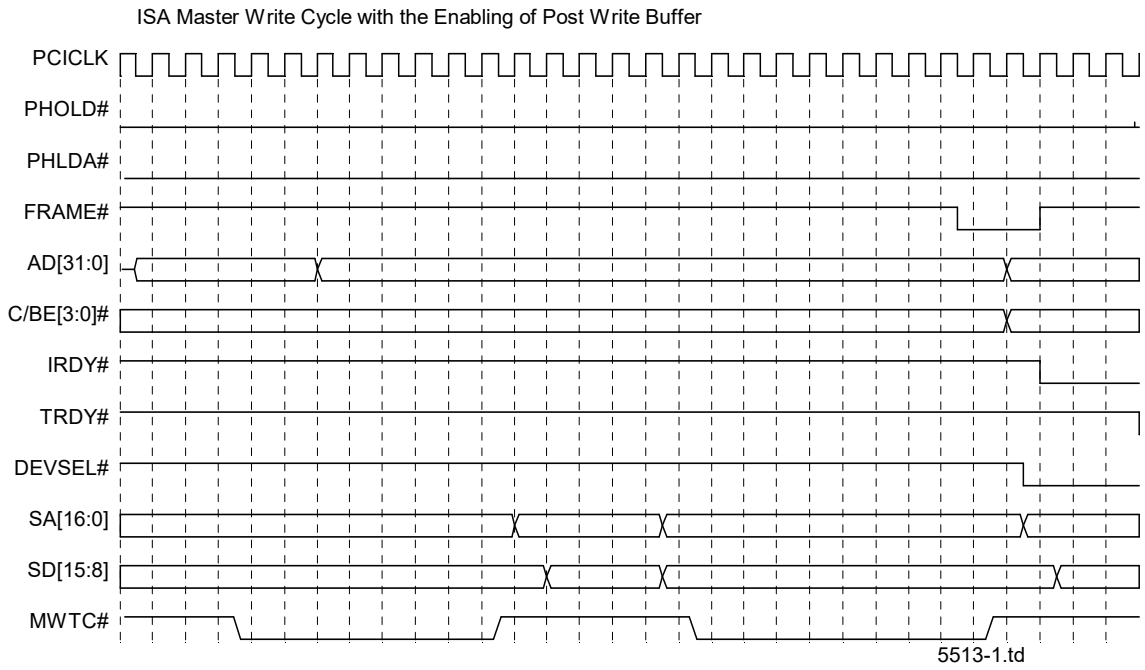


Figure 1.9 ISA Master Write Cycle with the Enabling of Post Write Buffer

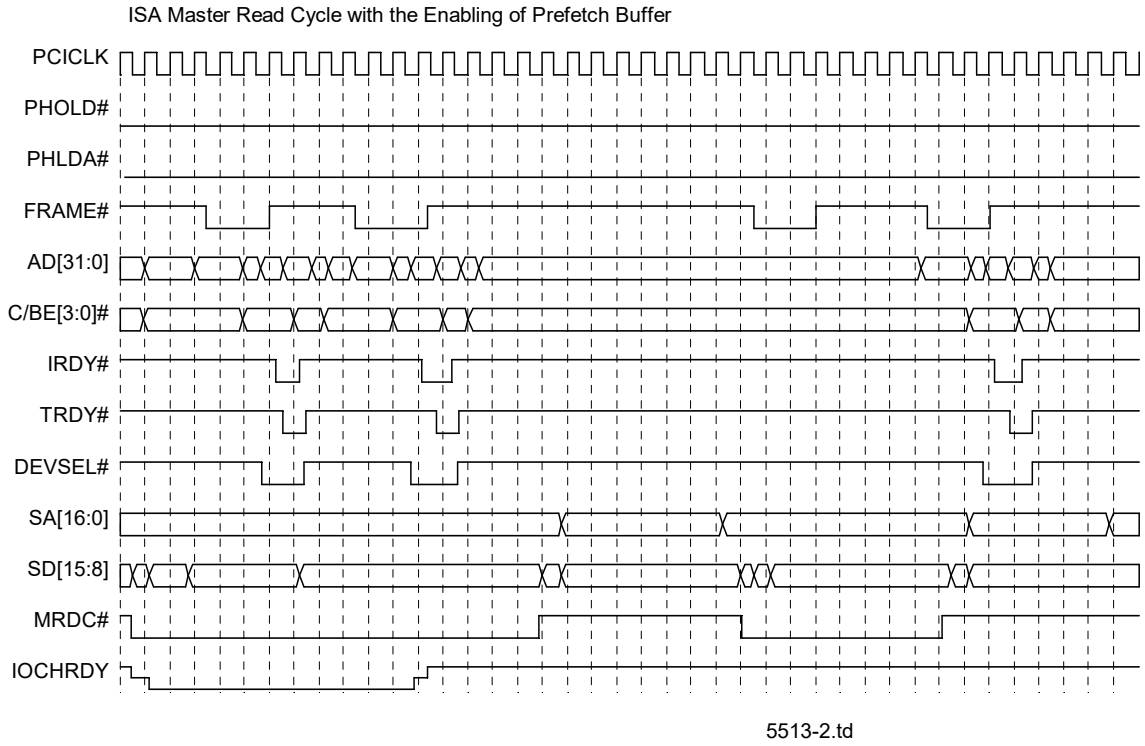


Figure 1.10 ISA Master Read Cycle with the Enabling of Prefetch Buffer

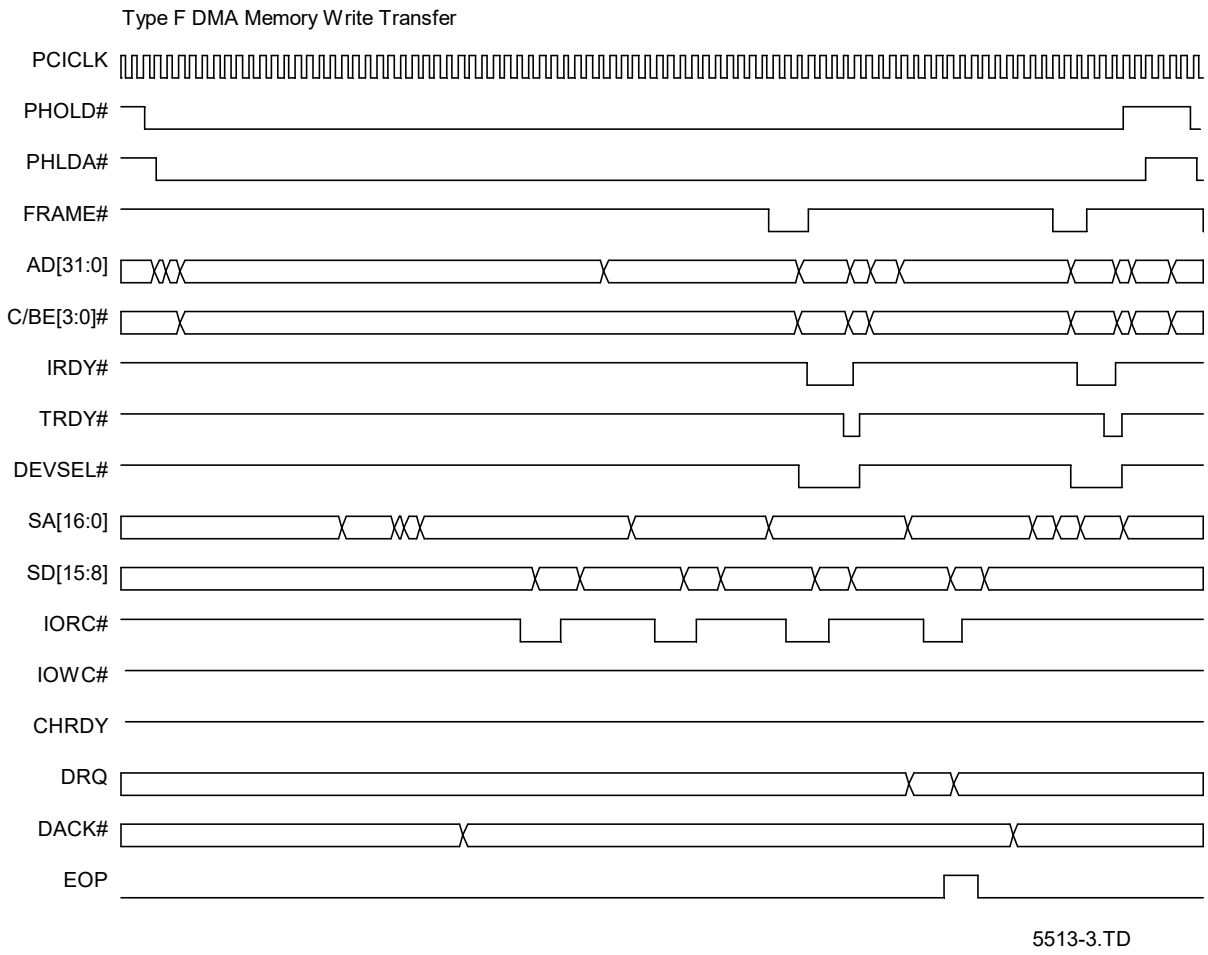


Figure 1.11 Type F DMA Memory Write Transfer

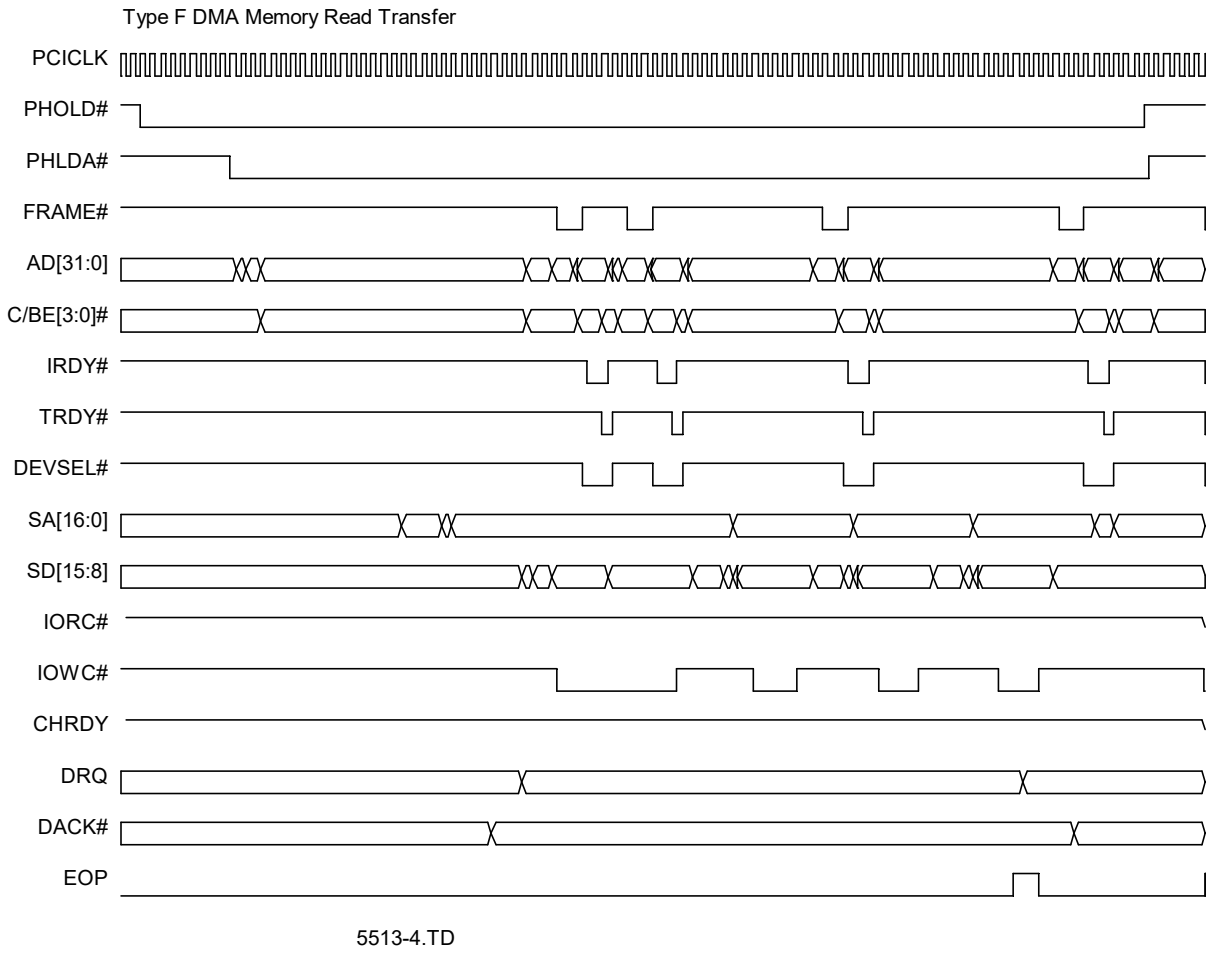


Figure 1.12 Type F DMA Memory Read Transfer

1.3. Register Description

1.3.1. PCI Configuration Register (PCI to ISA Bridge)

Registers 00h, 01h Vendor ID

Bits 15:0 = 1039h (Read Only)

Registers 02h, 03h Device ID

Bits 15:0 = 0008h (Read Only)

Registers 04h, 05h Command = 07h

Bits 15:4 Reserved. Read as 0's

Bit 3 Monitor Special Cycle Enable = 0

Bit 2 Behave as Bus Master Enable = 1

Bit 1 Respond to Memory Space Accesses = 1

Bit 0 Respond to I/O Space Accesses = 1

Registers 06h, 07h Status

Bits 15:14 Reserved. Read as 0's

Bit 13 Received Master-Abort

When the 5513 generates a master-abort, this bit is set to a 1. This bit is cleared to 0 by writing a 1 to this bit.

Bit 12 Received Target-Abort

When the 5513 receives a target-abort, this bit is set to a 1. Software clears this bit to 0 by writing a 1 to this bit location.

Bit 11 Reserved. Read as a 0

Bits 10:9 DEVSEL# Timing

The 5513 always generates DEVSEL# with medium timing, these two bits are always set to 01.

Bits 8:0 Reserved. Read as 0's.

Register 08h Revision ID

4.

Bits 7:0 = 00h (Read Only)

Register 0B~09h Class Code

Bits 23:0 060100h (Read Only)

Register 0Eh Header Type

Bits 7:0 80h (Read Only)

Register 40h BIOS Control Register

Bit 7 Reserved. Read as a 0.

Bit 6 Reserved. Read as a 0.

Bit 5

When ISA MASTER retries, Arbiter deasserts PHLDA#. This bit defaults to 0.

Bit 4 PCI Posted Write Buffer Enable

The default value is 0 (disabled).

Bits [3:0] determine how the 5513 responds to F segment, E segment, and extended segment (FFF80000-FFFDFFFF) accesses. 5513 will positively respond to extended segment access when bit 0 is set. Bit 1, combining with bits [3:2], enables 5513 to respond to E segment access.

Bit 3 Positive Decode of Upper 64K BYTE BIOS Enable.

Bit 2 BIOS Subtractive Decode Enable.

Bits [3:2]	F segment		E segment		Comment
	+	-	+	-	
00			√ *		5513 positively responds to E segment access.
01		√			5513 subtractively responds to F segment access.
10	√		√ *		5513 positively responds to E and F segment access.
11	√				5513 positively responds to F segment access.

*: enabled if bit 1 is set.

Bit 1 Lower BIOS Enable.

Bit 0 Extended BIOS Enable. (FFF80000~FFFDFFFF)

Register 41h INTA# Remapping Control Register

Bit 7 Remapping Control

When enabled, INTA#, is remapped to the PC compatible interrupt signal specified in IRQ remapping table. This bit is set to 1 after reset.

0: Enable

1: Disable

Bits 6:4 Reserved. Read as 0's.

Bits 3:0 IRQx Remapping table.

Bits	IRQx	Bits	IRQx	Bits	IRQx	Bits	IRQx
0000	reserved	0101	IRQ5	1010	IRQ10	1111	IRQ15
0001	reserved	0110	IRQ6	1011	IRQ11		
0010	reserved	0111	IRQ7	1100	IRQ12		
0011	IRQ3	1000	reserved	1101	reserved		
0100	IRQ4	1001	IRQ9	1110	IRQ14		

Register 42h INTB# Remapping Control Register

Bit 7 Remapping Control

Bits 6:4 Reserved. Read as 0's.

Bits 3:0 IRQ Remapping table.

Register 43h INTC# Remapping Control Register

Bit 7 Remapping Control

Bits 6:4 Reserved. Read as 0's.

Bits 3:0 IRQ Remapping table.

Register 44h INTD# Remapping Control Register

Bit 7 Remapping Control

Bits 6:4 Reserved. Read as 0's.

Bits 3:0 IRQ Remapping table.

NOTE: The difference INT[A:D]# can be remapped to the same IRQ signal, but this IRQ signal should be set to level sensitive.

Register 48h ISA Master/DMA Memory Cycle Control Register 1

The ISA master or DMA memory access cycles will be forwarded to PCI bus when the address fall within the programmable region defined by bits[7:4]. The base

address of the programmable region is 1MByte, and the top addresses is programmed in 1MByte increments from 1MByte to 16MByte. All memory cycles will be forwarded to PCI bus besides the cycle fall within memory hole defined in register 4Ah and 4Bh.

Bits 7:4

Bit 7	Bit 6	Bit 5	Bit 4	Top of Memory
0	0	0	0	1 MByte
0	0	0	1	2 MByte
0	0	1	0	3 MByte
0	0	1	1	4 MByte
0	1	0	0	5 MByte
0	1	0	1	6 MByte
0	1	1	0	7 MByte
0	1	1	1	8 MByte
1	0	0	0	9 MByte
1	0	0	1	10 MByte
1	0	1	0	11 MByte
1	0	1	1	12 MByte
1	1	0	0	13 MByte
1	1	0	1	14 MByte
1	1	1	0	15 MByte
1	1	1	1	16 MByte

ISA master and DMA memory cycles to the following memory regions will be forwarded to PCI bus if they are enabled.

Bit 3 **E0000h-EFFFFh Memory Region**

0: Disable

1: Enable, the cycle is forwarded to PCI bus.

Bit 2 **A0000h-BFFFFh memory Region**

0: Disable

1: Enable, the cycle is forwarded to PCI bus.

Bit 1 **80000h-9FFFFh Memory Region**

0: Disable

1: Enable

The cycle is forwarded to PCI bus.

Bit 0 **00000h-7FFFFh Memory Region**

0: Disable

1: Enable

The cycle is forwarded to PCI bus.

Register 49h ISA Master/DMA Memory Cycle Control Register 2

ISA master and DMA memory cycles to the following memory regions will be forwarded to PCI bus if they are enabled.

Bit 7 **DC000h-DFFFFh Memory region**

0: Disable

1: Enable

Bit 6 **D8000h-DBFFFh Memory Region**

0: Disable

1: Enable

Bit 5 **D4000h-D7FFFh Memory Region**

0: Disable

1: Enable

Bit 4 **D0000h-D3FFFh Memory Region**

0: Disable

1: Enable

Bit 3 **CC000h-CFFFFh Memory Region**

0: Disable

1: Enable

Bit 2 **C8000h-CBFFFh Memory Region**

0: Disable

1: Enable

Bit 1 **C4000h-C7FFFh Memory Region**

0: Disable

1: Enable

Bit 0 **C0000h-C3FFFh Memory Region**

0: Disable

1: Enable

Register 4Ah ISA Master/DMA Memory Cycle Control Register 3

Register 4Ah and register 4Bh are used to define the ISA address hole. The ISA address hole is located between 1MByte and 16MByte, and sized in 64KByte increments. ISA master and DMA memory cycles fall within this hole will not be forwarded to PCI bus. Register 4Ah and 4Bh are used to define the bottom and top address of the hole respectively. The hole is located between top and bottom address, and the bottom and top address must be at or above 1MByte. If bottom address is greater than top address, the ISA address hole is disabled.

Bits 7:0 A23~A16

Register 4Bh ISA Master/DMA Memory Cycle Control Register 4

This register is used to define the top address of the ISA Address hole.

Bits 7:0 A23~A16

Registers 4Ch-4Fh

Bits 7:0 ICW1 to ICW4 of the built-in interrupt controller (master) can be read from 4Ch to 4Fh.

Registers 50h-53h

Bits 7:0 ICW1 to ICW4 of the built-in interrupt controller (slave) can be read from 50h to 53h.

Registers 54h-55h

Bits 7:0 OCW2 to OCW3 of the built-in interrupt controller (master) can be read from 54h to 55h.

Registers 56h-57h

Bits 7:0 OCW2 to OCW3 of the built-in interrupt controller (slave) can be read from 56h to 57h.

Register 58h

Bits 7:0 Low byte of the initial count number of Counter 0 in the built-in CTC can be read from 58h.

Register 59h

Bits 7:0 High byte of the initial count number of Counter 0 in the built-in CTC can be read from 59h.

Register 5Ah

Bits 7:0 Low byte of the initial count number of Counter 1 in the built-in CTC can be read from 5Ah.

Register 5Bh

Bits 7:0 High byte of the initial count number of Counter 1 in the built-in CTC can be read from 5Bh.

Register 5Ch

Bits 7:0 Low byte of the initial count number of Counter 2 in the built-in CTC can be read from 5Ch.

Register 5Dh

Bits 7:0 High byte of the initial count number of Counter 2 in the built-in CTC can be read from 5Dh.

Register 5Eh

Bits 7:0 Control word (43h) of the built-in CTC can be read from 5Eh.

Register 5Fh

Bits 7:0 Indicates the status whether the LSB or MSB is read or written when Read/Write word function has been processed for the corresponding counter.

Register 60h MIRQ0 Remapping Control Register

This register controls the remapping of MIRQ0 to the PC/AT compatible IRQ inputs of the interrupt controller. MIRQ0 can be remapped to any one of the 11 interrupts.

Bit 7 MIRQ0 Remapping Control

When enabled, MIRQ0 is remapped to the PC compatible interrupt signal specified in IRQ remapping table.

0: Enable

1: Disable

Bit 6 MIRQ0/IRQx Sharing Control

0: Enable

1: Disable

The interrupt specified by IRQ remapping table is masked when this bit is disabled and MIRQ0 remapping is enabled.

When sharing and remapping are both enabled, MIRQ0 will be remapped to the IRQ channel programmed via Register 60h.

While MIRQ0 is enabled, the interrupt channel for ISA will automatically be masked. MIRQ0, MIRQ1 and INTA#, INTB#, INTC#, INTD# may be asserted at the same time.

Bits 5:4 Reserved. Read as zero.

Bits 3:0 Interrupt Remapping Table

This field is used to define the MIRQ0 remapping to one of the eleven PC compatible interrupts.

bits [3:0]	IRQ remapped	bits [3:0]	IRQ remapped
0000	Reserved	1000	Reserved
0001	Reserved	1001	IRQ9
0010	Reserved	1010	IRQ10
0011	IRQ3	1011	IRQ11
0100	IRQ4	1100	IRQ12
0101	IRQ5	1101	Reserved
0110	IRQ6	1110	IRQ14
0111	IRQ7	1111	IRQ15

Register 61h MIRQ1 Remapping Control Register

bit 7 MIRQ1 Remapping Control

0 : Enable

1 : Disable

bit 6 MIRQ1/IRQx Sharing Control

0: Enable

1: Disable

When sharing and remapping are both enabled, MIRQ0 will be remapped to the IRQ channel programmed via Register 61h.

While MIRQ1 is enabled, the interrupt channel for ISA will automatically be masked. MIRQ0, MIRQ1 and INTA#, INTB#, INTC#, INTD# may be asserted at the same time.

bits 5:4 Reserved. Read as zero.

bits 3:0 Interrupt Remapping Table

bits [3:0]	IRQ remapped	bits [3:0]	IRQ remapped
0000	Reserved	1000	Reserved

0001	Reserved	1001	IRQ9
0010	Reserved	1010	IRQ10
0011	IRQ3	1011	IRQ11
0100	IRQ4	1100	IRQ12
0101	IRQ5	1101	Reserved
0110	IRQ6	1110	IRQ14
0111	IRQ7	1111	IRQ15

Operation Rules for Rerouting Circuits:

1. If any one IDE channel is in compatibility mode, the IRQ channel mapped to that IDE channel should be assigned as the IDE IRQ channel. Nobody can share it.

   e.g.: IDE channel 0 is in compatibility mode, while channel 1 is native.

   IRQ 14 should be always used by IDE channel 0. Nobody can share it. IDE channel 1 should use DIRQ to reroute it's interrupt requests.

2. If channel n is rerouted by any one of MIRQ[1:0]: (Edge & Level trigger can be both applied)

   CASE 1: Share disable:
   Except for MIRQ1 or 0, nobody can share the channel.
   MIRQ0 and MIRQ1 can't be rerouted to the same channel.

   CASE 2: Share enable:
   Including MIRQ0, MIRQ1, INTA#, INTB#, INTC#, INTD#, and DIRQ may be rerouted to the same channel.

   Here, ISA IRQn will be automatically masked.

3. If both MIRQ[1:0] are disabled:

   PCI INTA#, INTB#, INTC#, and INTD# can be rerouted to the same channel. But ISA IRQn will be automatically masked.

4. None of MIRQ[1:0], PCI interrupt pins, DIRQ are rerouted to channel n:
   ISA IRQn can be enabled.

Register 62h - On-board Device DMA Control Register

This register is used to control the remapping of MDRQ[1:0] and MDACK[1:0]# to the DREQ and DACK# signals of the 8237 DMA controller.

Bit 7 **MDRQ1/MDACK1# Remapping Control**

0: Disable

1: Enable

Bits 6:4 **DMA Channel Remapping Table of MDRQ1/MDACK1#**

Bits[6:4]	DMA Channel

000	Channel 0
001	Channel 1
010	Channel 2
011	Channel 3
100	Disable
101	Channel 5
110	Channel 6
111	Channel 7

If a MDRQ/MDACK# pair is programmed to one of DMA channels, the corresponding DREQ/DACK# pins are masked for that channel.

Bit 3 MDRQ0/MDAK0# Remapping Control

0: Disable

1: Enable

When this bit set to 1, the MDRQ0/MDACK0# are mapped to the compatible ISA channel specified in bits[6:4]. When this bit set to 0, the ISA DREQ/DACK# pair is used for that channel.

Bits 2:0 DMA Channel Remapping Table of MDRQ0/MDACK0#

The following table is used to select the DMA channel for MDRQ0/MDACK0#

Bits[2:0]	**DMA Channel**
000	Channel 0
001	Channel 1
010	Channel 2
011	Channel 3
100	Disable
101	Channel 5
110	Channel 6
111	Channel 7

Register 63h - IDEIRQ Remapping Control Register

Bit 7 IDEIRQ Remapping Control

1: Disable

0: Enable

Bit 6:4 Reserved. Read as zero.

Bits 3:0 Interrupt Remapping Table

Bits [3:0]	**remapped IRQ**	**Bits [3:0]**	**remapped IRQ**
0000	Reserved	1000	Reserved
0001	Reserved	1001	IRQ9

0010	Reserved	1010	IRQ10
0011	IRQ3	1011	IRQ11
0100	IRQ4	1100	IRQ12
0101	IRQ5	1101	Reserved
0110	IRQ6	1110	IRQ14
0111	IRQ7	1111	IRQ15

Register 64h - GPIO0 Control Register

Bit 7 **GPIO0 Mode Control**

0: Output mode

1: Input mode (default)

Bit 6 **GPIO0 Input Active Level Control**

0: Active low

1: Active high

Bit 5 **GPIO0 Input Bounce-Free Control**

0: Disable

1: Enable

When this bit set to 1, the GPIO0 input goes through a de-bounce circuit.

Bit 4 **Reserved. Read as zero.**

Bits 3:0 **De-bounce Count for GPIO0 De-Bounce Circuit.**

The minimum value is 2. The timer-expire interval is calculated by the following equation: The timer-expire interval=(Count-1)x0.6s

Register 65h

Bit 7 **Enable bit of the arbiter between SIO and built-in IDE Master. While disabled, IDE Master will not work.**

0: Disabled

1: Enable (default)

Bits 6:0 **Reserved (Read as 0)**

Registers 66h, 67h - GPIO0 Output Mode Control Register

A 16-bit I/O space base address defined in bit[15:2] is used to cause GPIO0 to assert "active low" signal for subtractively decoded I/O cycles generated by PCI masters that fall in the range specified by this register. This register is available only when GPIO0 is set to output mode.

4.

Bits 15:2 A[15:2] of GPIO0 I/O Space Base Address

Bits 1:0 GPIO0 I/O Space Address Mask

00: Mask A1, A0

01: Mask A2, A1, A0

10: Disable GPIO0 output mode function

11: Mask A3, A2, A1, A0

Registers 68h, 69h - Reserved

Register 6Ah - GPIO Status Register

Bits 7:5 **Reserved. Read as zero.**

Bit 4 **Arbiter Operating Mode**

0: Fixed priority mode.

1: Rotating priority mode.

Bit 3 **Reserved (This bit should be programmed as 0.)**

Bit 2 **Built-in RTC Status (Read Only)**

0: Not used

1: Used

When built-in RTC is used, this bit is set to 1.

Bit 1 **Reserved**

Bit 0 **GPIO0 Status**

This bit is set when GPIO0 is active and should be cleared at the end of SMI handler. This bit is meaningful only when register 65h bit 7 set to 1.

Register 70h

Attribute Read/Write
Default 00h

Bit 7 **Enable/Disable the prefatch/postwrite of the ISA master and DMA controller.**

0 : Disable

1: Enable

Bit 6 **Enable/Disable the DEVDET logic**

0: Disable

1: Enable

When the P5513 cooperates with P596, this bit must be set to 1 because the PMU of P596 must use the DEVDET interface to get the information of IRQs and NMI from P5513. When P5513 cooperates with P5511, this bit must be set to default value.

Bit 5 **Reserved**

Bit 4 **Enable/disable keyboard lock.**

0: Disable

1: Enable

When this bit is set to 0, the keyboard lock is disabled and the pin 10 can be used as GPIO0. When this bit is set to 1, pin 10 is used as the keyboard lock.

Bit 3 **Hardware trap status for keyboard controller.**

0 : the external keyboard controller is used

1 : the internal keyboard controller is used.

This bit is read only, any write to this bit can not alter the status.

Bit 2 **Software Disable PS/2 Mode of the Keyboard Controller**

0: No Effect

1: Force the Keyboard Controller to disable the PS/2 mode regardless of the result of the hardware trap.

This bit is used to disable the PS/2 mode when the hardware trap enables the PS/2 mode.

Bit 1 **Reserved**

Bit 0 **This bit must be written with 0.**

Register 71h

Attribute: Read/Write
Default: 00h

This register is to set which DMA channel can perform type F DMA transfers. A 1 on any bit sets the corresponding DMA channel to perform type F DMA transfers.

Bit 7 **DMA channel 7**

Bit 6 **DMA channel 6**

Bit 5 **DMA channel 5**

Bit 4 **Reserved**

Bit 3 **DMA channel 3**

Bit 2 **DMA channel 2**

Bit 1 **DMA channel 1**

Bit 0 **DMA channel 0**

Register 72h

4.

Attribute R/W
Default 80h

Bit 7 USB Function Enable.

1: Enable(default)

0: Disable

Bit 6 USB port 0 Enable.

When enabled, the MDRQ[1:0] is used as USBV0+, USBV0- respectively. In 5513C, the two pins are tri-state bi-directional, and is in the input direction upon power up. In this situation, the 5513C still provides a motherboard DMA request/acknowledge pair by programming IRQ12, or WAKEUP0 as the MDRQ0 signal.

0: Disabled

1: Enabled

Bit 5 USB port 1 Enable.

When enabled, the MIRQ[1:0] is used as USBV1+, USBV1- respectively. In 5513C, the two pins are tri-state bi-directional, and is in the input direction upon power up. In this situation, the mother board interrupt request function may still be reserved by moving the MIRQ[1:0] to pin 200, and 199 respectively.

0: Disabled

1: Enabled

Bit 4 Reserved.

Bit 3 WAKEUP0 Direction Control.

Bit 2 DACK[7:6]# Direction Control. This bit controls the direction of DACK[7:6]#.

0: Input

1: Output

Bit 1 DAK Encoder Enable.

When set, the DACK[7:0]# is encoded to DAK[2:0]#, no matter that the internal KBC is used. This gives the availability of DACK[7:3]# to be programmed to other function at the expense of requiring the external F138 to decode DAK[2:0]# to DACK[7:0]#.

Bit 0 MIRQ[1:0] Pin Reassignment.

When set, Pin 199, and 200 are used as MIRQ[1:0] signals. This selection is available on 5511C, and would be valid only when the DAK Encoder is enabled, or the built-in KBC is employed.

Register 73h

Bits 7:3 Reserved

Bit 2 IRQ12/MDRQ0 Select:

When set, the IRQ12 serves as MDRQ0.

Bit 1 PSMDAT/MDRQ0 Select:

When set, the WAKEUP0 serves as the MDRQ0 function if the PS/2 mouse is disabled. If the PS/2 mouse is enabled, the WAKEUP0 functions as PSMDAT no matter that the bit is set or clear.

Bit 0 This bit must be programmed with 0.

1.3.2. Non-Configuration Registers

DMA Registers

These registers can be accessed from PCI bus.

Address	Attribute	Register Name
0000h	R/W	DMA1 CH0 Base and Current Address Register
0001h	R/W	DMA1 CH0 Base and Current Count Register
0002h	R/W	DMA1 CH1 Base and Current Address Register
0003h	R/W	DMA1 CH1 Base and Current Count Register
0004h	R/W	DMA1 CH2 Base and Current Address Register
0005h	R/W	DMA1 CH2 Base and Current Count Register
0006h	R/W	DMA1 CH3 Base and Current Address Register
0007h	R/W	DMA1 CH3 Base and Current Count Register
0008h	R/W	DMA1 Status(r) Command(w) Register
0009h	WO	DMA1 Request Register
000Ah	WO	DMA1 Write Single Mask Bit
000Bh	WO	DMA1 Mode Register
000Ch	WO	DMA1 Clear Byte Pointer
000Dh	WO	DMA1 Master Clear
000Eh	WO	DMA1 Clear Mask Register
000Fh	R/W	DMA1 Write All Mask Bits(w) Mask Status Register(r)
00C0h	R/W	DMA2 CH0 Base and Current Address Register
00C2h	R/W	DMA2 CH0 Base and Current Count Register
00C4h	R/W	DMA2 CH1 Base and Current Address Register
00C6h	R/W	DMA2 CH1 Base and Current Count Register
00C8h	R/W	DMA2 CH2 Base and Current Address Register
00CAh	R/W	DMA2 CH2 Base and Current Count Register
00CCh	R/W	DMA2 CH3 Base and Current Address Register
00CEh	R/W	DMA2 CH3 Base and Current Count Register
00D0h	R/W	DMA2 Status(r) Command(w) Register
00D2h	WO	DMA2 Request Register

4.

00D4h	WO	DMA2 Write Single Mask Bit Register
00D6h	WO	DMA2 Mode Register
00D8h	WO	DMA2 Clear Byte Pointer
00DAh	WO	DMA2 Master Clear
00DCh	WO	DMA2 Clear Mask Register
00DEh	R/W	DMA2 Write All Mask Bits(w) Mask Status Register(r)

These registers can be accessed from PCI bus or ISA bus.

Address	Attribute	Register Name
0080h	R/W	Reserved
0081h	R/W	DMA Channel 2 Low Page Register
0082h	R/W	DMA Channel 3 Low Page Register
0083h	R/W	DMA Channel 1 Low Page Register
0084h	R/W	Reserved
0085h	R/W	Reserved
0086h	R/W	Reserved
0087h	R/W	DMA Channel 0 Low Page Register
0088h	R/W	Reserved
0089h	R/W	DMA Channel 6 Low Page Register
008Ah	R/W	DMA Channel 7 Low Page Register
008Bh	R/W	DMA Channel 5 Low Page Register
008Ch	R/W	Reserved
008Dh	R/W	Reserved
008Eh	R/W	Reserved
008Fh	R/W	Refresh Low Page Register

Interrupt Controller Registers (These registers can be accessed from PCI bus or ISA bus.)

Address	Attribute	Register Name
0020h	R/W	INT 1 Base Address Register
0021h	R/W	INT 1 Mask Register
00A0h	R/W	INT 2 Base Address Register
00A1h	R/W	INT 2 Mask Register

Timer Registers (These registers can be accessed from PCI bus or ISA bus.)

Address	Attribute	Register Name
0040h	R/W	Interval Timer 1 - Counter 0
0041h	R/W	Interval Timer 1 - Counter 1
0042h	R/W	Interval Timer 1 - Counter 2
0043h	WO	Interval Timer 1 - Control Word Register

Other Registers (These registers can be accessed from PCI bus or ISA bus.)

Address	Attribute	Register Name
0061h	R/W	NMI Status Register
0070h	WO	CMOS RAM Address and NMI Mask Register

4.

00F0h	WO	Coprocessor Error Register

Register 4D0h IRQ Edge/Level Control Register 1

Bit 7 IRQ7

0: Edge sensitive

1: Level sensitive

Bit 6 IRQ6

0: Edge sensitive

1: Level sensitive

Bit 5 IRQ5

0: Edge sensitive

1: Level sensitive

Bit 4 IRQ4

0: Edge sensitive

1: Level sensitive

Bit 3 IRQ3

0: Edge sensitive

1: Level sensitive

Bit 2 IRQ2

This bit must be set to 0. Read as 0.

Bit 1 IRQ1

This bit must be set to 0. Read as 0.

Bit 0 IRQ0

This bit must be set to 0. Read as 0.

After reset this register is set to 00h.

Register 4D1h IRQ Edge/Level Control Register 2

Bit 7 IRQ15

0: Edge sensitive

1: Level sensitive

Bit 6 IRQ14

0: Edge sensitive

1: Level sensitive

Bit 5 **IRQ13**

This bit must be set to 0. Read as 0.

Bit 4 **IRQ12**

0: Edge sensitive

1: Level sensitive

Bit 3 **IRQ11**

0: Edge sensitive

1: Level sensitive

Bit 2 **IRQ10**

0: Edge sensitive

1: Level sensitive

Bit 1 **IRQ9**

0: Edge sensitive

1: Level sensitive

Bit 0 **IRQ8**

This bit must be set to 0. Read as zero.

After reset this register is set to 00h.

1.3.3. ISA Internal Register

ISA internal registers are accessed through an address/data registers pair. Address register located at port 22h is written with the index of ISA internal register. Then ISA internal register content can be read or written through the data register at port 23h. The port 22h can be read to get the last written-in value.

Register 50h

Bits 7:6 **Bus clock selection**

00: 7.159MHz

01: PCICLK/4

10: PCICLK/3

Bit 5 **Flash EPROM Control bit 0 (Please refer to Register 80h bit 2 for details.)**

Bit 4 **Reserved**

Bit 3 **Access Upper 128 Bytes CMOS SRAM**

0: Disable

1: Enable

Bit 2 **Flash EPROM Control bit 1**

Previous implementation on flash EPROM support limits that EPROM is flashed upon power on till bit 5 of register 50h is set to 1. The new added feature will allow EPROM to be flashed anytime. Bit 2 of the register 50h is added and the setting of both bit 2 and bit 5 will now control the EPROM flash operation.

Register 50h bit 5	Register 50h bit 2	Operation
0	0	EPROM can be flashed
1	0	EPROM can't be flashed again
X	1	EPROM can be flashed whenever bit 5 is 0

Bit 1 **Reserved**

Bit 0 **ISA Slew Rate Control**

The default value of the following ISA signals is 8mA(min), including SA[16-0], LA[23-17], SBHE#, MRDC#, MWTC#, SMRDC#, SMWTC#, IORC#, and IOWC#. Besides, Bit 0 of ISA configuration register 80h is used to program the currents of the above signals to 12mA(min) when it is set to 1.

Register 51h

Bits 7:6 **16-bit I/O cycle command recovery time**

00 : 5 BUSCLK

01 : 4 BUSCLK

10 : 3 BUSCLK

11 : 2 BUSCLK

Bits 5:4 **8-bit I/O cycle command recovery time**

00 : 8 BUSCLK

01 : 5 BUSCLK

10 : 4 BUSCLK

11 : 3 BUSCLK

Bit 3 **Reserved**

Bit 2 **16-bit memory, I/O wait state selection**

0 : 1 wait state

1 : 0 wait state

Bit 1 **Reserved**

4.

Bit 0 Reserved

4.

Register 53h

Bits 7:2 Reserved

Bit 1 Reserved and must be set to 0.

Bit 0 PCI Output and Bi-directional Buffers Current Selection

0: 50mA/2.2V (default value)

1: 95mA/2.2V

Register 54h BIOS Register

Bits 7:0 BIOS can use this register to store data.

Register 55h

Bits 7:0 The same value as port 70h.

Register 58h

Bits 7:3, 1 Corresponds to the mask bits of the IRQ7-1.

When disabled, any event from the corresponding IRQ will cause the system to exit the system standby state.

0: Disable

1: Enable

Bit 2 GPIO0 Mask bit

When disabled, GPIO0 will cause the system to exit the system standby state.

0: Disable

1: Enable

Bit 0 Mask bit of the NMI.

When disabled, an event from the NMI will cause the system to exit the system standby state.

0: Disable

1: Enable

Register 59h

Bits 7:0 Corresponds to the mask bits of the IRQ8-15.

4.

When disabled, any event from the corresponding IRQ will cause the system to exit the system standby state.

Register 5Ah

Bits 7:1 Corresponds to the mask bits of the IRQ7-1.

When disabled, any event from the corresponding IRQ will cause the system to exit the monitor standby state.

Bit 0 Is the mask bit of the NMI.

When disabled, an event from the NMI will cause the system to exit the monitor standby state.

Register 5Bh

Bits 7:0 Corresponds to the mask bits of the IRQ8-15.

When disabled, any event from the corresponding IRQ will cause the system to exit the monitor standby state.

1.3.4. PCI IDE Configuration Registers

Register 00, 01h - Vendor ID

Bits 15:0 1039h(Read Only)

Register 02, 03h - Device ID

Bits 15:0 0597h(Read Only)

Register 04h - Command low byte

Bits 7:3 These bits are hardwired to 0.

Bit 2 Bus Master Enable

When set, the Bus master function is enabled. It is disabled by default.

Bit 1 Memory Space Enable

This bit is disabled by default. Read only.

Bit 0 I/O Space Enable

When enabled, the built-in IDE will respond to any access of the IDE legacy ports in the compatibility mode, or to any access of the IDE relocatable ports in the native mode. Also, any access to the PCI bus master IDE registers are allowed. This bit is zero(disabled) on reset.

Register 05h - Command high byte

Bits 15:8 00h(Read Only)

Register 06h - Status low byte

Bits 7:6 These bits are hardwired to zero.

Bit 5 This is a reserved bit, and is recommend to program 0.

Bits 4:0 These bits are hardwired to zero.

Register 07h - Status high byte

Bits 7:6 These bits are hardwired to zero.

Bit 5 Master Abort Asserted

This bit is set when a PCI bus master IDE transaction is terminated by master abort. While this bit is set, IDE will issue an interrupt request. This bit can be cleared by writing a 1 to it.

Bit 4 Received Target Abort

The bit is set whenever PCI bus master IDE transaction is terminated with target abort.

Bit 3 Signaled Target Abort.

The bit will be asserted when IDE terminates a transaction with target abort.

Bits 2:1 DEVSEL# Timing DEVT.

These two bits define the timing of asserting DEVSEL#. The built-in IDE always asserts DEVSEL# in fast timing, and thus the two bits are hardwired to 0 per PCI Spec.

Bit 0 Reserved, Read as "0".

Register 08h - Revision Identification

Bits 7:0 B0h(Read Only)

Register 09h - Programming Interface Byte

Bit 7 Master IDE Device

This bit is hardwired to one to indicate that the built-in IDE is capable of supporting bus master function.

Bits 6 IDE Channel Status Reporting Bit

While the bit is enabled, Bits 5 and 4 can be queried to determine status of the IDE controller. (The default value is '1', which means enable.)

Bit 5 **IDE Primary channel enable.**

This bit can be read or written. BIOS and OS code can change this bit as follows:

If a '1' is written and read back, then the device has been enabled.

If a '1' is written and a '0' is read back, then the device stays disabled. If a '0' is written and read back, the device has been disabled. If a '0' is written and a '1' is read back, the device stays enabled.

The default value of this bit is '1'.

Bit 4 **IDE Secondary channel enable.**

This bit can be read or written. BIOS and OS code can change this bit as follows:

If a '1' is written and read back, then the device has been enabled.

If a '1' is written and a '0' is read back, then the device stays disabled. If a '0' is written and read back, the device has been disabled. If a '0' is written and a '1' is read back, the device stays enabled.

The default value of this bit is '1'.

Bit 3 **Secondary IDE Programmable Indicator**

This bit is hardwired to one to indicate that the secondary IDE channel can be programmed to operate in compatible or native mode.

Bit 2 **Secondary IDE Operating Mode**

This bit defines the mode that the secondary IDE channel is operating in. Zero corresponds to 'compatibility' while one means native PCI mode. By default, the bit is 0 and is programmable.

Bit 1 **Primary IDE Programmable Indicator**

This bit is hardwired to one to indicate that the primary IDE channel can be programmed to operate in compatible or native mode.

Bit 0 **Primary IDE Operating Mode**

This bit defines the mode that the primary IDE channel is operating in. Zero corresponds to 'compatibility' while one means native PCI mode. The powerup state for this bit is 0, and can be set if native mode is expected.

Register 0Ah - Subclass ID

Bits 7:0 **01h**

Register 0Bh - Class ID

Bits 7:0 **01h**

Register 0Ch - Cache Line Size

Bits 7:0 00h

Register 0Dh- Latency Timer

Bits 7:0 Programmable (from 0 to 255). The default value is 0.

Register 0Eh - Header Type

Bits 7:0 80h

Register 0Fh - BIST

Bits 7:0 00h

Register 10, 11, 12, 13h Primary Channel Base Address Register

Register 14, 15, 16, 17h Primary Channel Base Address Register

Register 18, 19, 1A, 1Bh Secondary Channel Base Address Register

Register 1C, 1D, 1E, 1Fh Secondary Channel Base Address Register

In the native mode, these four registers define the IDE base address for each of the two IDE devices in both the primary and secondary channels respectively. In the compatible mode, the four registers can still be programmed and read out, but it does not affect the IDE address decoding.

Register 20, 21, 22, 23h Bus Master IDE Control Register Base Address

Offset Register	Register Access
00h	Bus Master IDE Command Register (Primary)
01h	Reserved
02h	Bus Master IDE Status Register(Primary)
03h	Reserved
04-07h	Bus Master IDE PRD (*) Table Pointer (Primary)
08h	Bus Master IDE Command Register (Secondary)
09h	Reserved
0Ah	Bus Master IDE Status Register (Secondary)
0Bh	Reserved
0C-0Fh	Bus Master IDE PRD (*) Table Pointer (Secondary)

*PRD: Physical Region Descriptor

Initialization of the base address during the BIOS boot up sequence is a must. The recommended value for register 23, 22, 21, and 20h are 00004000h, 0000B000h, 0000C000h, and etc.

Register 24 to 2Bh These bits are hardwired to zero

4.

Register 2C, 2Dh, 2E, 2Fh Reserved. Read as"0".

Register 30, 31, 32, 33h Expansion ROM Base Address

These four byte registers are recommended not to be programmed.

The following 10 registers define the speed of accessing IDE data and command registers. The four most significant bits of each Recovery Time Control byte are hardwired to zero, and the rest is R/W programmable with the following definition.

Recovery Time Control

Bits 3:0	Recovery Time
0000	12 PCICLK
0001	1 PCICLK
0010	2 PCICLK
0011	3 PCICLK
0100	4 PCICLK
0101	5 PCICLK
0110	6 PCICLK
0111	7 PCICLK
1000	8 PCICLK
1001	9 PCICLK
1010	10 PCICLK
1011	11 PCICLK
1100	13 PCICLK
1101	14 PCICLK
1110	15 PCICLK
1111	15 PCICLK

The five most significant bits of each Active Time Control byte are hardwired to zero, and the rest is R/W programmable with the following definition.

Active Time Control

Bits 2:0	Active Time
000	8 PCICLK
001	1 PCICLK
010	2 PCICLK
011	3 PCICLK
100	4 PCICLK
101	5 PCICLK
110	6 PCICLK
111	12 PCICLK

Register 40h IDE Primary Channel/Master Drive Data Recovery Time Control.

Register 41h IDE Primary Channel/Master Drive Data Active Time Control.

4.

Register 42h IDE Primary Channel/Slave Drive Data Recovery Time Control.

Register 43h IDE Primary Channel/Slave Drive Data Active Time Control

Register 44h IDE Secondary Channel/Master Drive Data Recovery Time Control.

Register 45h IDE Secondary Channel/Master Drive Data Active Time Control

Register 46h IDE Secondary Channel/Slave Drive Data Recovery Time Control.

Register 47h IDE Secondary Channel/Slave Drive Data Active Time Control

Register 48h IDE Command Recovery Time Control

Register 49h IDE Command Active Time Control

Register 4Ah IDE General Control Register 0

Bit 7 **Enable\disable burst mode. (1: Enable; default value = 0)**

Bit 6 **Reserved (The bit should be programmed with '0'.)**

Bit 5 **Synchronization of I/O channel ready by PCI clock**

0: Enable (Default)

1: Disable

Bit 4 **Secondary Channel using Master PIO mode.**

Bit 3 **Primary Channel using Master PIO mode.**

Bit 2 **IDE Secondary Channel enable. (0 to disable)**

Bit 1 **IDE Primary Channel enable. (0 to disable)**

Bit 0 **Reserved.**

Register 4Bh IDE General Control register 1

Bit 7 **Enable Prefetch of the Slave Drive in Secondary Channel. ('1' to enable.)**

Bit 6 **Enable Prefetch of the Slave Drive in Primary Channel. ('1' to enable.)**

Bit 5 **Reserved. (The bit should be programmed as '0')**

Bit 4 **Bus Master speed control**

0: PCI Request asserted while there are 20 bytes in FIFO

1: PCI Request asserted while there are 16 bytes in FIFO

Bit 3 **Secondary channel post write enable. (1 to enable)**

Bit 2 **Primary channel post write enable. (1 to enable)**

Bit 1 **Enable Prefetch of the Master Drive in Secondary Channel. ('1' to enable.)**

Bit 0 **Enable Prefetch of the Master Drive in Primary Channel. ('1' to enable.)**

(Following two 16-bit wide registers define the prefetching length of each IDE channel respectively.)

Register 4Ch	**Prefetch Count of Primary Channel (Low Byte)**
Register 4Dh	**Prefetch Count of Primary Channel (High Byte)**
Register 4Eh	**Prefetch Count of Secondary Channel (Low Byte)**
Register 4Fh	**Prefetch Count of Secondary Channel (High Byte)**

1.3.5. PCI Bus Master IDE Registers

The PCI Bus master IDE Registers use 16 bytes of I/O Space. These registers can be accessed through I/O R/W to the address defined in the Bus Master IDE register Base Address in the Configuration space. The definition of each register is described below.

Bus Master IDE Command Register

Bits 7:4 **Reserved. Return 0 on reads.**

Bit 3 **Read or Write Control. This bit defines the R/W control of the bus master transfer. When set to zero, PCI bus master reads are conducted. When set to one, PCI bus master writes are conducted.**

Bits 2:1 **Reserved.**

Bit 0 **Start/Stop Bus Master**

The 5513 built-in IDE Controller enables its bus master operation whenever it detects this bit changing from a zero to a one. The operation can be halted by writing a zero to this bit.

Bus Master IDE Status Register

Bit 7 **Simplex Only**

This bit is hardwired to zero to indicate that only one bus master channel can be operated at a time.

Bit 6 **Drive 1 DMA Capable**

This R/W bit can be set by BIOS or driver to indicate that drive 1 for this channel is capable of DMA transfers.

Bit 5 **Drive 0 DMA Capable**

This R/W bit can be set by BIOS or driver to indicate that drive 0 for this channel is capable of DMA transfers.

Bits 4:3 Reserved. Return 0 on reads

Bit 2 Interrupt

The bit is set by the rising edge of the IDE interrupt line to indicate that all data transferred from the drive is visible in the system memory. Writing a '1' to this bit can reset it.

Bit 1 Error

This bit is set when the IDE controller encounters an error during data transferring to/from memory.

Bit 0 Bus Master IDE Device Active

This bit is set when the start bit in the command register is set. It can be cleared when the last transfer of a region is performed, or the start bit is reset.

PRD Table Pointer Register

This 32-bit register contains address pointing to the starting address of the PRD table.

Bits 31:2 Base Address of the PRD Table

Bits 1:0 Reserved

1.4. Pin Assignment and Description

1.4.1. Hardware Trap

The following is a summary of all the power on options that are loaded into the PSIO based on the voltage level presented on the respective strapping at the rising edge of PCIRST#.

Table 1-4

Pin No	Symbol	Description
158	SDIR#	Internal/External KBC Select: This trapping status can be accessed through the reading of bit 3 of configuration register 70h. 0 : Internal KBC is enabled. 1 : Internal KBC is disabled. Once built-in KBC is employed, an external F138 is required to decode DAK[2:0] into DACK[7:5,3:0] respectively. The DACK3#, and DACK5# are acted as KBDAT, and KBCLK. The KLOCK# comes from GPIO0 if bit 4 of configuration register 70h is set. The DACK[7:6]# is reserved for further application. But, if USB port 1 is used, DACK[7:6]# can be used to serve as MIRQ[1:0] by setting bit of configuration register
23	PHOLD#	Enable/Disable the Support of PS/2 Mouse: The prerequisite for PSIO to support the PS/2 mouse is to enable the internal KBC, and to set the bit. Under such circumstances, WAKEUP0, and IRQ1 acts as PSMDAT, and PSMCLK, respectively. By the nature, the IRQ12 is internally generated, and is directly fed to the 8259. The IRQ12, in this case, can be used as the MDRQ0 signal by the setting of bit 2 of configuration register 70h, if the USB port 0 is enabled. This makes the SiS5513 offer at least one motherboard DMA request/acknowledge pair even though the USB function, the internal KBC, and the PS/2 mouse are all employed. On the other hand, if the PS/2 mouse is disabled by clearing the bit, the WAKEUP0 can be served as MDRQ0 by the setting of bit 1 of the configuration register 70h. 0: Disable PS/2 mouse 1: Enable PS/2 mouse
9	ROMKBCS#	External Super I/O Select: The power up value on this signal determines if the external super I/O(with built-in RTC, and KBC), like NS303 is used. 0: Select external super I/O 1: Deselect external super I/O

The actual function of multi-function pins in various configuration is summarized as follows:

Table 1-5

	Pin 15	**Pin 14**	**Pin 13**	**Pin 12**
Ext RTC	RTCRD	RTCALE	RTCWR	IRQ8
Int RTC	PSRSTB	-RTCPWRGD	OSC0	OSCI

NOTE:
Following is a list of some recommended applications for a reference purpose. The first one is actually the very basic application provided by 5513A. The second one is the application provided by 5513B which supports KBC and PS/2 mouse in addition to 5513A. As it is mentioned earlier, IRQ12 will be released if PS/2 mouse is disabled. Also, KLOCK# shares the pin with GPIO0, which is software controllable. In 5513C, the USB function is included, with the support of two USB ports. The USB function can be enabled/disabled through software programming so can each USB port. Although 5513 multiplexes the USB signals with PnP signals, it still tries to reserve the minimum support of PnP function. For instance, if USB port 0 is enabled, one motherboard DMA REQ/ACK can still be supported by programming pin 191, or pin 20 as MDRQ0 depending on if IRQ12 is allocated for external serial device. If USB port 1 is enabled, the Pin 199, and 200 can be programmed to be MIRQ[1:0], respectively.

To support Hotkey in the 5511G series chipset, Pin 200 can also be programmed to serve as the "Sleep" event which should be connected to the BREAK# pin of 5511G. In 5596 series chipset, this "sleep event" in response to Hotkey is transmits also through DEVDET signal.

Table 1-6

	(1)5513A	**(2)5513B**	**(3)5513C+KBC+ USB+PNP**	**(4)5513C+USB+P NP**
Pin No.	**Signal**	**Signal**	**Signal**	**Signal**
10	GPIO0	CPIO0/KLOCK#	KLOCK#/GPIO0	GPIO0
20	WAKEUP0	PSMDAT	PSMDAT	WAKEUP0 /MDRQ0
118	MDRQ0	MDRQ0	/USBV0+	/USBV0+
119	MDRQ1	MDRQ1	/USBV0-	/USBV0-
120	MDACK0#	MDACK0#	VCC3	VCC3
121	MDACK1#	MDACK1#	/USBCLK	/USBCLK
122	MIRQ0	MIRQ0	/USBV1+	/USBV1+
123	MIRQ1	MIRQ1	/USBV1-	/USBV1-
181	IRQ1	PSMCLK	PSMCLK	IRQ1
191	IRQ12	IRQ12	IRQ12/MDRQ0	IRQ12
194	DACK0#	DAK0	DAK0	DACK0#/DAK0
195	DACK1#	DAK1	DAK1	DACK1#/DAK1
196	DACK2#	DAK2	DAK2	DACK2#/DAK2
197	DACK3#	KBDAT	KBDAT	DACK3#
198	DACK5#	KBCLK	KBCLK	DACK5#
199	DACK6#	-	MIRQ0	DACK6#/MIRQ0
200	DACK7#	-	MIRQ1/HSLEEP	DACK7#/MIRQ1

4.

1.4.2. Pin Assignment

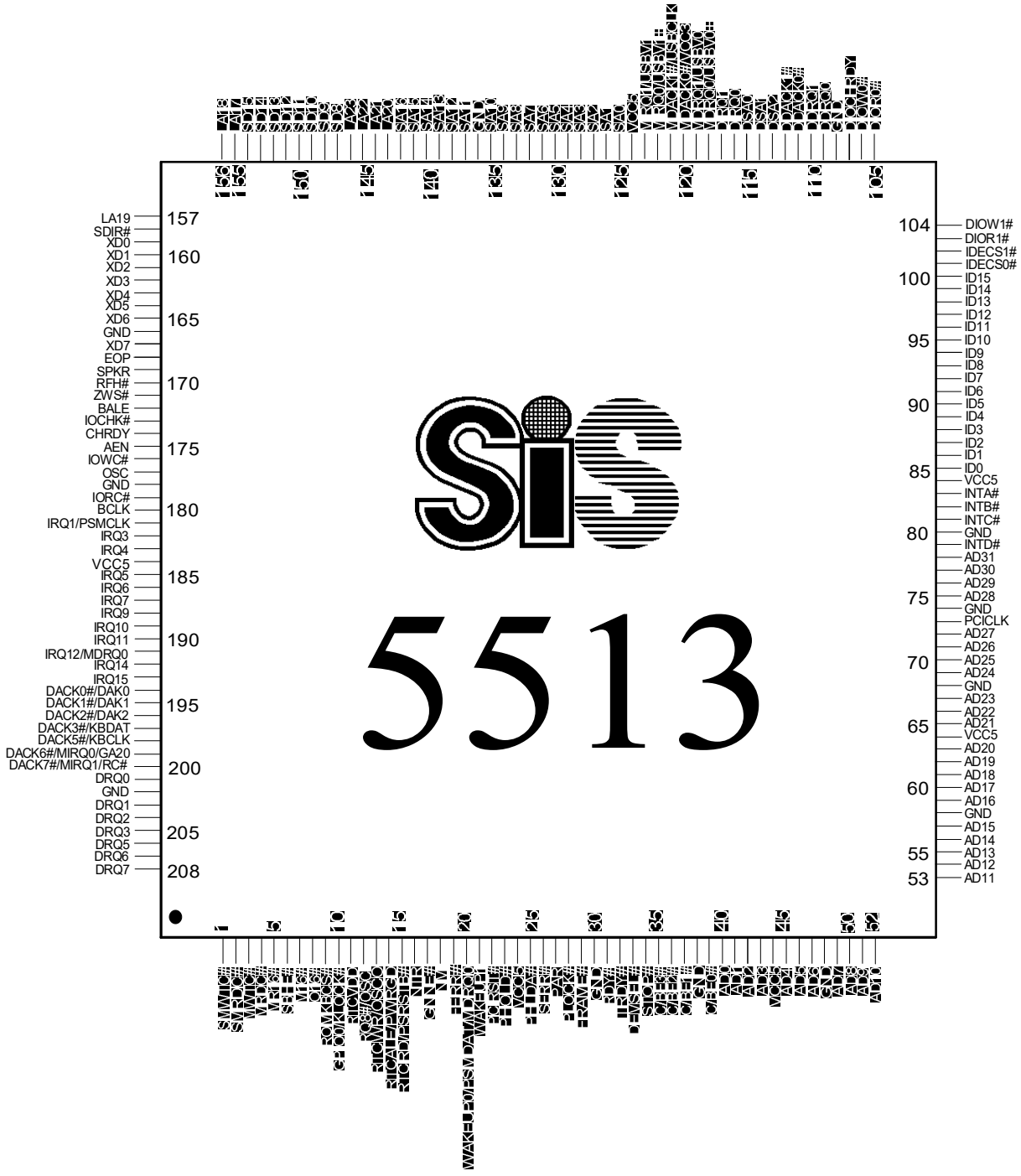


Figure 1.13

4.

1.4.3. Pin Listing (# means active low)

Table 1-7

1=SMWTC#	5V	48=GND	VSS	95=ID10	5V
2=SMRDC#	5V	49=AD7	5V	96=ID11	5V
3=MWTC#	5V	50=AD8	5V	97=ID12	5V
4=MRDC#	5V	51=AD9	5V	98=ID13	5V
5=MR16#	5V	52=AD10	5V	99=ID14	5V
6=SBHE#	5V	53=AD11	5V	100=ID15	5V
7=M16#	5V	54=AD12	5V	101=IDECS0#	5V
8=IO16#	5V	55=AD13	5V	102=IDECS1#	5V
9=ROMKBCS#	5V	56=AD14	5V	103=DIOR1#	5V
10=GPIO0/KLOCK#	5V	57=AD15	5V	104=DIOW1#	5V
11=RTCVDD	5V	58=GND	VSS	105=DIOR0#	5V
12=IRQ8#/OSCI	5V	59=AD16	5V	106=DIOW0#	5V
13=RTCWR/OSCO	5V	60=AD17	5V	107=DIOCHRDY	5V
14=RTCALE/PWRGD	5V	61=AD18	5V	108=GND	VSS
15=RTCRD/PSRSTB#	5V	62=AD19	5V	109=DDRQ0	5V
16=INTR	5V	63=AD20	5V	110=DDRQ1	5V
17=IGNNE#	5V	64=VCC5	5V	111=DDACK0#	5V
18=NMI	5V	65=AD21	5V	112=DDACK1#	5V
19=FERR#	5V	66=AD22	5V	113=DSA2	5V
20= WAKEUP0/PSMDAT/ MDRQ0	5V	67=AD23	5V	114=DSA1	5V
21=WAKEUP1	5V	68=GND	VSS	115=DSA0	5V
22=PCIRST#	5V	69=AD24	5V	116=DIRQ0	5V
23=PHOLD#	5V	70=AD25	5V	117=DIRQ1	5V
24=VCC5	5V	71=AD26	5V	118=MDRQ0/USBV0+	5V
25=PHLDA#	5V	72=AD27	5V	119=MDRQ1/USBV0-	5V
26=SERR#	5V	73=PCICLK	5V	120=MDACK0#	5V
27=PAR	5V	74=GND	VSS	121=MDACK1#/USBCLK	5V
28=PLOCK#	5V	75=AD28	5V	122=MIRQ0/USBV1+	5V
29=FRAME#	5V	76=AD29	5V	123=MIRQ1/USBV1-	5V
30=GND	VSS	77=AD30	5V	124=VCC5	5V
31=IRDY#	5V	78=AD31	5V	125=SA0	5V
32=TRDY#	5V	79=INTD#	5V	126=SA1	5V
33=DEVSEL#	5V	80=GND	VSS	127=SA2	5V
34=STOP#	5V	81=INTC#	5V	128=SA3	5V
35=C/BE3#	5V	82=INTB#	5V	129=SA4	5V
36=C/BE2#	5V	83=INTA#	5V	130=SA5	5V
37=C/BE1#	5V	84=VCC5	5V	131=SA6	5V
38=GND	VSS	85=ID0	5V	132=SA7	5V
39=C/BE0#	5V	86=ID1	5V	133=SA8	5V
40=AD0	5V	87=ID2	5V	134=SA9	5V
41=AD1	5V	88=ID3	5V	135=SA10	5V
42=AD2	5V	89=ID4	5V	136=GND	VSS
43=AD3	5V	90=ID5	5V	137=SA11	5V
44=VCC5	5V	91=ID6	5V	138=SA12	5V
45=AD4	5V	92=ID7	5V	139=SA13	5V
46=AD5	5V	93=ID8	5V	140=SA14	5V
47=AD6	5V	94=ID9	5V	141=SA15	5V

142=SA16	5V	176=IOWC#	5V
143=LA20	5V	177=OSC	5V
144=LA21	5V	178=GND	VSS
145=LA22	5V	179=IORC#	5V
146=LA23	5V	180=BCLK	5V
147=SD8	5V	181=IRQ1/PSMCLK	5V
148=SD9	5V	182=IRQ3	5V
149=SD10	5V	183=IRQ4	5V
150=SD11	5V	184=VCC5	5V
151=SD12	5V	185=IRQ5	5V
152=SD13	5V	186=IRQ6	5V
153=SD14	5V	187=IRQ7	5V
154=SD15	5V	188=IRQ9	5V
155=LA17	5V	189=IRQ10	5V
156=LA18	5V	190=IRQ11	5V
157=LA19	5V	191=IRQ12/MDRQ0	5V
158=SDIR#	5V	192=IRQ14	5V
159=XD0	5V	193=IRQ15	5V
160=XD1	5V	194=DACK0#/DAK0	5V
161=XD2	5V	195=DACK1#/DAK1	5V
162=XD3	5V	196=DACK2#/DAK2	5V
163=XD4	5V	197=DACK3#/KBDAT	5V
164=XD5	5V	198=DACK5#/KBCLK	5V
165=XD6	5V	199=DACK6#/MIRQ0/GA20	5V
166=GND	VSS	200=DACK7#/MIRQ1/RC#	5V
167=XD7	5V	201=DRQ0	5V
168=EOP	5V	202=GND	VSS
169=SPKR	5V	203=DRQ1	5V
170=RFH#	5V	204=DRQ2	5V
171=ZWS#	5V	205=DRQ3	5V
172=BALE	5V	206=DRQ5	5V
173=IOCHK#	5V	207=DRQ6	5V
174=CHRDY	5V	208=DRQ7	5V
175=AEN	5V		

NOTE: Pin 120 will be VCC3 (3.3V power) in the version of 5513 with USB.

1.4.4. Pin Description

Table 1-8 PCI Interface

Pin No.	Symbol	Typ	Function
39, 37-35	C/BE[3:0]#	I/O	Bus Command and Byte Enables. During the address phase of a transaction, C/BE[3:0]# define the bus command. During the data phase C/BE[3:0]# are used as byte enables. The 5513 drives C/BE[3:0]# as an initiator of a PCI bus cycle and monitors C/BE[3:0]# as a target.

78-75, 72-69, 67-59, 57-49	AD[31:0]	I/O	PCI Address/Data. AD[31:0] is a multiplexed address and data bus. During the first clock of a transaction, AD[31:0] contains a physical byte address. During the subsequent clocks, AD[31:0] contains data. When the 5513 is a target, AD[31:0] are inputs during the address phase of a transaction. During the following data phases, the 5513 supplies data on AD[31:0] for a PCI read, or accepts data for a PCI write. As an initiator, the 5513 drives a valid address on AD[31:2] during the address phase, and drives write data or latches read data on AD[31:0] during the data phases. The 5513 always drives AD[1:0] low as a master during the address phase.
29	FRAME#	I/O	FRAME# is an input to the 5513 when the 5513 is the target. FRAME# is an output when the 5513 is the initiator. FRAME# is tri-state during reset.
31	IRDY#	I/O	IRDY# indicates the 5513's ability, as an initiator, to complete the current data phase of the transaction. During a write, IRDY# indicates the 5513 has valid data present on AD[31:0]. During a read, it indicates the 5513 is prepared to latch the read data. IRDY# is an input to the 5513 when the 5513 is the target and an output when the 5513 is an initiator.
32	TRDY#	I/O	TRDY# indicates a slave's ability to complete the current data phase of the transaction. During a read, TRDY# indicates that the 5513, as a target, has placed valid data on AD[31:0]. During a write, it indicates that the 5513, as a target, is prepared to latch write data. TRDY# is an output when the 5513 is a target and an input when the 5513 is an initiator.
33	DEVSEL#	I/O	The 5513 asserts DEVSEL# to claim a PCI transaction through positive or subtractive decoding. As an output, the 5513 asserts DEVSEL# when it samples IDSEL active in configuration cycles to 5513 configuration registers. The 5513 also asserts DEVSEL# when an internal 5513 register is addressed or when the 5513 subtractively decodes a cycle. As an input, DEVSEL# indicates a PCI target has responded to a 5513 initiated transaction. The 5513 also samples this signal for all PCI transactions to decide to subtractively decode the cycle.
34	STOP#	I/O	STOP# indicates that the 5513, as a target, is requesting an initiator to stop the current transaction. As a master, STOP# causes the 5513 to stop the current transaction. STOP# is an output when the 5513 is a target and an input when the 5513 is an initiator.

27	PAR	O	PAR is an even parity calculated based on AD[31:0] and C/BE3-0#. PAR is an output during the address phase(delayed by one clock) for all 5513 initiated transactions. It is also an output during the data phase (delayed by one clock) when the 5513 is the initiator of a PCI write transaction, and when it is the target of a read transaction.
26	SERR#	I	SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, the 5513 generates a non-maskable interrupt to the CPU.
28	PLOCK#	I	PLOCK# is always an input to the 5513. When the 5513 is the target of a transaction and samples PLCOK# negated during the address phase of a transaction, the 5513 considers itself a locked resource until it samples PLOCK# and FRAME# negated. When other masters attempt accesses while the 5513 is locked, the 5513 responds with a target initiated retry termination.
73	PCICLK	I	PCICLK provides timing for all transactions on the PCI bus. All other PCI signals are sampled on the rising edge of PCICLK, and all timing parameters are defined with respect to this edge. Frequencies supported by the 5513 include 25 and 33 MHz.
22	PCIRST#		PCIRST# forces the 5513 to a known state. All I/O and sustained tri-state I/O signals are forced to a high impedance state. All registers are set to their default values. PCIRST# may be asynchronous to PCICLK when asserted or negated. Although asynchronous, negation must be a clean, bounce-free edge. Note that PCIRST# must be asserted for more than 1us.
83-81, 79	INT[A:D]#	I	PCI Interrupt A to Interrupt D

Table 1-9 ISA Interface

Pin No.	Symbol	Typ	Function
142-137, 135-125	SA[16:0]	I/O	System address. They are inputs when an external bus master is in control and are outputs at all other times.
146-143, 157-155	LA[23:17]	I/O	Latched system address. They are inputs when an external bus master is in control and are outputs at all other times.
167, 165-159	XD[7:0]	I/O	Peripheral Data Bus lines.
154-147	SD[15:8]	I/O	System Data Bus are directly connected to the ISA slots.
8	IO16#	I	16-bit I/O chip select indicates that the AT bus cycle is a 16-bit I/O transfer when asserted or an 8-bit I/O transfer when it is negated.

7	M16#	I	16-bit memory chip select indicates a 16-bit memory transfer when asserted or an 8-bit memory transfer when it is negated.
6	SBHE#	I/O	Byte high enable signal indicates that the high byte has valid data on the ISA 16-bit data bus. This signal is an output except during ISA master cycles.
5	MR16#	I	Master* is an active low signal from AT bus. When active, it indicates that the ISA bus master has the control of the system. The address and control signals are all driven by the ISA bus master.
4	MRDC#	I/O	AT bus memory read command signal is an output pin during AT/DMA/refresh cycles and is an input pin in ISA master cycles.
3	MWTC#	I/O	AT bus memory write command signal is an output pin during AT/DMA cycles and is an input pin in ISA master cycles.
2	SMRDC#	I/O	AT bus memory read. It instructs the memory devices to drive data onto the data bus. It is active only when the memory being accessed is within the lowest 1MB.
1	SMWTC#	I/O	AT bus memory write. It instructs the memory devices to store the data presented on the data bus. It is active only when the memory being accessed is within the lowest 1MB.
179	IORC#	I/O	AT bus I/O read command signal is an output pin during AT or DMA cycles and is an input pin in ISA master cycles. When low, it strobes an I/O device to place data on the data bus.
176	IOWC#	I/O	AT bus I/O write command signal is an output pin during AT or DMA cycles and is an input pin in ISA master cycles. When low, it strobes data on the data bus into a selected I/O device.
175	AEN	O	Address Enable is driven high on the ISA bus to indicate the address lines are valid in DMA or ISA master cycles. It is low otherwise.
174	CHRDY	I/O	I/O channel ready is normally high. It can be pulled low by the slow devices on the AT bus to add wait states for the ISA memory or I/O cycles. When a DMA or an ISA master accesses a VL-Bus target, IORDY is an output to control the wait states.
173	IOCHK#	I	I/O channel Check is an active low input signal which indicates that an error has taken place on the I/O bus.

4.

172	BALE	O	Bus address latch enable is used on the ISA bus to latch valid address from the CPU. Its falling edge starts the ISA command cycles.
171	ZWS#	I	Zero wait state is an active low signal. The system ignores the IORDY signal and terminates the AT bus cycle without additional wait state when it is asserted.
180	BCLK	I/O	ISA bus clock, for ISA bus controller, ISA bus interfaces and the DMA controller. It can be programmed to derive from the SYSCLK or from the 14MHz clock.
170	RFH#	I/O	Refresh signal is used to initiate a refresh cycle. This signal is an input in ISA bus master cycles and is an output in other cycles.
177	OSC	I	OSC is the buffered input of the external 14.318MHz oscillator.
168	EOP	O	Terminal Count of DMA. A pulse is generated by the DMA controller when the terminal count (TC) of any channel reaches 1. When a TC pulse occurs, the DMA controller will terminate the service, and if auto-initialize is enabled, the base registers will be written to the current registers of that channel. The mask bit and the TC bit in the Status word will be set for the currently active channel unless the channel is programmed for auto-initialize. In that case, the mask bit remains clear.
208-203, 201	DRQ7-5,3-0	I	DMA Request inputs are used by external devices to indicate when they need service from the internal DMA controllers.
181, 191	IRQ1/ PSMCLK, IRQ12/ MDRQ0	I/O	These are the synchronous interrupt inputs to the 8259 interrupt controller. Specifically, when internal KBC is enabled, IRQ1 can be served as PSMCLK, and IRQ12 as MDRQ0, respectively.
182-183, 185-190 192-193	IRQ 3-7, IRQ 9, 10-11,14,15	I	These are the synchronous interrupt request inputs to the 8259 controller.

Table 1-10 IDE Interface & on Board Plug and Play

100-85	ID[15:0]	I/O	IDE data bus.
103, 105	DIOR[1:0]#	O	IDE I/O read cycle command.
104, 106	DIOW[1:0]#	O	IDE I/O write cycle command
107	DIOCHRDY	I	IDE I/O channel ready signal.
110, 109	DDRQ[1:0]	I	IDE DMA request signals.
112, 111	DDACK[1:0]#	O	IDE DMA acknowledge signals.
113	DSA[2:0]	O	IDE address [2:0].
117-116	DIRQ[1:0]	I	IDE interrupt request signals.

102-101	IDECS[1:0]#	O	IDE chip select signals.
123-122	MIRQ1/ USB1-, MIRQ0/ USBV1+	I/O	These are motherboard interrupt request signals which can be rerouted to any of the eleven PC compatible interrupt through programming the PCI configuration register 60h, and 61h. When USB function and USB port 1 is enabled, these pins are used as the two differential inputs of the USB port 1.
119-118	MDRQ1/ USBV0-, MDRQ0/ USBV0+	I/O	These are motherboard DMA request signals which can be remapped to any of the seven ISA compatible DMA channels. When USB function and port 0 is enabled, these two pins are used as the two differential inputs of the USB port 0.
121	MDACK1# /USBCLK	O	When USB function is enabled, this pin acts as the USB clock source. Otherwise, it is used as the motherboard DMA acknowledge signal associated with MDRQ1. Upon power up, it is an input, and an external weak pull up resistor associated with it is recommended. Only when the USB function is disabled, will the pin back to the role of MDACK1# which is of course in the output direction. To replace 5513A(B) with 5513C, the BIOS needs to disable the USB function when keeping all the original PnP support.
120	MDACK0#	O	The pin is the motherboard DMA acknowledge signal associated with the MDRQ0. In the version with USB, this pin should be changed to 3.3V power pin.

Table 1-11 Others

196-194	DACK[2:0] #/DAK[2:0]	O	These three pins are used as the DAK[2:0] which is encoded from DACK[7:0]# of the internal DMA controller, when the internal KBC is used, or when the DAK encoder is enabled by setting bit 1 of configuration register 72h.
197	DACK3#/ KBDAT	I/O	When the internal KBC is enabled, this pin is used as the keyboard data. Otherwise, it is the DACK3# signal as it was in 5513A, and 5513B.
198	DACK5#/ KBCLK	I/O	When the internal KBC is enabled, this pin is used as the keyboard clock. Otherwise, it is the DACK5# signal as it was in 5513A, and 5513B.

199	DACK6#/ MIRQ0/ GA20	I/O	This signal is an input upon power up. When the internal KBC is disabled, or the DAK encoder is disabled, it is the responsibility of BIOS to change its direction from input to output so that DACK6# function is maintained. This pin can be used as MIRQ0 by setting bit 0 of configuration register 72h. This pin can also be used as the Gate-A20 pin.
200	DACK7#/ MIRQ1/ RC#	I/O	This signal is an input upon power up. When the internal KBC is disabled, or the DAK encoder is disabled, it is the responsibility of BIOS to change its direction from input to output so that DACK6# function is maintained. This pin can be used as MIRQ1 by setting bit 0 of configuration register 72h. The third function of the pin is used as Fast Keyboard Reset.
12	IRQ8#/ OSCI	I	• When using internal RTC: This pin is used as the time base of the built-in RTC. This signal should be connected to 32.768 KHz crystal or oscillator input. • When using external RTC: This pin is used as IRQ8#, which is the asynchronous interrupt request input to the 8259 controller.
15	RTCRD/ PSRSTB#	I/O	• When using internal RTC: This signal is used as PSRSTB# (power strobe). PSRSTB# establishes the condition of the control register in RTC when power is first applied to the device. • When using external RTC: The signal is used as the data read strobe of RTC. It is used to drive the RTC data onto the XD bus when the CPU accesses the RTC.
14	RTCALE/ PWRGD	I/O	• When using internal RTC: The signal must be high for bus cycles in which the CPU accesses the RTC. All address, data, data strobe, and R/W pins of the internal RTC are disconnected from the processor when this signal is low. • When using external RTC: The signal is used to latch the address from the XD bus when CPU accesses RTC.
11	RTCVDD	I	Battery power for RTC internal RTC.
13	RTCWR/ OSCO	O	When using internal RTC: this pin should be connected the other end of the 32.768 KHz crystal or left unconnected if an oscillator is used. When using external RTC: This pin is used as data write strobe of RTC. It is used to store the data presented on the XD bus when CPU accesses the RTC. This pin must be connected to the R/W pin of RTC.
10	GPIO0/ KBLOCK	I/O	This pin is used as the keyboard lock signal or general purpose input/output 0.

4.

20	WAKEUP0/ PSMDAT/ MDRQ0	I/O	Upon power up, this signal is an input, and an external pull up resistor is required. By setting bit 3 of configuration register 72h, the pin reverts to an output signal functioning as WAKEUP0. When in input mode, it functions as PSMDAT if PS/2 mouse is enabled. Otherwise, it is the MDRQ0 signal.
21	WAKEUP1	O	In 5596 series, this signal transmits the IRQs, NMI, and Hotkey "Sleep" event to the 5596 PMU. In reality, these PMU related information are multiplexed by PCICLK in 5513, and then demultiplexed in 5596.
23	PHOLD#	I/O	The 5513 asserts PHOLD# to request PCI bus on behalf of IDE master, DMA, or ISA masters. The trapping logic of this pin on the PCIRST# rising edge also determines if the PS/2 mouse is to be supported by 5513 internal KBC.
25	PHLDA#	I	SIO Grant. It is driven by the 5511 to indicate that the PCI arbiter has granted the use of the PCI bus to the 5513.
9	ROMKBCS#	I/O	Keyboard or System ROM Chip Select. When asserted, it means the keyboard or ROM is to be accessed. Also, a high logic trapped on the PCICLK rising shows the support of the external super I/O.
169	SPKR	O	Speaker is the output for the speaker.
158	SDIR#	I/O	The internal KBC is also enabled when a low logic on this signal is sensed on the PCICLK rising edge.
19	FERR#	I	Floating point error from the CPU. It is driven active when a floating point error occurs.
17	IGNNE#	OD	IGNNE# is normally in high impedance state, and is asserted to inform CPU to ignore a numeric error. A resistor connected to 3.3V is required to maintain a correct voltage level to CPU.
18	NMI	OD	Non-maskable interrupt is rising edge trigger signal to the CPU and is generated to invoke a non-maskable interrupt. Normally, this signal is low. It goes high impedance state when a non-maskable interrupt source comes up. An external pull up resistor is required to be directly connected to CPU.
16	INTR	OD	Interrupt goes high impedance whenever a valid interrupt request is asserted. Hence, an external pull up resistor is required to be directly connected to the CPU's interrupt pin.
24, 64, 84, 124, 44, 184	VCC5		+5V DC power

4.

178, 74, 202, 166, 136, 108, 30, 38, 48, 58, 68, 80	GND		Ground

1.5. Electrical Characteristics

1.5.1. Absolute Maximum Ratings

Table 1-12

Parameter	Min	Max	Unit
Ambient operating temperature	0	70	^{O}C
Storage temperature	-40	125	^{O}C
Input voltage	-0.3	5.5	V
Output Voltage	-0.5	5.5	V
Power Dissipation		1	W

Note:
Stress above these listed may cause permanent damage to device. Functional operation of this device should be restricted to the conditions described under operating conditions.

1.5.2. DC Characteristics

TA = 0 - 70 ^{O}C, VSS = 0V , VDD=5V$\pm$5%

Table 1-13

Symbol	Parameter	Min	Max	Unit	Condition
V_{IL}	Input Low voltage	-0.3	0.8	V	
V_{IH}	Input High Voltage			V	
V_{OL}	Output Low Voltage		0.45	V	
V_{OH}	Output High Voltage	2.4		V	
I_{OL1}	Output Low Current	4		mA	***Note 1***
I_{OH1}	Output High Current	4		mA	***Note 1***
I_{OL2}	Output Low Current	8		mA	***Note 2***
I_{OH2}	Output High Current	8		mA	***Note 2***
I_{OL3}	Output Low Current	8,12		mA	***Note 3***
I_{OH3}	Output High Current	8,12		mA	***Note 3***
I_{OL4}	Output Low Current	6		mA	***Note 4***
I_{OH4}	Output High Current	6		mA	***Note 4***
I_{IL}	Input Leakage Current		+10	mA	
I_{OL}	Output Leakage Current		-10	mA	
C_{IN}	Input Capacitance		12	pF	
C_{OUT}	Output Capacitance		12	pF	
$C_{I/O}$	I/O Capacitance		12	pF	

Note:

1. I_{OL1} and I_{OH1} are applicable to ROMKBCS#, RTCWR/IDECYC#, RTCRD/PSRSTB#, RTCALE/PWRGD, WAKEUP0, WAKEUP1, PHOLD#, PAR, C/BE[3:0]#, AD[31:0], SDIR#, XD[7:0], SPKR, BCLK, DAK[2:0], MDAK[1:0]#, INT, NMI, IGNEE#.
2. I_{OL2} and I_{OH2} are applicable to RFH#, CHRDY, DIOCHRDY, AEN, BALE, EOP, SD[15:8].

4.

3. I_{OL3} and I_{OH3} are applicable to SMWTC#, SMRDC#, MWTC#, MRDC#, SBHE#, LA[23:20], IDECS[1:0]#, LA[21:17], SA[16:0], IOWC#, IORC#, DIORC[1:0]#, DIOWC[1:0]#, Please refer to Register description.

4. I_{OL4} and I_{OH4} are applicable to FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#.

1.5.3. AC Characteristics

The AC characteristic is measured under the following capacitive condition.

Capacitive load	Pin
35pf	BCLK, DAK[0:2], BALE, AEN, NMI, SDIR, EOP, SPKR, INT
50pf	FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, C/BE[3:0]#, XD[7:0]
150pf	SD[15:8], SBHE#, RFH#, CHRDY, MWTC#, MRDC#, IORC#, IOWC#, SA[19:0], LA[23:17]

Table 1-14

Para-meter	Description	Min	Typ	Max	Unit
ISA Bus Interface Signals (Figure 1.9)					
	BCLK High		63.2		ns
	BCLK Low		56.8		ns
t1	BALE valid delay from BCLK		4.5	7	ns
t2	IORC#, IOWC#, MRDC#, MWTC# valid delay from BCLK		16.5	24	ns
t3	IORC#, IOWC#, MRDC#, MWTC# invalid delay from BCLK		12	18	ns
t5a	M16# setup time to BCLK rising		15		ns
t5b	M16# hold time from BCLK rising		6		ns
t6a	IO16# setup time to BCLK falling		19		ns
t6b	IO16# hold time from BCLK falling		6		ns
t7	16 bit IORC#, IOWC# pulse width		1.5		BCLK
	8 bit IORC#, IOWC# pulse width		4.5		BCLK
	16 bit MRDC#, MWTC# *1		2		BCLK
	8 bit MRDC#, MWTC#		4.5		BCLK
	ROM MRDC#, MWTC# *1		2		BCLK
Data Buffer Interface					
t8	SD, XD data set up time to IORC#, MRDC# inactive	10			ns
t9	SD, XD data hold time to IORC#, MRDC# inactive	3			ns
t10	SD, XD valid data delay from IOWC#, MWTC# active (for data swapping)	15	22		ns
t11a	SD, XD data hold time from IOWC#, MWTC# inactive in write disassembly cycle	15	22		ns

t11b	SD, XD data hold time from IOWC#, MWTC# inactive in write cycle		172		ns
t12	SD, XD valid to IOWC#, MWTC# active		142		ns
t13	SDIR deassertion to IORC#, MRDC# active (16-bit)		1	2	BCLK
	SDIR deassertion to IORC#, MRDC# active (8-bit)	1.5		2.5	BCLK
t14	SDIR assertion delay from IORC#, MRDC# inactive		2		BCLK
Address Buffer Interface					
t15	SA, LA propagation delay from PCICLK in Frame# address phase		34	51	ns
t16	SA0, SA1, SBHE# hold time from the negation of IORC#, IOWC#, MWTC#, MRDC#	10			ns
t17a	CHRDY setup time to BCLK rising		15.2		ns
t17b	CHRDY hold time to BCLK rising	14.8			ns
t44	ZWS# setup time to BCLK falling		10		ns
t45	ZWS# hold time to BCLK falling	20			ns
DMA Compatible Timings (Figure 1.10, 1.11)					
t18	DAK active to IORC# active		0.5		DMACLK
t19	DAK active to IOWC# active		1.5		DMACLK
t20	DAK active hold from IORC# inactive		0.5		DMACLK
t21	DAK active hold from IOWC# inactive		0.5		DMACLK
t22a	AEN active to IORC# active		6		DMACLK
t22b	AEN active to IOWC# active		7		DMACLK
t23a	AEN inactive from IORC# inactive		3		DMACLK
t23b	AEN inactive from IOWC# inactive		4		DMACLK
t24a	BALE active to IORC# active		1.5		DMACLK
t24b	BALE active to IOWC# active		2.5		DMACLK
t25a	BALE inactive from IORC# inactive		1		DMACLK
t25b	BALE inactive from IOWC# inactive		1		DMACLK
t26a	LA, SA, SBHE# valid set up time to IORC#		1		DMACLK
t26b	LA, SA, SBHE# valid set up time to IOWC#		2		DMACLK
t27a	LA, SA, SBHE# valid hold from IORC#		0.5		DMACLK
t27b	LA, SA, SBHE# valid hold from IOWC#		0.5		DMACLK
t28	IORC# pulse width		4		DMACLK
t29	IOWC# pulse width		2		DMACLK
t30	MRDC# pulse width		3		DMACLK

4.

t31	MWTC# pulse width		3		DMACLK
t32	MWTC# active from IORC# active		1		DMACLK
t33	IOWC# active from MRDC# active		1		DMACLK
t34	MWTC# inactive from IORC# inactive		0		ns
t35	IOWC# inactive from MRDC# inactive		1.5		ns
t36	Read data valid from IORC# active		267.5		ns
t37	Read data valid hold from IORC# inactive		32.2		ns
t38	Write data valid setup to IOWC# inactive		162.5		ns
t39	Write data valid hold from IOWC# inactive		13.2		ns
t40	EOP active delay from IOWC# active		-7.6		ns
t41	EOP active delay from IORC# active		112.3		ns
t42	EOP active delay from IOWC# inactive		0.7		ns
t43	EOP active delay from IORC# inactive		0.8		ns
Note: DMACLK = BCLK or BCLK/2 depends on bit 0 of ISA configuration register 01H.					
Refresh Timing (Figure 1.20)					
t44	RFH# active setup to MRDC# active		2		BCLK
t45	RFH# active hold from MRDC# inactive		0.5		BCLK
t46	AEN active to RFH# active delay		3		ns
Miscellaneous Timing (Figure 1.12 ~ 1.16, 1.18, 1.19)					
t47	SERR#, IOCHK# active to NMI output floating active			200	ns
t48	INT output floating delay from IRQ active			100	ns
t49	IRQ active pulse width	100			ns
t50	IGNEE# active from IOWC# active for port F0h access			220	ns
t51	IGNEE# inactive from FERR# inactive			150	ns
t52	SPKR valid delay from OSC timing			200	ns
t53	RTCALE pulse width		532.3		ns
t54	RTCALE active from IORW# active		4		ns
t54a	RTCWR active from IOWR# active		5		ns
t54b	RTCRD active from IORD# active		5		ns
t54c	RTCWR inactive from IOWR# inactive	3.5	5	10	ns
t54d	RTCRD inactive from IORD# inactive	3.5	5	10	ns

***1: No command delay**

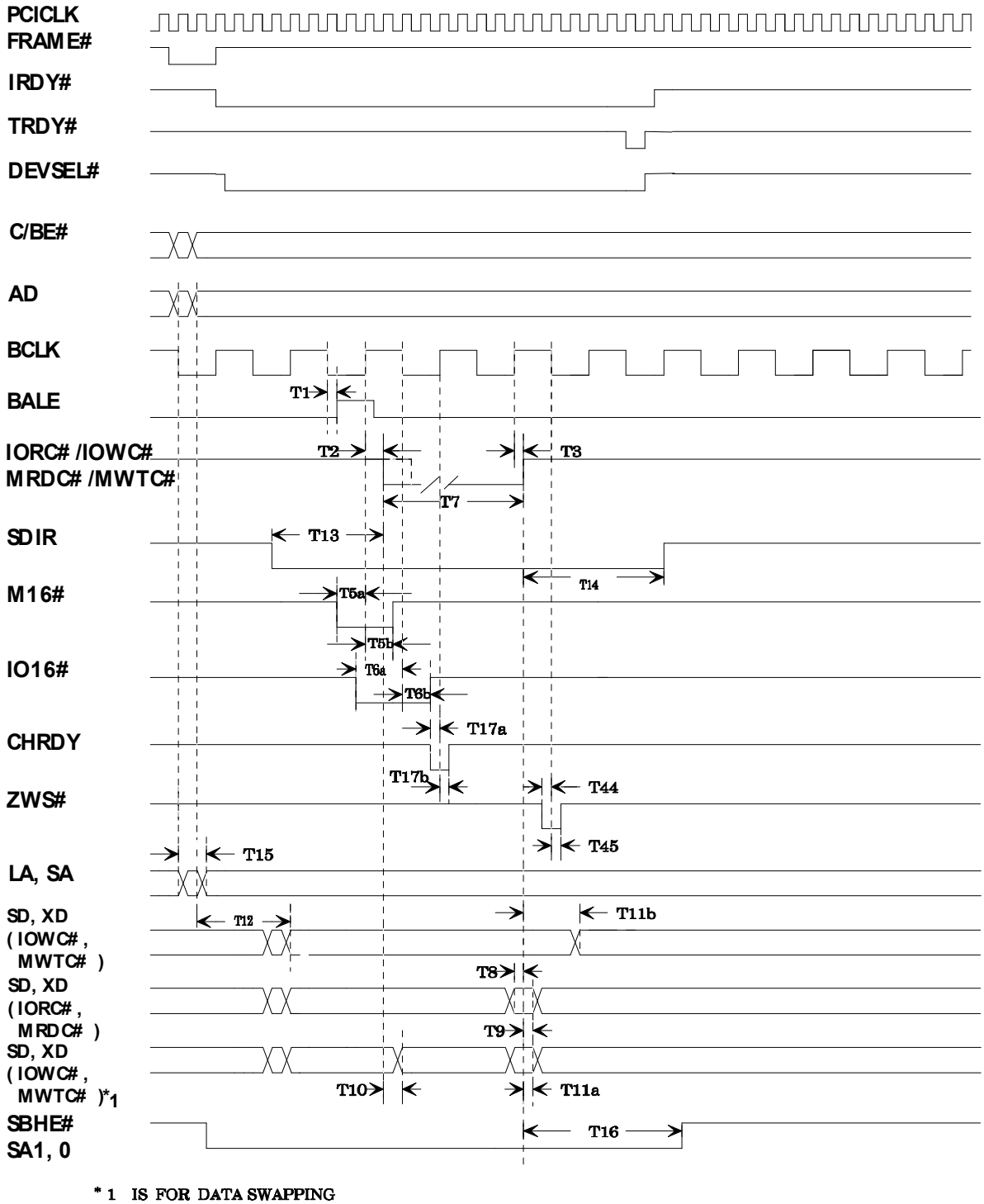
PCI Bus AC Specifications (Figure 1.17) The following parameters are applicable to AD[31:0], C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, LOCK#, IDSEL#, DEVSEL#, PAR, and SERR#.					
		Min	**Typ**	**Max**	**Units**
t57	Signal valid delay from PCICLK rising edge *2			11	ns
t58	Signal invalid delay from PCICLK rising edge	2			ns
t59	Hi-impedance to Active delay from PCICLK rising edge	2			ns
t60	Active to Hi-impedance delay from PCICLK rising edge			28	ns
t61	Setup time of input signal	7			ns
t62	Hold time of input signal	0			ns

***2: This parameter is measured under 50pf.**

PCI IDE Timing (Figure 1.21 ~ 1.22)					
Para-meter	**Description**	**Min**	**Typ**	**Max**	**Unit**
t63	Write Active Time	1		12	PCICLK
t64	Write Recovery Time	1		13	PCICLK
t65	Write Cycle Time (Post Write Buffer Enable)		5		PCICLK
t66	Read Active Time	1		12	PCICLK
t67	Read Recovery Time	1		13	PCICLK
t68	Read Cycle Time (Prefetch Buffer Enable)	3	5		PCICLK

Keyboard Controller Timing				
Para-meter	**Description**	**Min.**	**Max.**	**Units**
T69	Data valid after clock falling	8	12	us
T70	Keyboard clock period	20	--	us
T71	Keyboard clock pulse width	10	--	us
T72	Data valid before clock falling	4	--	us
T73	Keyboard ack after finish receiving	20	--	ns
T74	Transmit time-out	--	2	ms
T75	Start bit ready after clock disable	128	256	us
T76	Clock enable after start bit ready	--	128	us

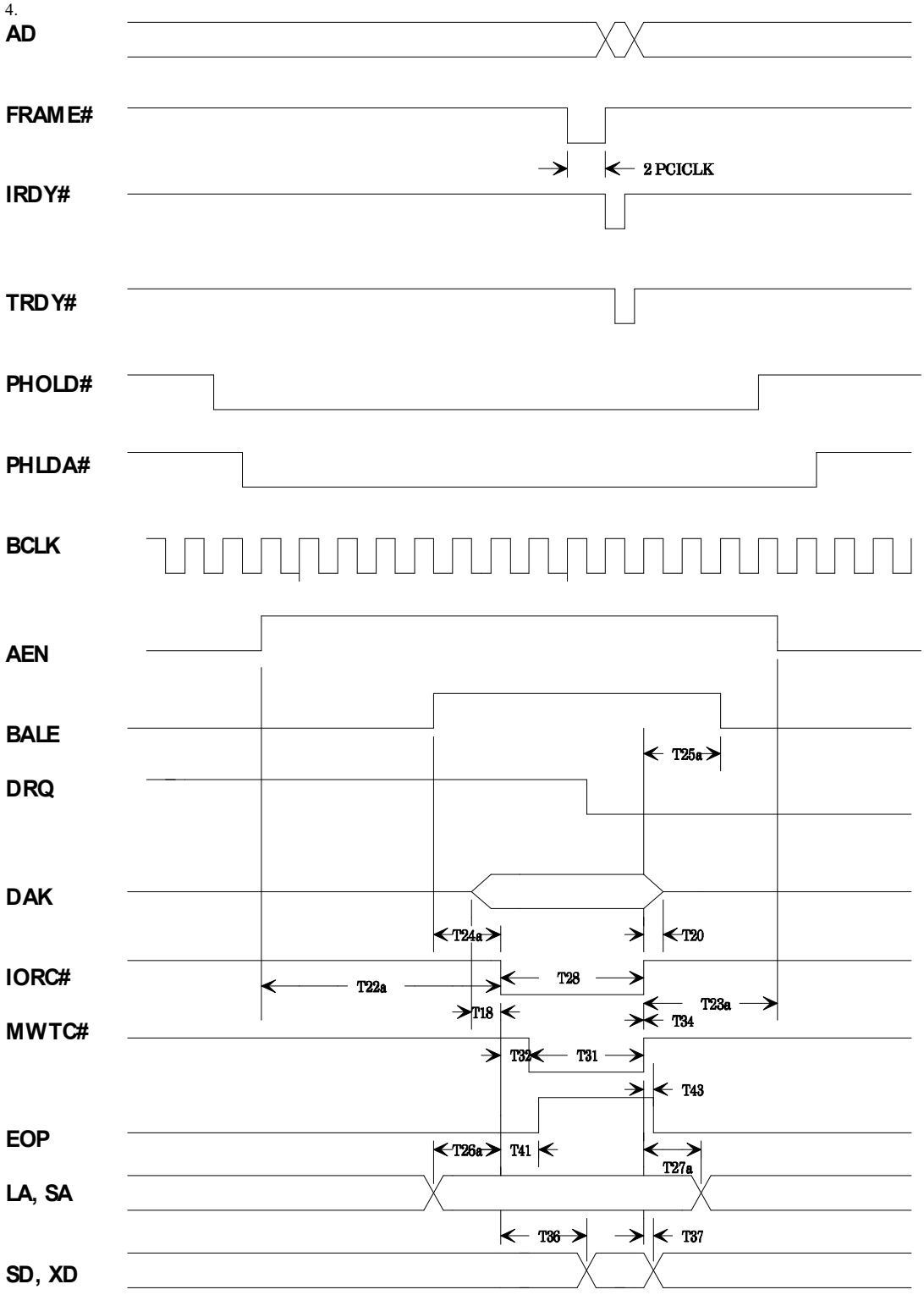
1.5.4. AC Timing Diagram



*1 IS FOR DATA SWAPPING

Figure 1.14 PCI to AT Bus Cycle

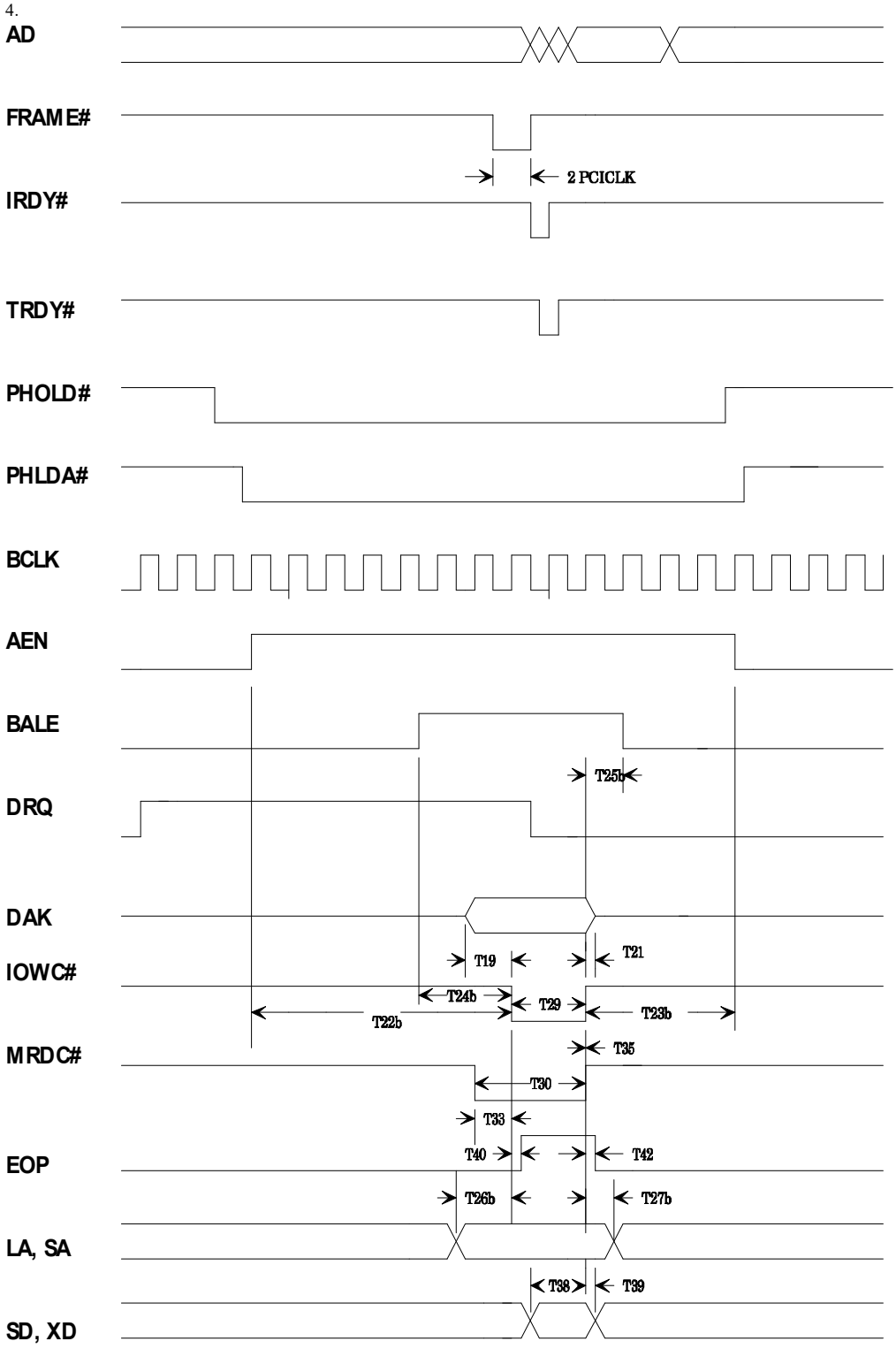
4.



DMA cycle (IOWC#, MRDC#), DMACLK = BCLK

Figure 1.15 DMA Cycle (IOWC#, MRDC#)

4.



DMA cycle (IORC#, MWTC#), DMACLK = BCLK

Figure 1.16 DMA Cycle (IORC#, MWTC#)

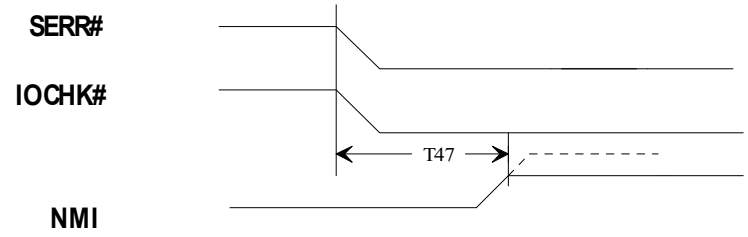


Figure 1.17

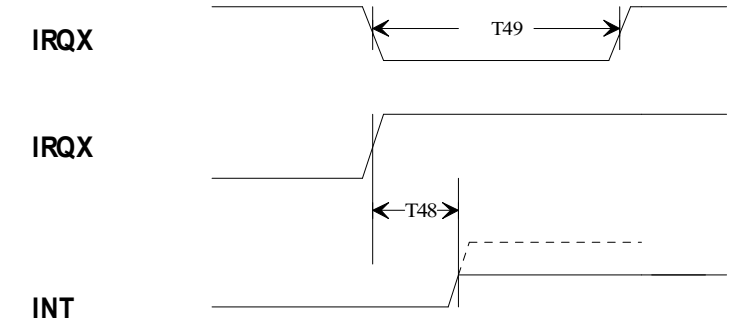


Figure 1.18

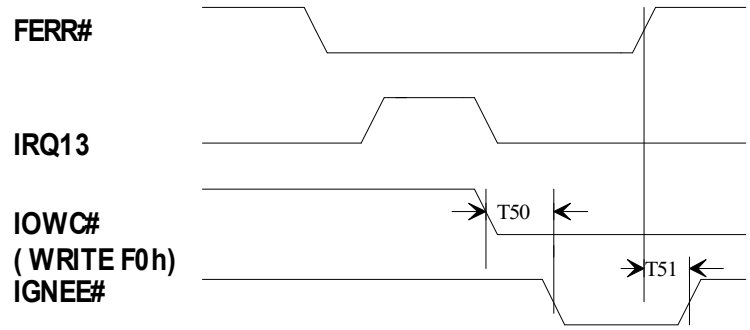


Figure 1.19

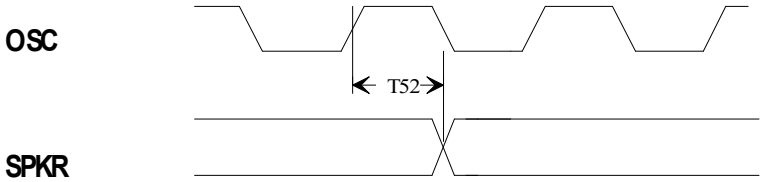


Figure 1.20

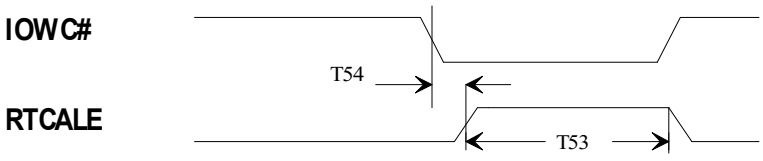


Figure 1.21

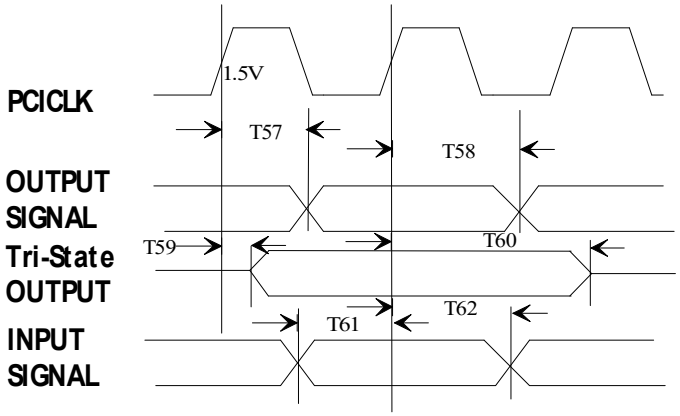


Figure 1.22

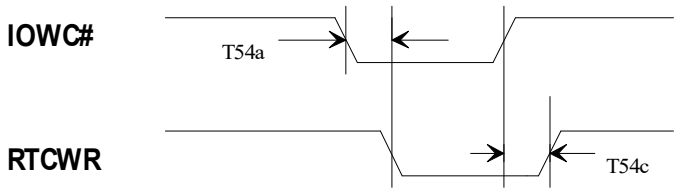


Figure 1.23

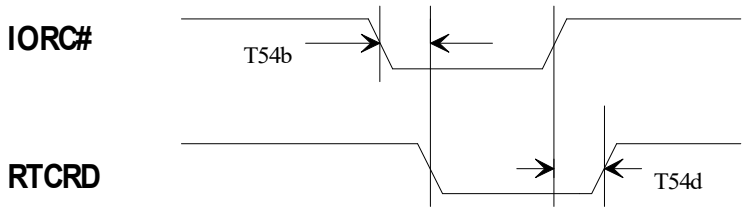


Figure 1.24

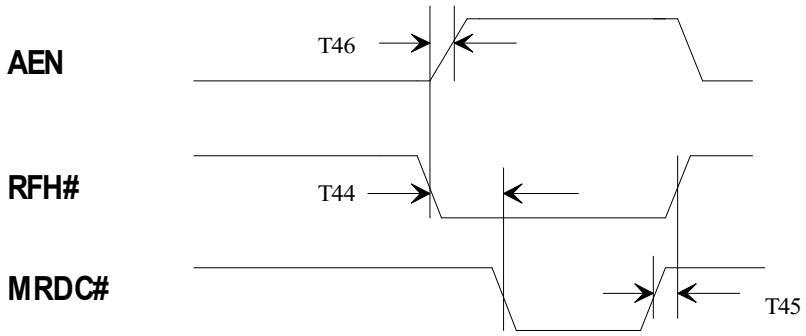


Figure 1.25

4.

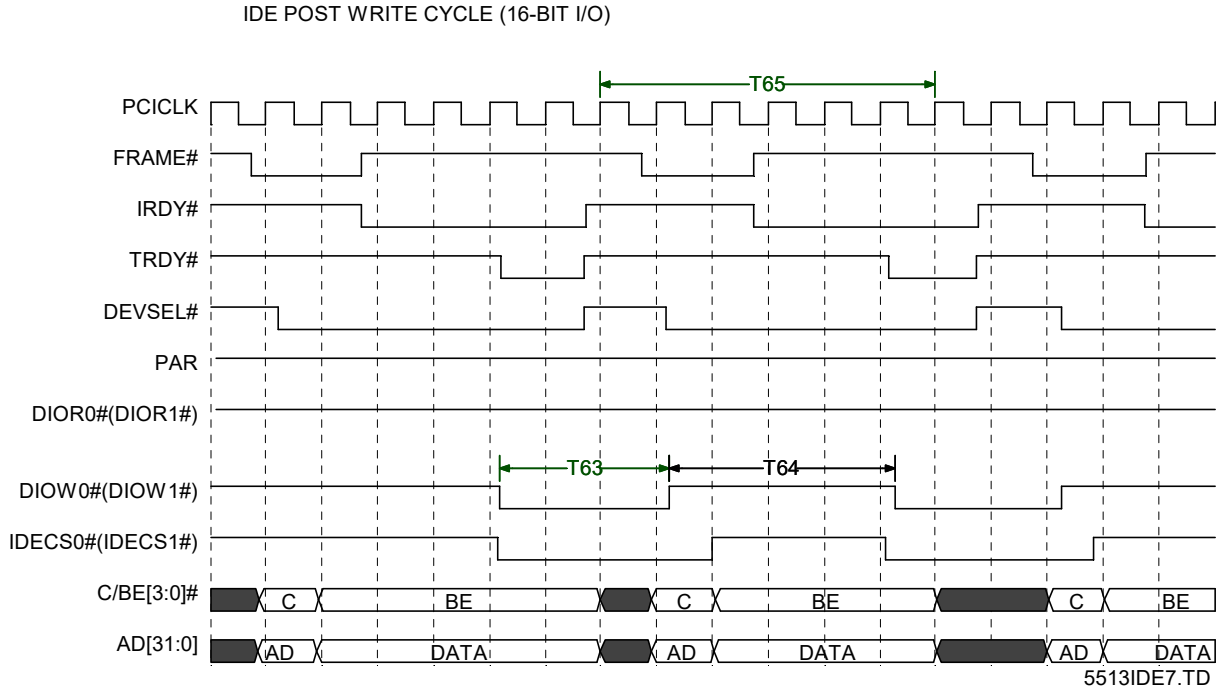


Figure 1.26 IDE POST Write Cycle (16-Bit I/O)

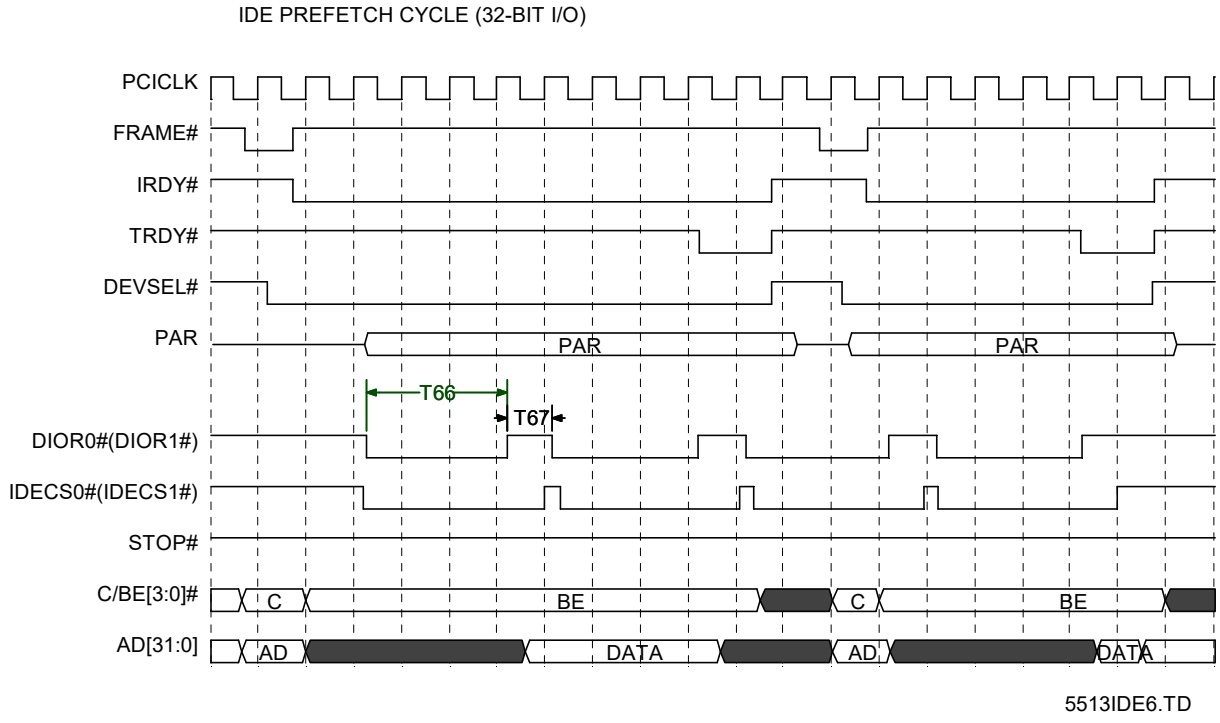


Figure 1.27 IDE Prefetch Cycle (32-Bit I/O)

4.

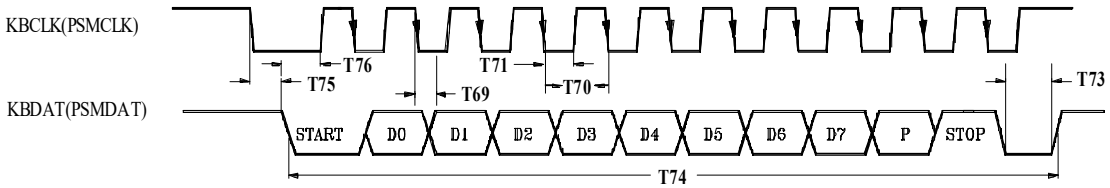


Figure 1.28 Send Data to Keyboard (PS/2 mouse)

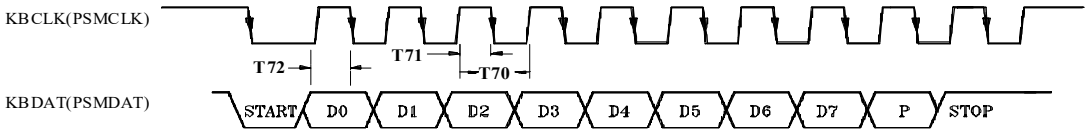


Figure 1.29 Receive Data from Keyboard (PS/2 mouse)

2. Mechanical Dimension

2.1. SiS5513 (208 pins)

QFP208-P (208-Pin Plastic Flat Package) Unit:mm

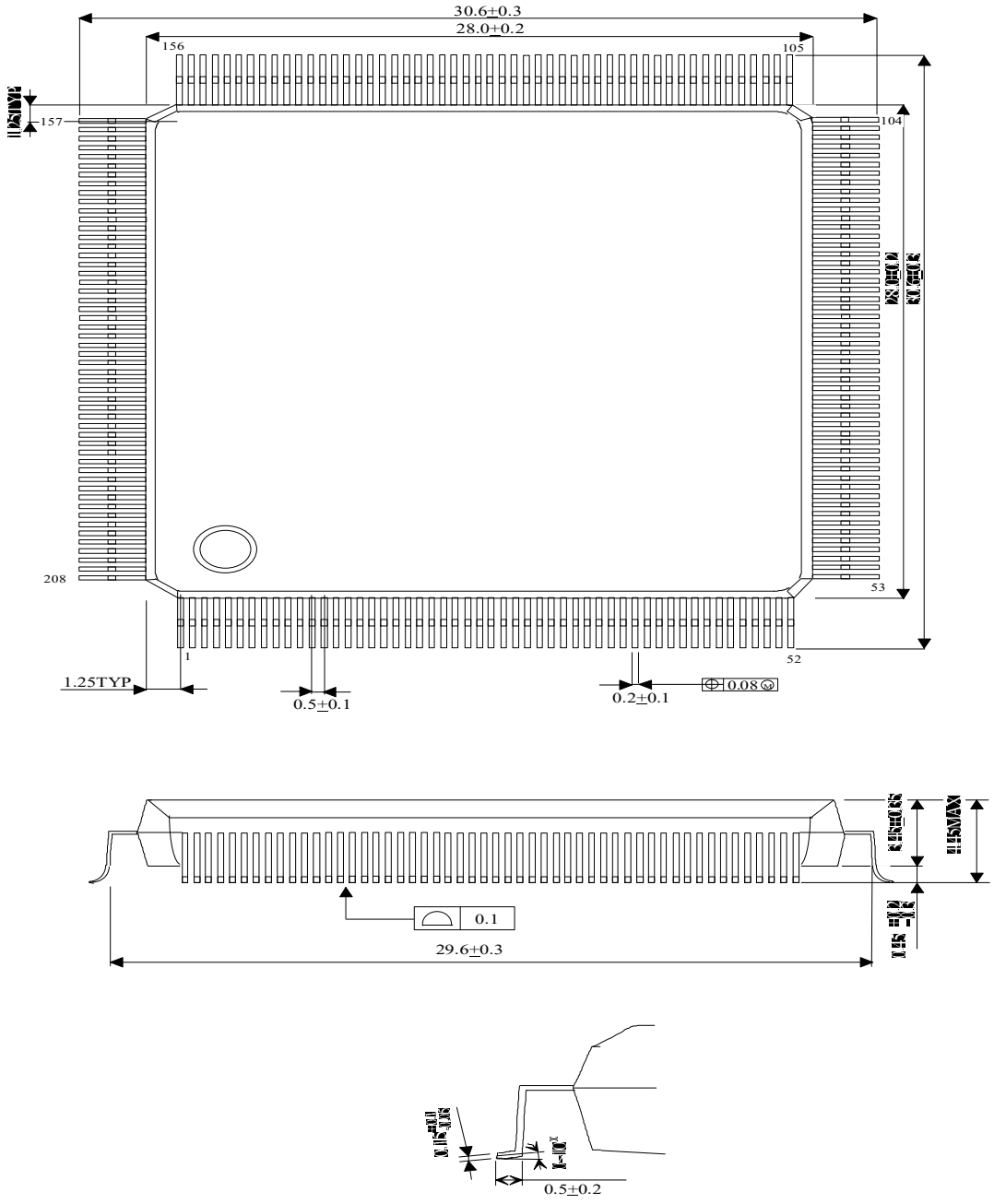


Figure 2.1

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