TVP3409
Data Manual

Video Interface Palette
True-Color CMOS RAMDAC

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TEXAS INSTRUMENTS

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1 Introduction

The TVP3409 is intended to be a direct replacement for the ATT20C409 RAM digital-to-analog converter (RAMDAC). The TVP3409 RAMDAC supports 8-bit multiplexed operation that can be input on 16 pixel terminals. The TVP3409 retains register compatiblity with the ATT20C498 and ATT20C499 devices. The TVP3409 features 24-bit packed pixel modes that provide 24-bit graphics at up to 1024 x 768 screen resolution. Dual clock synthesizers offer two programmable and two fixed frequencies in phase-locked-loop A (PLLA) and one programmable and three fixed frequencies in phase-locked-loop B (PLLB). After reset, the frequencies are:

PLLA: 25.175, 28.322, 50, and 75 MHz

PLLB: 30, 40, 50, and 60 MHz

Easy identification of the RAMDAC allows the video BIOS to determine if a requested mode is available on the hardware being used.

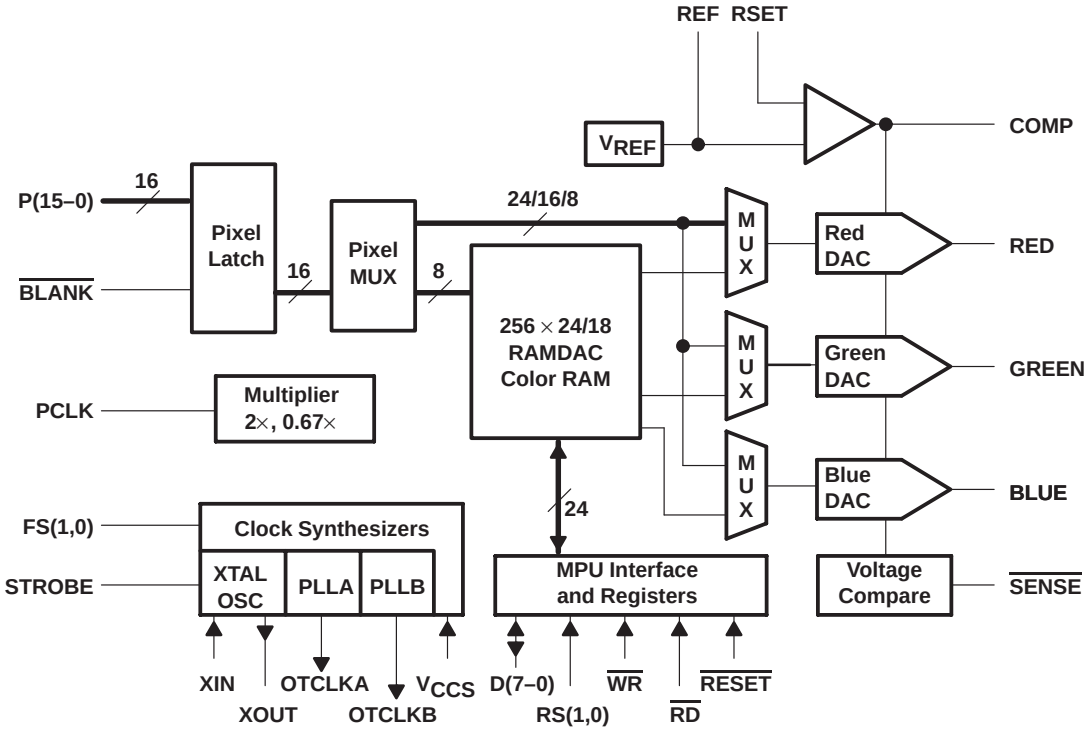
1.1 Features

- Functionally Interchangeable with ATT20C409
- 170/135 MHz (0.8 μm CMOS)
  - 170 MHz 2:1 Multiplex 8-Bit Pseudocolor
  - 73 MHz True Color
- 16-Bit Pixel Port Usable as an 8-Bit Port
  - Compatible With ATT20C490 Using P(7–0)
  - Compatible With ATT20C498 Using P(15–0)
- 9 Software Selectable Color Modes
  - 24-Bit Packed Pixel
  - 24-Bit True Color
  - 8-Bit Pseudocolor
- Dual Programmable Clock Synthesizers
  - Pixel Clock and Memory Clock
  - Reset to 28.322-MHz and 25.175-MHz VGA Frequencies
  - Strobe Input Latches Frequency Select Lines
- On-Chip PLL Clock Doubler
  - 85 MHz input
  - 170 MHz Pixel Output
- 2:1 and 1:1 Pixel Multiplexing
- Power Dissipation of 1.19 W at 135 MHz Typical
- 256 × 24 Color RAM
- Triple 8-Bit Monotonic Digital-to-Analog Converters (DACs)
- Software Compatible With the AT&T ATT20C498/499/409
- 68-Terminal Plastic Leaded Chip Carrier (PLCC) Package

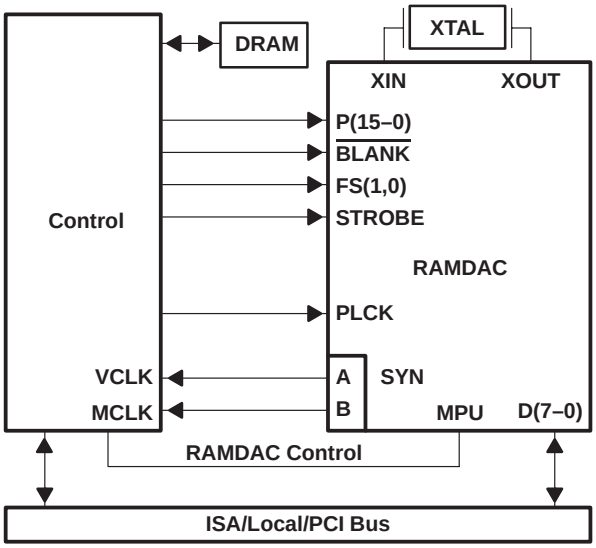
1.2 Applications

- Performance Available With 2M-Byte Frame Buffer (noninterlaced)
  - 1600 × 1280 Resolution, 8 Bits/Pixel, 60 Hz
  - 1024 × 768 Resolution, 16 Bits/Pixel, 100 Hz
  - 800 × 600 Resolution, 24 Bits/Pixel, Unpacked, 75 Hz
  - 800 × 600 Resolution, 24 Bits/Pixel, Packed, 110 Hz
- Additional Performance Available With 3M-Byte Frame Buffer (noninterlaced)
  - 1280 × 1024 Resolution, 16 Bits/Pixel, 60 Hz
  - 1024 × 768 Resolution, 24 Bits/Pixel, Packed, 67 Hz
- True-Color Desktop, PC Add-in Card
- X-Windows Terminals
- Green PCs

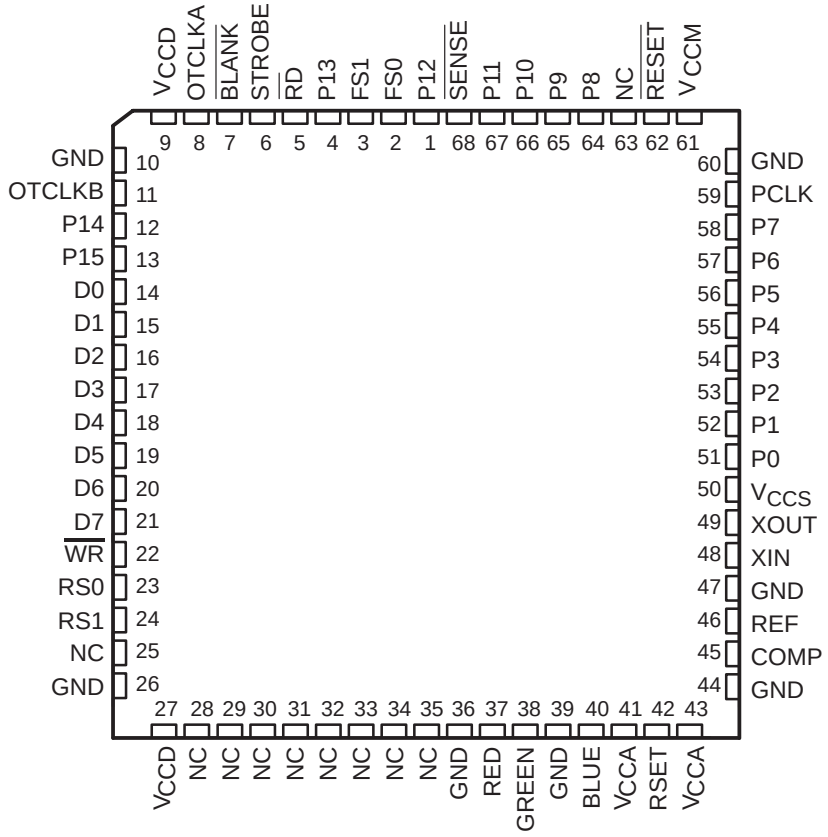
1.3 Functional Block Diagram



1.4 System Block Diagram



1.5 Terminal Assignments



NC – No internal connection

1.6 Ordering Information

TVP3409 – XXX XX

Pixel Clock Frequency Indicator

MUST CONTAIN THREE CHARACTERS:

- 135: 135-MHz pixel clock
- 170: 170-MHz pixel clock

Package

MUST CONTAIN TWO LETTERS:

FN: Plastic Leaded Chip Carrier

1.7 Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{\text{BLANK}}$	7	I	Blank (active low, TTL compatible). $\overline{\text{BLANK}}$ is latched on the rising edge of PCLK. When $\overline{\text{BLANK}}$ is low, the 1.44 mA current source on the analog outputs is turned off. The DACs ignore digital input from memory. In mode 14, pixel data is aligned with the rising edge of PCLK after $\overline{\text{BLANK}}$ rises.
COMP	45		Compensation terminal. Bypass this terminal with an external 0.1 μF capacitor to V_{CC}.
D(7–0)	14–21	I/O	Data bus (TTL compatible). Data is transferred between the data bus and the internal registers under control of the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ signals. In a microprocessor unit (MPU) write operation, D(7–0) is latched on the rising edge of $\overline{\text{WR}}$. To read data D(7–0) from the device, $\overline{\text{RD}}$ must be in an active low state. The rising edge of the $\overline{\text{RD}}$ signal indicates the end of a read cycle. Following the read cycle, the data bus goes to a high-impedance state. Note that for 6-bit operation, color data is contained in the lower six bits of the data bus. D0 is the LSB and D5 is the MSB. When the MPU writes color data, D6 and D7 are ignored. During MPU read cycles, D6 and D7 are a logic 0.
FS(1,0)	2, 3	I	Clock frequency select (TTL compatible). FS(1,0) select the register sets that determine the frequency of the clock synthesizers. FS(1,0) select the register sets when CC0(7) and CC0(3) = 0. When CC0(7) and CC0(3) = 1, bits in the CC register select the register sets.
GND	10, 26, 36, 39, 44, 47, 60		Ground. GND terminals connect to circuit ground.
OTCLKA	8	O	Output clock A (TTL compatible). Output clock from analog PLLA synthesizer.
OTCLKB	11	O	Output clock B (TTL compatible). Output clock from analog PLLB synthesizer.
PCLK	59	I	Pixel clock (TTL compatible). The duty cycle can be 30% to 70%. The rising edge of the pixel clock latches the pixels and the $\overline{\text{BLANK}}$ input.
P(12–13), P(14–15), P(0–7), P(8–11)	1,4, 12, 13, 51–58, 64–67	I	Pixel in (TTL compatible). These terminals are latched on the rising edge of PCLK. Pixels are presented to the DACs as color data in true-color modes and are used as addresses in the pseudocolor mode to look up color data in the color RAM. Unused inputs should be connected to GND.
$\overline{\text{RD}}$	5	I	Read (active low, TTL compatible). When $\overline{\text{RD}}$ is low, data is transfered from the selected internal register to the data bus. RS(1,0) is latched on the falling edge of $\overline{\text{RD}}$.
RED, GREEN, BLUE	37, 38, 40	O	Color analog out. High-impedance current sources that are capable of driving a double-terminated 75-Ω coaxial cable.
REF	46		Voltage reference. REF should be bypassed with an external 0.1 μF capacitor to GND.
$\overline{\text{RESET}}$	62	I	Reset (TTL compatible). This input resets internal registers to 0x00. $\overline{\text{RESET}}$ programs the clock synthesizer register sets to produce 28.322 MHz and 25.175 MHz.
RSET	42	I	Reference resistor. An external resistor (R_{SET}) is connected between the RSET terminal and GND to control the magnitude of the full-scale current (refer to Section 2.6.8, DAC Gain for more information).
RS(1,0)	23, 24	I	Register select (TTL compatible). These inputs are sampled on the falling edge of $\overline{\text{RD}}$ or $\overline{\text{WR}}$ to determine which one of the internal registers is to be accessed.

1.7 Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{\text{SENSE}}$	68	O	Monitor detect (active low, TTL compatible). $\overline{\text{SENSE}}$ is logic 0 when one or more of the RED, GREEN, or BLUE outputs has exceeded the internal voltage reference level of 340 mV ± 70 mV.
STROBE	6	I	Strobe for reference frequency select (TTL compatible). FS(1,0) are connected to an internal transparent latch. When STROBE is high, data can be written to FS(1,0). When STROBE is low, the latch is closed and data cannot be written to FS(1,0). The falling edge of STROBE latches FS(1,0). When STROBE is tied permanently high, care must be taken to ensure that noise does not exist on the FS(1,0) inputs.
V_{CCA}	41, 43		Analog power. V_{CCA} terminals connect to 5 V. These terminals supply the power for the analog DACs and should be connected to a filtered supply plane.
V_{CCD}	9, 27		Digital power. V_{CCD} terminals connect to 5 V. These terminals can be connected to the filtered supply plane or connected to the digital supply plane of the RAMDAC.
V_{CCS}	50		Clock synthesizer power. V_{CCS} connects to 5 V. This can be a separate supply from the RAMDAC (see Appendix A, Application Information).
V_{CCM}	61		Clock multiplier power. V_{CCM} connects to 5 V. This can be a separate supply from the RAMDAC (see Appendix A, Application Information).
$\overline{\text{WR}}$	22	I	Write (active low, TTL compatible). $\overline{\text{WR}}$ controls the data transfer from the data bus to the selected internal register. D(7–0) data is latched at the rising edge of $\overline{\text{WR}}$, and RS(1,0) data is latched at the falling edge of $\overline{\text{WR}}$.
XIN	48	I	Crystal in. XIN is the external crystal or stable frequency source connection to the internal crystal oscillator. The recommended frequency is a 14.318 MHz system clock. When using a crystal, it connects across XIN and XOUT.
XOUT	49	O	Crystal out. XOUT is the external crystal connection to the internal crystal oscillator. All passive components are integrated on-chip to implement a tuned resonant circuit. This terminal should float when using a stable external frequency source connected to XIN.

2 Detailed Description

The TVP3409 RAMDAC is compatible with the architecture of the ATT20C499 and ATT20/21C498 RAMDACs. The TVP3409 contains 24-bit packed pixels on a 16-terminal interface. The device includes dual clock synthesizers which can synthesize a pixel clock and a memory clock from a reference frequency. The device includes a third analog PLL for pixel clock multiplication. Multiplication of 2× or 2/3× the pixel clock is set automatically when certain color modes are programmed. Clock synthesis and clock multiplication reduce the maximum clock speed on the board. The reduced clock speed eases high-speed board design and FCC certification. Table 2–1 lists the feature comparisons and functional differences between the TVP3409/ATT20C409, the ATT20C499, and the ATT21C498 RAMDACs.

The TVP3409 has been designed to allow a single board layout for assembly using either the TVP3409 or other industry standard 44-terminal PLCC RAMDAC.

The TVP3409 includes simple indexed addressing of all control, test, and identification registers using only two register select terminals. This supplements multiple accesses of the pixel read mask register (RMR) used in this and other devices.

A 14.318 MHz crystal connects across the XIN and XOUT terminals when using the clock synthesizer (see Section 1.4, System Block Diagram). Other input crystal frequencies can be used. When using a reference frequency instead of a crystal, the signal connects to XIN and XOUT floats (disconnected).

Table 2–1. Feature Comparisons and Functional Differences of the TVP3409/ATT20C409, ATT21C498, and ATT20C499

FEATURE	TVP3409/ATT20C409	ATT20C499	ATT21C498
Pixel interface	16 terminals	24 terminals	16 terminals
Packed 24-bit pixels	Yes	Yes	Yes
Clock synthesizers	Dual	Dual	No
Clock multiplication factors	2, 0.67 PCLK (analog)	2, 0.67 PCLK (analog)	2x (digital)
Multiplexer rate for 8-bit pixels	2:1	2:1	2:1
Color modes	9	13	11
Software compatible to ATT20C498	Yes	Yes	Yes
Control registers	CR(1,0), CC0	CR(1,0), CC0	CR0
Clock synthesizer A register set A Read/write access: AA, AB AC, AD	 None Read/Write	 Read Read/Write	 N/A
Clock synthesizer B register set B Read/write access: BA, BB BC, BD	 None None Read/Write	 Read Read/Write Read/Write	 N/A
MSW Terminal	No	Yes	Yes
Package	68 PLCC	68 PLCC	44 PLCC
Manufacturer identification register (MIR) value	MIR = 0x97	MIR = 0x84	MIR = 0x84
Device identification register (DIR) value	DIR = 0x09	DIR = 0x99	DIR = 0x98
Revision identification	No	No	No
Maximum speed (MHz)	170	170	170

2.1 Register Descriptions

The standard register set listed in Table 2–2 is accessed directly using RS(1,0).

Table 2–2. Standard Register Set

RS1	RS0	REGISTER ADDRESSED BY MPU	REGISTER	ACCESS	VGA PORT
L	L	Write-mode address register	WMA	R/W	3C8
L	H	Look-up table data register. This register sends data to RAMDAC color RAM.	LUT	R/W	3C9
H	L	Pixel read mask register	RMR	R/W	3C6
H	H	Read-mode address register	RMA	R/W	3C7

The state machine register set is listed in Table 2–3. The RMR can also be accessed using the state machine by setting CR0(0) = 0. When CR0(0) = 0, the registers can be accessed through the back door using the state machine.

Table 2–3. State Machine Register Set

RS1	RS0	REGISTER ADDRESSED BY MPU	REGISTER	ACCESS	NUMBER OF RMR READS† CR0(0) = 0
H	L	Pixel read mask register	RMR	R/W	1–4
H	L	Control register 0	CR0	R/W	5
H	L	Manufacturer's identification register	MIR	Read	6
H	L	Device identification register	DIR	Read	7
H	L	Reserved	TST	Read	8–10

† This mode is ATT20C498 function compatible and allows access to all ATT20C498 level functionality.

The indexed register set is listed in Table 2–4. Indexed addressing must be used for programming the control register 1 (CR1), the clock control register (CC), and the indexed clock synthesizer configuration registers listed in Table 2–5.

Table 2–4. Indexed Register Set

RS1	RS0	REGISTER ADDRESSED BY MPU	REGISTER	ACCESS	INDEXED ACCESS CR0(0) = 1	NUMBER OF RMR READS† CR0(0) =0
H	L	Control register 0	CR0	R/W	0x01	5
H	L	Manufacturer's identification register	MIR	Read	0x02	6
H	L	Device identification register	DIR	Read	0x03	7
H	L	Reserved	TST	Read	0x04	8–10
H	L	Control register 1	CR1	R/W	0x05	N/A
H	L	Clock synthesizer control register	CC	R/W	0x06	N/A
H	L	Reserved	—	—	0x07–0x0F	—

† This mode is ATT20C498 function compatible and allows access to all ATT20C498 level functionality.

Table 2–5. Indexed Clock Synthesizer Configuration Registers (see Notes 1, 2, and 3)

REGISTER	INDEXED ACCESS CR0(0) = 1	REGISTER ADDRESSED BY MPU	DESCRIPTION
AA0	0x40	Reserved	Reserved
AA1	0x41	Reserved	Reserved
AA2	0x42	Reserved	Reserved
AA3	0x43	Reserved	Reserved
AB0	0x44	Reserved	Reserved
AB1	0x45	Reserved	Reserved
AB2	0x46	Reserved	Reserved
AB3	0x47	Reserved	Reserved
AC0	0x48	Clock A control register 0 of set C	Feedback divider (M)
AC1	0x49	Clock A control register 1 of set C	Reference (N) and postscaler (P) dividers
AC2	0x4A	Clock A control register 2 of set C	Reserved
AC3	0x4B	Clock A control register 3 of set C	Reserved
AD0	0x4C	Clock A control register 0 of set D	Feedback divider (M)
AD1	0x4D	Clock A control register 1 of set D	Reference (N) and postscaler (P) dividers
AD2	0x4E	Clock A control register 2 of set D	Reserved
AD3	0x4F	Clock A control register 3 of set D	Reserved
—	0x50 – 0x5F	Reserved	Reserved
BA0	0x60	Reserved	Reserved
BA1	0x61	Reserved	Reserved
BA2	0x62	Reserved	Reserved
BA3	0x63	Reserved	Reserved
BB0	0x64	Reserved	Reserved
BB1	0x65	Reserved	Reserved
BB2	0x66	Reserved	Reserved
BB3	0x67	Reserved	Reserved
BC0	0x68	Reserved	Reserved
BC1	0x69	Reserved	Reserved
BC2	0x6A	Reserved	Reserved
BC3	0x6B	Reserved	Reserved
BD0	0x6C	Clock B control register 0 of set D	Feedback divider (M)
BD1	0x6D	Clock B control register 1 of set D	Reference (N) and postscaler (P) dividers
BD2	0x6E	Clock B control register 2 of set D	Reserved
BD3	0x6F	Clock B control register 3 of set D	Reserved
—	0x70–0x7F	Reserved	Reserved

NOTES: 1. RS1 = 1 and RS0 = 0
2. Access = R/W
3. For RMR reads CR0(0) = 0 is not applicable.

2.2 Internal Register Set

The TVP3409 is designed to support enhanced features in a VGA-compatible architecture. A typical VGA system only supports RS0 and RS1 register select signals. With two register select lines, access to four registers is provided (see Table 2–2). In order to provide enhanced features, additional register locations are required (see Table 2–4 and Table 2–5) in the VGA-accessible register space.

To provide additional registers, two more addressing schemes have been added. The first scheme uses a back door. The back door provides access to a control register (CR0), a manufacturer's identification register (MIR), and a device identification register (DIR). The back door is opened by sequential reads to the pixel read mask register (RMR). The pixel read mask register was chosen because it is not often used in normal VGA operation.

The second method is indirect indexed addressing. Indexed addressing can be used to access the RMR, CR0 (when CR0(0) = 1), MIR, DIR, TST, CR1, CC and the registers in Table 2–5. Indexed addressing is the only way to read or write CR1, CC, and the registers in Table 2–5.

To use this method, set CR0(0) = 1 using the back door (multiple accesses to the RMR). Write the address register (WMA) with the address of the register to be read or written. The index of the registers accessible indirectly are listed in the indexed access column in Tables 2–4 and 2–5. Perform a read or write operation when RS(1,0) = 10. The value is read from or written to the register indexed by the contents of the address register.

2.2.1 Write-Mode Address Register (WMA)

This register holds an 8-bit value that is used as an index when writing to the look-up table (LUT) data register or extended indexed registers. For the LUT data register, this register points to one of the 256 RAMDAC color RAM locations. Each of the RAMDAC color RAM locations are 24-bits wide (8-bits read, 8-bits green and 8-bit blue). To write all 24-bits of a RAMDAC color RAM location, three successive writes are made to the same address. After the sequence of three writes is completed, the 24-bit value is transferred to the RAMDAC color RAM.

The LUT and RMR registers listed in Table 2–6 apply only in the 8-bit modes.

Table 2–6. Standard Register Set

REGISTER	REGISTER TYPE	7	6	5	4	3	2	1	0
WMA	Read Write	A7	A6	A5	A4	A3	A2	A1	A0
LUT	Read Write	D7	D6	D5	D4	D3	D2	D1	D0
RMR	Read Write	M7	M6	M5	M4	M3	M2	M1	M0
RMA	Read Write	A7	A6	A5	A4	A3	A2	A1	A0

This register is only used while writing to the LUT data register or reading or writing the extended indexed registers. After this register is set to the desired index, MPU data can be written to the LUT data register or register values can be written to extended indexed registers. The WMA register is autoincrementing when writing to the LUT. When three writes to the LUT data register are complete, the LUT data register data is written to the RAMDAC color RAM and the WMA register increments by one. For this reason, the WMA should be written every time extended indexed registers are accessed.

2.2.2 Read-Mode Address Register (RMA)

This register holds an 8-bit value that is used as an index when reading from the LUT data register or reading or writing the extended indexed registers. To read all 24-bits of a RAMDAC color RAM location, three successive reads are made to the same address.

This register is autoincrementing when reading the LUT. When written, the RMA reads the RAMDAC color RAM data into the LUT data register then the RMA increments by one. When the three reads from the LUT data register are complete, the device transfers new RAMDAC color RAM data at the RMA address into the LUT data register and the RMA increments by one again. When using the RMA for access to the indexed registers, write a value one less than the desired index. The RMA register increments by one before using the index to access the information being read or written.

2.2.3 Look-Up Table Data Register (LUT)

This register is the data port through which reads and writes are made to the RAMDAC color RAM. The write-mode address register or read-mode address register specifies which RAMDAC color RAM location is to be accessed. This register is an 8-bit port to a 24-bit location. Three accesses are needed to read or write the LUT data register. Because both the write-mode address and read-mode address registers are autoincrementing, accesses to this port should be made three at a time to avoid leaving a partially read or written LUT data register. A partially written data register is not transferred to the RAMDAC color RAM. The blue value must be written before the RAMDAC color RAM is updated.

2.2.4 Pixel Read Mask Register (RMR)

The contents of the RMR can be accessed by the MPU at any time and are not initialized on power up. The RMR bits are logically ANDed with the 8-bit pixels in pseudocolor mode. In true-color modes, pixels are not modified by the RMR. A logic one stored in a data bit of the RMR leaves the corresponding bit in the pixel unchanged. A logic 0 in the RMR sets the pixel bit to 0. Bit D0 of the RMR corresponds to pixel bit P0.

Reading the RMR four times without accessing another RAMDAC register directs the next (fifth) read or write access to control register 0. The sixth consecutive read from the RMR returns the MIR. The seventh consecutive read from the RMR returns the DIR (see Table 2–7).

Table 2–7. Accessing the RMR Enables Indirect Access of CR0, MIR, and DIR

RMR READ NO.	REGISTER NAME	REGISTER TYPE	7	6	5	4	3	2	1	0
5	CR0	Read Write	CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
6	MIR	Read Only	1	0	0	0	0	1	0	0
7	DIR	Read Only	0	0	0	0	1	0	0	1

The eighth, ninth, and tenth consecutive reads from the RMR return don't care values. These states are defined in the back-door state machine to maintain compatibility with the ATT20C409, ATT20C499, and ATT20C498 test registers. These test registers are not being implemented in the TVP3409 and, therefore, do not return usable information (see Figure 2–1).

2.2.5 Manufacturer's Identification Register (MIR)

This 8-bit register contains an 8-bit value to identify the manufacturer of the RAMDAC. The MIR is read by reading the RMR six times without accessing any other RAMDAC register. The first four reads return the contents of the RMR. The fifth read returns the CR0 contents. The sixth read returns the MIR contents (97 hex). The seventh read returns the DIR contents.

2.2.6 Device Identification Register (DIR)

This 8-bit register contains an 8-bit value to identify the type of RAMDAC. The DIR is read by reading the RMR seven times without accessing any other RAMDAC register. The TVP3409 returns the value 09 hex.

2.2.7 Control Register 0 (CR0)

Control register 0 is written to or read by the MPU. CR0 is not initialized at power on. CR0 bit 0 is the least significant bit (LSB) in the control register and corresponds to D0 of the MPU port. Table 2–8 defines the bits of the control register.

CR0 bits (7–4) determine the color mode as shown in Table 2–17.

Setting CR0(3) to a 1 places the RAMDAC in power-down mode. In the power-down state, the device retains the information in the color look-up table. Access to the color look-up table is disabled during the power-down mode. The internal registers can be written to while the device is in the power-down mode. The crystal oscillator and clock synthesizers are powered down separately.

The CR0(2) bit is reserved.

The 8/6 select bit CR0(1) determines whether the MPU port reads and writes 8 bits or 6 bits of color data to the color look up table RAM. In 6-bit mode, color data is on the lower 6 bits of the data bus, with D0 being the LSB and D5 the most significant bit (MSB) of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 are logic 0. Note that in the 6-bit mode, the full scale output current is about 1.5% lower than when in the 8-bit mode. This is a result of the two LSBs of each 8-bit DAC always being a logic 0 in the 6-bit mode. In the 8-bit color mode, bit D0 is the color data LSB and bit D7 is the MSB.

The CR0(0) bit controls access to the extended registers.

This register is operational upon power up. It can be read or written to by the MPU at any time and it is not initialized. All bits are set to 0 upon asserting $\overline{\text{RESET}}$. To read from or write to this register, use the internal state machine for access by reading the RMR (see Table 2–3).

Table 2–8. Control Register 0

BIT	NAME	DESCRIPTION
CR0(7–4)	Color Mode	These bits control the color modes (see Tables 2–17).
CR0(3)	Power Down (RAMDAC)	Logic 0: Normal operation Logic 1: Sleep CR0(3) powers the RAMDAC off. The device does not power up for MPU updates. The data in the LUT is maintained during power down. Internal registers can be accessed while the RAMDAC is powered down. CR1(3,2) powers down the clock synthesizers (for green PC compatibility).
CR0(2)	Reserved	
CR0(1)	8/6 Select	Logic 0: 6-bit data to the DAC Logic 1: 8-bit data to the DAC A logic 0 specifies 6 bits per DAC operation (256K possible colors). A logic 1 specifies 8 bits per DAC operation (16M possible colors).
CR0(0)	Extended Register Enable (Indirect or Indexed Access)	Logic 0: Index accesses disabled to extended registers. Logic 1: Index accesses enabled to extended registers. Bit 0 controls access to the extended registers. When bit 0 is a logic 0, access to the extended registers is enabled by multiple accesses to the RMR (state machine addressing). This does not allow access to CR1, CC, or the clock configuration registers. When this bit is a logic 1, all extended registers can be accessed with indexed addressing using the WMA or RMA register as an address pointer and RS(1,0)= 10 for the data register.

2.2.8 Control Register 1 (CR1)

Control register 1 is operational on power up. The control register can be read from or written to by the MPU at any time and is not initialized. All bits are set to 0 upon asserting RESET. To read or write this register, set bit CR0(0) = 1, write 0x05 to the WMA, and set RS(1,0) = 10. This register can be accessed by using indexed addressing (see Table 2–4). Table 2–9 defines the bits of the control register.

CR1(4) enables the blank pedestal.

CR1(3) powers down clock synthesizer A.

CR1(2) powers down clock synthesizer B.

CR1(1) disables the SENSE terminal.

CR1(0) is reserved. Bit 0 always returns a 0 regardless of what value is written. CR1(0) is the LSB and corresponds to D0 on the MPU port.

Table 2–9. Control Register 1

BIT	NAME	DESCRIPTION
CR1(7)	Reserved	
CR1(6,5)	Reserved	
CR1(4)	Blank Pedestal Enable	Logic 0: No blank pedestal. Logic 1: Blank pedestal enabled. CR1(4) controls whether the BLANK terminal shuts off a 7.5 IRE† current source on R, G, and B when blanking is asserted. For VGA compatibility, write a 0 to bit 4.
CR1(3)	OTCLKA Synthesizer Power Down	Logic 0: OTCLKA synthesizer enabled. Logic 1: OTCLKA synthesizer powered down and output is 3-stated. A logic 1 disables clock synthesizer A (PLLA). This bit should be a logic 1 to achieve the lowest power state for the device. Set this bit to a logic 1 when not using clock synthesizer A.
CR1(2)	OTCLKB Synthesizer Power Down	Logic 0: OTCLKB synthesizer enabled. Logic 1: OTCLKB synthesizer powered down and output is 3-stated. A logic 1 disables clock synthesizer B (PLLB). Bit 2 should be a logic 1 to achieve the lowest power state for the device. Set bit 2 to a logic 1 when not using clock synthesizer B.
CR1(1)	SENSE Disable	Logic 0: SENSE terminal enabled. Logic 1: SENSE terminal disabled and output is 3-stated. A logic 0 enables the SENSE terminal to output the SENSE signal.
CR1(0)	Reserved	This bit always returns a 0 without regard to what was written.

† Institute of Radio Engineers (IRE)

2.2.9 Clock Synthesizer Control Register (CC)

The clock synthesizer control register is written to or read by the MPU and it is not initialized at power on. Table 2–10 defines the bits of the clock synthesizer control register.

CC(0) is the LSB and corresponds to D0 on the MPU port.

CC(7) determines whether the frequency select input terminals FS(1,0) or the clock synthesizer control register bits CC(5,4) control the frequency selection for clock synthesizer A (PLLA) and OTCLKA.

CC(6) is reserved. This bit can be read which returns the value written, but it does not affect the function of the device.

CC(3) determines whether the frequency select input terminals FS(1,0) or the clock synthesizer control register bits CC(1,0) control the frequency selection for clock synthesizer B (PLLB) and OTCLKB.

CC(2) is reserved. This bit can be read which returns the value written, but it does not affect the function of the device.

This register is operational on power up. It can be read or written to by the MPU at any time and it is not initialized. All bits are set to zero upon asserting $\overline{\text{RESET}}$. To read or write this register, set bit CR0(0) = 1, write 0x06 to the WMA, and set RS(1,0) = 10. This register cannot be accessed by state machine addressing (see Table 2–4).

Table 2–10. Clock Synthesizer Control Register

BIT	NAME	DESCRIPTION
CC(7)	Control Option Clock A Select	Logic 0: Input terminals FS(1,0) control clock A Logic 1: Bits CC(5,4) control clock A Bit 7 determines control of clock synthesizer A.
CC(6)	Reserved	Bit 6 is reserved. Bit 6 can be read which returns the value written, but does not affect the function of the device.
CC(5,4)	Register Set Select (for Clock A)	Logic 00: Reserved Logic 01: Reserved Logic 10: Register set C Logic 11: Register set D Bits 5 and 4 select which register set configures clock A.
CC(3)	Control Option Clock B Select	Logic 0: Input terminals FS(1,0) control clock B. Logic 1: Bits CC(1,0) control clock B. Bit 3 determines control of clock synthesizer B.
CC(2)	Reserved	Bit 2 is reserved. Bit 2 can be read which returns the value written, but does not affect the function of the device.
CC(1,0)	Register Set Select (for Clock B)	Logic 00: Reserved Logic 01: Reserved Logic 10: Reserved Logic 11: Register set D Bits 1 and 0 select which register set configures clock B.

2.2.10 Clock Synthesizer Register Sets

The clock synthesizer register sets determine the frequencies of clock synthesizer A (PLLA, OTCLKA) and clock synthesizer B (PLLB, OTCLKB) for a given reference frequency. There are four sets for OTCLKA and four sets for OTCLKB. A set of registers is chosen by toggling either the FS(1,0) terminals or the CC(5,4) or CC(1,0) bits.

Each register set consists of four registers. The four registers have information affecting seven functions of the clock synthesizer. The feedback divider term (M) together with the reference divider term (N) and postscaler term (P) determine the frequency according to equation 1 in Section 2.6.4.1, Determining Output Frequency. The M term is 8 bits, the N term is 6 bits, and the P term is 2 bits.

Table 2–12 and Table 2–14 show the fields associated with each term. The third and fourth registers are reserved and can be read which returns the values written, but does not affect the function of the device.

The clock synthesizer A register sets are operational on power up. They can be read from or written to by the MPU at any time and they are not initialized. All of the registers are reset to produce the frequencies in Table 2–19 upon asserting RESET. To read from or write to these registers, set bit CR0(0) = 1, write 0x40 – 0x4F to the WMA, and set RS(1,0) = HL. These registers cannot be accessed by state machine addressing (see Table 2–5 and Table 2–19).

Table 2–11. Clock Synthesizer A Parameters

REGISTER	CONTROL SET	ACCESS	REGISTER NUMBER	DESCRIPTION	DEFAULT FREQUENCY
Reserved	A CC(5,4) = 00 or FS(1,0) = LL	None	0		25.057 MHz
Reserved			1		
Reserved			1		
Reserved	B CC(5,4) = 01 or FS(1,0) = LH	None	0		28.189 MHz
Reserved			1		
Reserved			1		
AC0(7–0)	C CC(5,4) = 10 or FS(1,0) = HL	Read or Write	0	Feedback divider term (M)	50.114 MHz
AC1(7,6)			1	Postscaler divider term (P)	
AC1(5–0)			1	Reference divider term (N)	
AD0(7–0)	D CC(5,4) = 11 or FS(1,0) = HH	Read or Write	0	Feedback divider term (M)	75.170 MHz
AD1(7,6)			1	Postscaler divider term (P)	
AD1(5–0)			1	Reference divider term (N)	

Table 2–12. Clock Synthesizer A Register Set Fields

CLOCK REGISTER 0, BITS AND FIELDS								CLOCK REGISTER 1, BITS AND FIELDS							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
M(7–0)†								P(1,0)‡		N(5–0)§					

CLOCK REGISTER 2, BITS AND FIELDS								CLOCK REGISTER 3, BITS AND FIELDS							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Reserved								Reserved							

† M(7–0), 8 bits, integer from 0 to 255 (2 is added to this value)
‡ P(1,0), 2 bits, integer from 0 to 3 (these bits indicate the power of 2. See equation 1 in Section 2.5.4.1, Determining Output Frequency)
§ N(5–0), 6 bits, integer from 0 to 63 (2 is added to this value)

The clock synthesizer B register sets are operational on power up. They can be read from or written to by the MPU at any time. All of the registers are reset to produce the frequencies in Table 2–19 upon asserting $\overline{\text{RESET}}$. To read from or write to these registers, set bit CR0(0) = 1, write 0x60 – 0x6F to the WMA, and set RS(1,0) = HL. These registers can be accessed by indexed addressing (see Table 2–5).

Table 2–13. Clock Synthesizer B Parameters

REGISTER	CONTROL SET	ACCESS	REGISTER NUMBER	DESCRIPTION	DEFAULT FREQUENCY
Reserved	A	None	0		29.979 MHz
Reserved	CC(1,0) = 00 or FS(1,0) = LL		1		
Reserved			1		
Reserved	B	None	0		40.091 MHz
Reserved	CC(1,0) = 01 or FS(1,0) = LH		1		
Reserved			1		
Reserved	C	None	0		50.114 MHz
Reserved	CC(1,0) = 10 or FS(1,0) = HL		1		
Reserved			1		
BD0(7–0)	D	Read or Write	0	Feedback divider term (M)	59.957 MHz
BD1(7,6)	CC(1,0) = 11 or FS(1,0) = HH		1	Postscaler divider term (P)	
BD1(5–0)			1	Reference divider term (N)	

Table 2–14. Clock Synthesizer B Register Set Fields

CLOCK REGISTER 0, BITS AND FIELDS								CLOCK REGISTER 1, BITS AND FIELDS							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
M(7–0)†								P(1,0)‡		N(5–0)§					

CLOCK REGISTER 2, BITS AND FIELDS								CLOCK REGISTER 3, BITS AND FIELDS							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Reserved								Reserved							

† M(7–0), 8 bits, integer from 0 to 255 (2 is added to this value)
‡ P(1,0), 2 bits, integer from 0 to 3 (these bits indicate the power of 2)
§ N(5–0), 6 bits, integer from 0 to 63 (2 is added to this value)

2.3 Reset State

The following information describes how the RAMDAC operates after the $\overline{\text{RESET}}$ terminal has been toggled low.

When $\overline{\text{RESET}}$ is asserted, OTCLKA outputs 25.057 MHz (VGA graphics frequency), 28.189 MHz (VGA text frequency), 50.114 MHz, or 75.170 MHz depending on the values of the frequency select terminals FS(1,0) or the clock synthesizer control register bits CC(5,4) (see Table 2–19).

When $\overline{\text{RESET}}$ is asserted, OTCLKB outputs 29.979, 40.091, 50.114, or 59.957 MHz depending on the values of the frequency select terminals FS(1,0) or the clock synthesizer control register bits CC(1,0).

During normal operation, the clock synthesizers can be programmed to any frequency within the capability of the device. The clock synthesizers can be powered down and the outputs are then 3-stated.

When $\overline{\text{RESET}}$ goes inactive, the RAMDAC loads each internal register with 0x00 unless otherwise noted. The internal registers can be written through the MPU port even though the RAMDAC is not being clocked. The internal pixel color RAM cannot be written unless the RAMDAC is clocked. The RAMDAC resets as follows:

1. The crystal oscillator is enabled.
2. The 6-bit DACs (VGA, SVGA) are reset.
3. The device is configured in 8-bit pseudocolor mode.
4. The frequency select terminals FS(1,0) determine the frequencies of both synthesizer A and B.
5. Synthesizer A runs at one of four preprogrammed frequencies (25.057, 28.189, 50.114, and 75.170 MHz) until register sets AC0–AC2 or AD0–AD2 are changed and selected.
6. Synthesizer B runs at one of four preprogrammed frequencies (29.979, 40.091, 50.114, and 59.957 MHz) until register sets BC0–BC2 or BD0–BD2 are changed and selected.

2.4 Programming From Reset

The RAMDAC can be configured by programming the internal registers. To program all of the internal registers, the device needs to have indexed addressing enabled. Indexed addressing is enabled by setting bit CR0(0) = 1. Bit CR0(0) is set to 1 using an addressing mode available through the RMR. Using the RMR to address internal registers allows backward compatibily with only four hardware addressable registers. The following sequence of steps using DOS debug allows the indexed addressing mode to be enabled. Indexed addressing mode can also be accomplished easily in a programming language such as C.

1. Read the current state of command register 0 (CR0) with the RMR.
   –o 3C8 00 Write to port 3C8 (WMA) with the value 0x00
   Resets backdoor state machine
   –i 3C6 Read port 3C6 (RMR)
   Contents of the RMR
   –i 3C6 Contents of the RMR
   –i 3C6 Contents of the RMR
   –i 3C6 Contents of the RMR
   –i 3C6 Contents of the command register 0 (CR0)
2. Enable indexed programming by setting CR0(0) = 1.
   –o 3C8 00 Reset backdoor state machine
   –i 3C6 Contents of the RMR
   –i 3C6 Contents of the RMR
   –i 3C6 Contents of the RMR
   –i 3C6 Contents of the RMR
   –o 3C6 xxxx xxx1 (binary) Set CR0(0) =1
3. Indexed programming is now enabled.
   3C8 is the address port
   3C6 is the data port
4. To exit indexed programming, set CR0(0) = 0.
   –o 3C8 01 Select CR0
   –i 3C6 Read CR0
   –o 3C6 xxxx xxx0 (binary) Reset bit 0, leave other bits programmed as they are.

2.5 Changing Clock Frequencies

This section describes how to change the internal synthesizer frequencies without corrupting the on-chip pixel color RAM.

1. Power down the chip by setting CR0(3) = 1. The registers retain their values and can be read from and written to. The RAM cannot be read from or written to during this time.
2. Program a delay of approximately 300 µs. The delay varies depending on the noise in the system and the signals connected to the RAMDAC.
3. Change the synthesizer register settings and/or change the frequency select bits/lines.
4. Program another delay of approximately 300 µs. This varies depending on the noise in the system and the signals connected to the RAMDAC.
5. Power up the chip by setting CR0(3) = 0. The registers retain their values and can be read from and written to. The RAM can now be read from or written to.

The data (colors) integrity of the pixel color RAM should be intact. To add further protection to the values in the color RAM, copy the pixel color RAM to system memory before changing clock frequencies. Copy the values back after the frequency has settled.

2.6 Functional Descriptions

The following sections contain functional descriptions of the device.

2.6.1 State Machine Access to Extended Registers

State machine access to the extended registers is provided to give backward compatibility to the ATT20C498 RAMDAC. Indirect access to the extended registers is described by a state diagram shown in Figure 2–1. Table 2–16 indicates the register access in each state. The extended registers accessible in this manner are CR0, MIR, and DIR.

To read CR0, read the RMR five times. The fifth read returns the contents of CR0. To write CR0, read the RMR four times. This sets an internal flag allowing access to control register 0. The next write is directed to control register 0. The MIR and DIR registers are accessed in a similar manner as shown by Figure 2–1. The sixth read of the RMR returns the contents of the MIR (read only). The seventh read of the RMR returns the contents in the DIR (read only). The eighth, ninth, and tenth reads of the RMR return don't care values and are required for compatibility with the ATT20C4xx series devices. An additional read resets the state machine back to state 0.

Table 2–15 indicates I/O operations that reset the state machine to state 0. Any write operation resets the state machine to state 0.

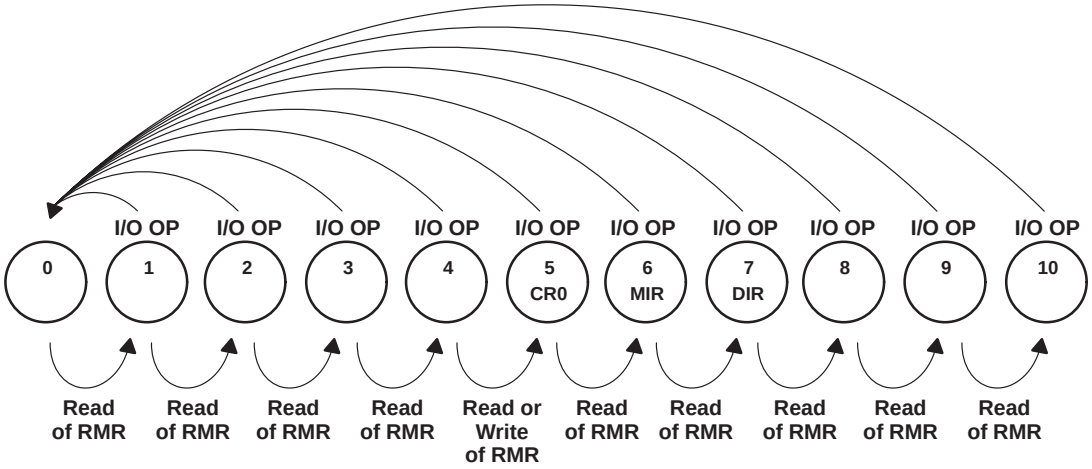
Table 2–15. I/O Transition and Logic-Level Combinations that Reset the State Machine to State 0

$\overline{WR}$	RS1	RS0
↓	L	L
↓	L	H
↓	H	L
↓	H	H

2.6.2 Indexed Access to Extended Registers

Indexing provides another way to access the extended registers and it is the only way to access CR1, CC, and the clock synthesizer register sets (see Table 2–5). CR0 must be accessed through state machine addressing to set bit 0 to a 1 before indexed accessing can be used. The CR0, MIR, and DIR registers can be accessed either by the RMR or by indexing.

To use this method, set CR0(0) = 1 using state machine accessing (multiple accesses to the RMR). Write the write-mode address register (WMA) with the address of the register to be read or written. Set RS(1,0) = HL. Perform a read or write operation. The value is read from or written to the desired register. The address register does not increment automatically. When the RMA is used for indexing, write a value 1 less than the desired value. The RMA increments before being used as an index. The addresses of the registers accessible by indexing are listed in the indexed access column in Table 2–4 and Table 2–5.



NOTE A: I/O OP is any I/O write to 3C6, 3C7, 3C8, or 3C9 (see Table 2–2).

Figure 2–1. State Diagram for Indirect Access to Extended Registers

Table 2–16. Access to CR0, MIR, and DIR Registers

STATE TABLE		
STATE	**STATE ENTRY CONDITIONS**	**STATE ACTIVITY**
0	Any I/O write	Normal I/O access
1	Read of RMR while in state 0	Normal I/O access
2	Read of RMR while in state 1	Normal I/O access
3	Read of RMR while in state 2	Normal I/O access
4	Read of RMR while in state 3	Normal I/O access
5	Read or write of RMR while in state 4	I/O access to CR0
6	Read of RMR while in state 5	Returns MIR, 97 hex
7	Read of RMR while in state 6	Returns DIR, 09 hex
8	Read of RMR while in state 7	Normal I/O access
9	Read of RMR while in state 8	Normal I/O access
10	Read of RMR while in state 9	Normal I/O access

2.6.3 Color Modes

The TVP3409 provides nine different color modes that are selectable by programming control register 0 bits CR0(7–4) (see Table 2–17).

In true color modes with multiple or fractional clocks per pixel, a clock multiplier provides the internal load pulse that latches the data into a 16- or 24-bit pixel. True color modes bypass the look-up table and are not gamma corrected. The modes are discussed in the following sections.

2.6.3.1 Mode 0

Mode 0 displays data formatted in 8-bit pseudocolor. Mode 0 is selected by setting control register 0 bits CR0(7–4) to 0000. Mode 0 ignores the P(15–8) inputs (see Figure 2–2).

2.6.3.2 Mode 1

Mode 1 displays data formatted for 15-bit per pixel true color (5–5–5). It is selected by setting control register 0 bits CR0(7–4) to 0001. Mode 1 uses all P(15–0) inputs.

2.6.3.3 Mode 2

Mode 2 accepts two 8-bit pseudocolor pixels on each clock. It is selected by setting control register bits CR0(7–4) to 0010. The internal clock doubler outputs the pixels at twice the PCLK frequency. This allows the RAMDAC to output 8-bit pseudocolor pixels at 135 MHz with 67.5 MHz data rates. Mode 2 uses all P(15–0) inputs.

2.6.3.4 Mode 3

Mode 3 formats data in 16-bit per pixel true color (5–6–5). It is selected by setting control register 0 bits CR0(7–4) to 0011. Mode 3 uses all P(15–0) inputs (see Figure 2–2).

2.6.3.5 Mode 4

Mode 4 accepts data formatted as 8-bit pseudocolor latched by two pixel clocks as 4-bit nibbles. Latching two nibbles allows backward compatibility to previous RAMDACs. It is selected by setting control register 0 bits CR0(7–4) to 0100. Mode 4 ignores the P(15–4) inputs.

2.6.3.6 Mode 5

Mode 5 accepts a 24-bit pixel formatted as two 16-bit words latched by two pixel clocks. This is not a packed mode. On the second pixel clock the upper byte is ignored. It is selected by setting control register 0 bits CR0(7–4) to 0101. Mode 5 uses all P(15–0) inputs.

2.6.3.7 Mode 6

In mode 6, the 16-bit (5–6–5) pixel is latched in two bytes with two PCLKs. Latching one byte per clock allows backward compatibilty to previous RAMDACs. Mode 6 is selected by setting control register 0 bits CR0(7–4) to 0110. $\overline{\text{BLANK}}$ going high signals that the first pixel information is available on P(15–0). The rising edge of PCLK captures $\overline{\text{BLANK}}$ going high and also captures the LSBs of the pixel information. The LSBs are latched first followed by the MSBs. The LSBs and MSBs follow in succession until $\overline{\text{BLANK}}$ goes low. The LSBs of the DACs are set to logical 0. Mode 6 ignores the P(15–8) inputs.

2.6.3.8 Mode 7

In mode 7 the 24-bit pixel is latched in three bytes with three PCLKs. Mode 7 is selected by setting the control register 0 bits CR0(7–4) to 0111. The pixel information is collected over three rising edges of the pixel clock. $\overline{\text{BLANK}}$ going high signals that the first pixel information is available on P(7–0). P(15–8) are ignored. The rising edge of PCLK that captures $\overline{\text{BLANK}}$ going high also captures the blue information of the first pixel. The blue pixel is latched first followed by the green pixel and red pixel. Blue, green, and red follow in succession until $\overline{\text{BLANK}}$ goes low. Mode 7 ignores the P(15–8) inputs.

2.6.3.9 Modes 8 – 13

Reserved

2.6.3.10 Mode 14

Mode 14 formats data in packed 24-bit per pixel true color (2 pixels for three pixel clocks) using P(15–0) terminals. BGR data (24-bit) are latched every 1 1/2 pixel clocks or two 24-bit pixels every three pixel clocks. The external clock is multiplied by 2/3 by an internal multiplier. Mode 14 is selected by setting control register 0 bits CR0(7–4) to 1110. Mode 14 uses all P(15–0) inputs (see Figure 2–3).

2.6.3.11 Mode 15

Reserved

Table 2–17 details the 16 display formatting modes of the TVP3409. These modes are set by control register 0 bits CR0(7–4). Pixel data inputs are only latched on the rising edge of PCLK. P(7–0) indicates an address for the LUT. In the table, a R, G, or B indicates an input to the DACs, and all R, G, and Bs indicate bypass modes.

Table 2–17. Color Modes

PRIM. MODE NO.	CR0 (7–4)	PRIMARY MODE DESCRIPTION	NO. OF PCLK	PIXEL DATA	
				0 – 7	8 – 15
0	0000	8 Bit	↑	P0 P1 P2 P3 P4 P5 P6 P7	X X X X X X X X
1	0001	15 Bit (5–5–5)	↑	B3 B4 B5 B6 B7 G3 G4 G5	G6 G7 R3 R4 R5 R6 R7 X
2	0010	2× 8 Bit	↑	P0 P1 P2 P3 P4 P5 P6 P7	P0 P1 P2 P3 P4 P5 P6 P7
3	0011	16 Bit (5–6–5)	↑	B3 B4 B5 B6 B7 G2 G3 G4	G5 G6 G7 R3 R4 R5 R6 R7
4	0100	8 Bit	↑↑	P0 P1 P2 P3 X X X X P4 P5 P6 P7 X X X X	X X X X X X X X X X X X X X X X
5	0101	24 Bit True Color	↑↑	B0 B1 B2 B3 B4 B5 B6 B7 R0 R1 R2 R3 R4 R5 R6 R7	G0 G1 G2 G3 G4 G5 G6 G7 X X X X X X X X
6	0110	16 Bit (5–6–5)	↑↑	B3 B4 B5 B6 B7 G2 G3 G4 G5 G6 G7 R3 R4 R5 R6 R7	X X X X X X X X X X X X X X X X
7	0111	24 Bit True Color	↑↑↑	B0 B1 B2 B3 B4 B5 B6 B7 G0 G1 G2 G3 G4 G5 G6 G7 R0 R1 R2 R3 R4 R5 R6 R7	X X X X X X X X X X X X X X X X X X X X X X X X
8	1000	Reserved	–	Reserved	Reserved
9	1001	Reserved	–	Reserved	Reserved
10	1010	Reserved	–	Reserved	Reserved
11	1011	Reserved	–	Reserved	Reserved
12	1100	Reserved	–	Reserved	Reserved
13	1101	Reserved	–	Reserved	Reserved
14	1110	2× 24 Bit True Color Packed	↑↑↑	B0 B1 B2 B3 B4 B5 B6 B7 R0 R1 R2 R3 R4 R5 R6 R7 G0 G1 G2 G3 G4 G5 G6 G7	G0 G1 G2 G3 G4 G5 G6 G7 B0 B1 B2 B3 B4 B5 B6 B7 R0 R1 R2 R3 R4 R5 R6 R7
15	1111	Reserved	–	Reserved	Reserved

NOTE 4: CR0(2) = 1 also causes the C field to be ignored.
The clock multiplier operates in modes 2 and 14. In mode 2 the multiplier doubles the PCLK. In mode 14 the PCLK is multiplied by 2/3.

Table 2–18 details the pixel clock and the pixel rates of the TVP3409 for each speed grade. These modes are set by bits CR(7–4) of control register 0. The table also shows the pipeline delay for each mode.

Table 2–18. Color-Mode Speeds

	TVP3409-170 MHz		TVP3409-135 MHz		
PRIMARY MODE NUMBER	MAX PCLK FREQUENCY (MHz)	PIXEL RATE (MHz)	MAX PCLK FREQUENCY (MHz)	PIXEL RATE (MHz)	PIPELINE DELAY (CLKS)
0	110	110	110	110	6
1	110	110	110	110	6
2	85	170	67.5	135	6
3	110	110	110	110	6
4	110	55	110	55	7
5	110	55	110	55	7
6	110	55	110	55	7
7	110	36	110	36	8
8	–	–	–	–	–
9	–	–	–	–	–
10	–	–	–	–	–
11	–	–	–	–	–
12	–	–	–	–	–
13	–	–	–	–	–
14	110	73	110	73	6
15	–	–	–	–	–

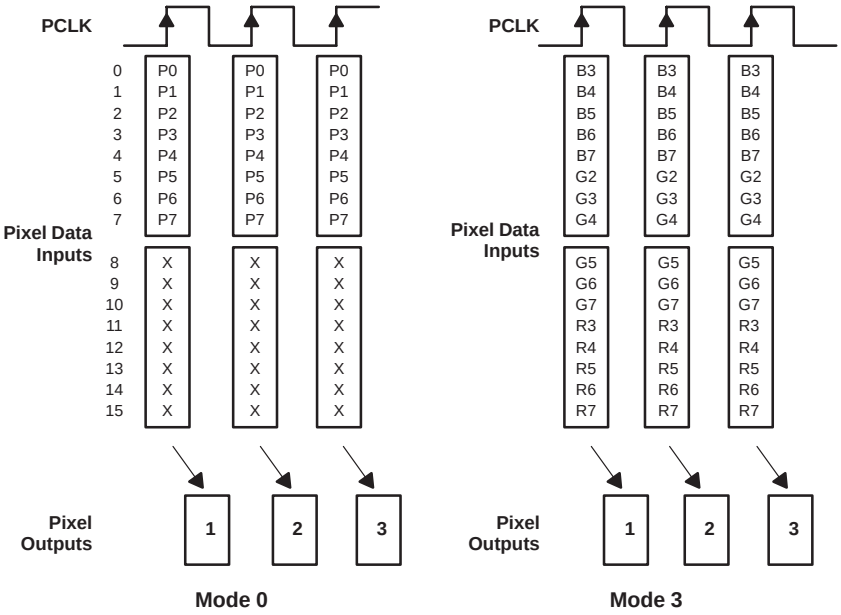
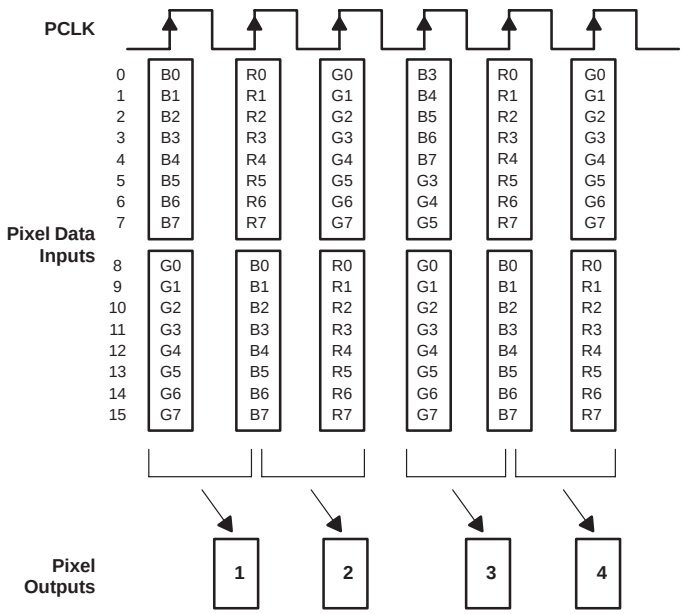


Figure 2–2. Mode 0 and Mode 3 Operation



NOTE A: In this mode two pixels are delivered for every three pixel clocks. The internal clock multiplier factor is 2/3. Thus, a 110-MHz PCLK results in a pixel rate of 73 Mpixels per second.

Figure 2–3. Mode 14, 24 Bits/Pixel, Packed in 16-Terminal Port Operation

2.6.4 Clock Synthesizers

The TVP3409 includes dual programmable clock synthesizers (PLLA, PLLB). The synthesizer signals are output on the OTCLKA and OTCLKB terminals. An internal loop filter eliminates the need for external loop filter components. The clock synthesizers are included to reduce the number of components on the circuit board. This also reduces the high frequency signals on the circuit board by generating them internally.

One synthesizer can generate a pixel clock, the other synthesizer can generate a system or memory clock. The synthesizers reset to a predefined frequency. The reset frequencies for the PLL clocks are shown in Table 2–19.

The synthesizers are programmed by writing to the clock synthesizer control and indexed clock configuration registers. These registers are included in the indexed register map of the RAMDAC (see Table 2–4 and Table 2–5).

The synthesizer includes a crystal oscillator for connection to an external crystal using XIN and XOUT. XIN can also connect to a standard 14.318 MHz system clock. The synthesizer generates any frequency up to the maximum frequency supported by the device. The maximum frequency is achieved by programming the M, N, and P values in the synthesizer loop. Once the digital integer values have been programmed in the register sets (up to four), the clock synthesizer control register bits can switch between the predefined frequencies.

Upon reset, the M, N, and P values are loaded to give the reset frequencies in Table 2–19. The reset frequencies can be changed by reloading new values for M, N, and P.

Table 2–19. Clock Synthesizer Reset Frequencies and FS(1,0) Terminal Logic Levels

OTCLKA			OTCLKB		
FS(1,0)	CC(5,4)	RESET FREQUENCY (MHz)	FS(1,0)	CC(1,0)	RESET FREQUENCY (MHz)
LL	00	25.057	LL	00	29.979
LH	01	28.189	LH	01	40.091
HL	10	50.114	HL	10	50.114
HH	11	75.170	HH	11	59.957

PCLK must meet the minimum high time as specified by the clock period and duty cycle AC specifications in Section 3, Electrical Characteristics. When switching PCLK frequencies, LUT corruption can occur if the PCLK high time is not met. Allow approximately one second after switching frequencies for the synthesizer outputs to settle to a valid clock signal.

The diagram in Figure 2–5 is duplicated for the internal PLL (the TVP3409 has two PLLs on chip).

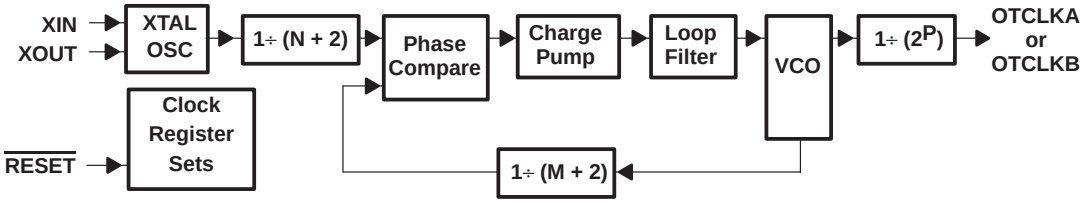


Figure 2–4. Clock Synthesizer Block Diagram

2.6.4.1 Determining Output Frequency

The output frequency, OTCLK, is determined by the following equation.

$$OTCLK = \frac{F_{ref} \times (M + 2)}{(N + 2) \times 2^{P}} \quad (1)$$

Where F_{ref} is the input reference frequency, M is the feedback divider (8-bits), N is the input reference frequency divider (6-bits), and P is the postscaler divider or the exponent setting the output frequency divider (2-bits). Each synthesizer has four selectable frequencies. There are eight sets of M, N, and P registers. These registers are listed in Table 2–5.

Clock synthesizer A (PLLA) and clock synthesizer B (PLLB) can be controlled by frequency select lines or control register bits. Each synthesizer is independently programmed to determine whether the FS(1,0) terminals or the control register bits control its frequency. When both synthesizers are programmed to use the frequency select lines, both synthesizers move in frequency at the same time to their respective register sets A, B, C, or D. When using the control register bits to control frequency, synthesizers A and B move in frequency independently and can move to different register sets. They do not have to both be set to the same register set A, B, C, or D.

See Appendix A, Application Information for component connections and Appendix B, Register Summary for values for the clock synthesizer.

2.6.5 Clock Multiplier

The clock multiplier is a third PLL that is automatically activated when either mode 2 or mode 14 is programmed. In mode 2, the multiplier doubles the PCLK. In mode 14, the PCLK is multiplied by 2/3.

2.6.6 MPU Interface

The TVP3409 supports a standard MPU interface, allowing the MPU direct access to the write-mode address register (WMA), look-up table data register (LUT), pixel read mask register (RMR), or read-mode address register (RMA). As outlined in Table 2–2, the RS(1,0) select inputs indicate whether the MPU is accessing the WMA, LUT, RMR, or RMA. To eliminate the requirement for external address multiplexers, an 8-bit address register addresses the RAMDAC color RAM.

An address register can also be used as an indexed address to access the extended registers inside the TVP3409. For indexed addressing, CR0(0) = 1, RS(1,0) = HL and the RMR becomes the indexed data register.

2.6.6.1 Writing the RAMDAC LUT

The MPU writes the WMA register with the address of the RAMDAC color RAM location to be modified. Using RS(1,0) to select the LUT, the MPU completes three continuous write cycles (6 or 8 bits each of red, green, and blue). Following the blue write cycle, the 3 bytes of color information are concatenated into an 18- or 24-bit word and written to the location specified by the WMA register. The WMA register advances to the next RAMDAC color RAM location which the MPU can modify by simply writing another sequence of red, green, and blue data. A block of color values in successive locations can be written to by writing the start address and performing continuous R, G, and B write cycles until the entire block has been written.

2.6.6.2 Reading the RAMDAC LUT

The MPU loads the RMA register with the address of the RAMDAC color RAM location to be read. The contents of the RAMDAC color RAM at the address specified by the RMA register are copied into the LUT register, and the RMA register advances to the next RAMDAC color RAM location. Using RS(1,0) to select the LUT, the MPU completes three continuous read cycles (6 or 8 bits each of red, green, and blue). After the blue read cycle, the contents of the RAMDAC color RAM at the address specified by the RMA register are copied into the LUT register, and the RMA register advances to the next address. A block of color values in successive locations can be read by writing the start address and performing continuous R, G, and B read cycles until the entire block has been read.

2.6.6.3 Additional Information

Following a blue read or write cycle to color RAM location 0xFF, the address register resets to 0x00.

Operation of the MPU interface occurs asynchronously to the pixel clock. Internal logic synchronizes data transfers between the RAMDAC color RAM and the LUT register. The transfers occur between MPU accesses. As a result, the $\overline{WR}$ and $\overline{RD}$ signals must maintain a logic high for several clock cycles. See Section 3.5.3, Microprocessor Port for the $\overline{RD}$ and $\overline{WR}$ pulse duration times. To eliminate sparkling on the CRT screen during a MPU access to the RAMDAC color RAM, internal logic maintains the previous output color data on the analog outputs while the transfer between RAMDAC color RAM and the LUT register occurs.

To monitor the red, green, and blue read/write cycles, the address register has two additional bits AD(a) and AD(b) that count modulo 3, as shown in Table 2–20. They are reset to 0 when the MPU writes to the address register (WMA or RMA) and are not reset to 0 when the MPU reads the address register. The MPU does not have access to these bits.

Table 2–20. Modulo 3 Counter Operation

AD(b,a)	ADDRESSED BY MPU
00	Red color RAM byte
01	Green color RAM byte
10	Blue color RAM byte

The WMA and RMA address registers increment following a blue read or write cycle. They are accessible to the MPU and are used to address RAMDAC color RAM locations. The MPU can read the address register at any time without modifying its contents or the existing read/write mode. The pixel clock must be active for MPU accesses to the RAMDAC color RAM.

2.6.7 $\overline{\text{SENSE}}$ Output

The $\overline{\text{SENSE}}$ output is a logic 0 when one or more of the red, green, or blue outputs have exceeded the internal voltage reference level (340 mV). This output determines the presence of a CRT monitor, and, with diagnostic code, the difference between a loaded or unloaded RGB line can be discerned. The 340 mV reference has a 70 mV tolerance.

2.6.8 DAC Gain

The device gain from the voltage reference to the DAC output current is shown in Table 2–21. To set the full-scale white current on the DACs while using an internal or external voltage reference, use the formula in equation (2).

$$I_O(\text{mA}) = [V_{ref}(\text{V}) \times 1000 \times \text{K}] / R_{SET}\ (\Omega) \qquad (2)$$

Where:

V_{ref} is the voltage reference in volts
K is the gain constant
R_{SET} is the resistor connected between the RSET terminal and ground.

In this case, a voltage reference of 1.235 V with R_{SET} = 147 Ω and a K factor of 3.17 results in I_O = 26.63 mA. A 6-bit DAC with no blank (H) results in a K factor of 2.1 and I_O = 17.64 mA.

The recommended R_{SET} for RS-343A compatibility applications (doubly terminated 75 Ω) is 147 Ω. The recommended R_{SET} for PS/2™ applications (50 Ω) is 182 Ω.

Table 2–21. Device Gain Factor (K)

$\overline{\text{BLANK}}$	K (8-BIT)	K (6-BIT)
L	2.28	2.26
H	2.12	2.1

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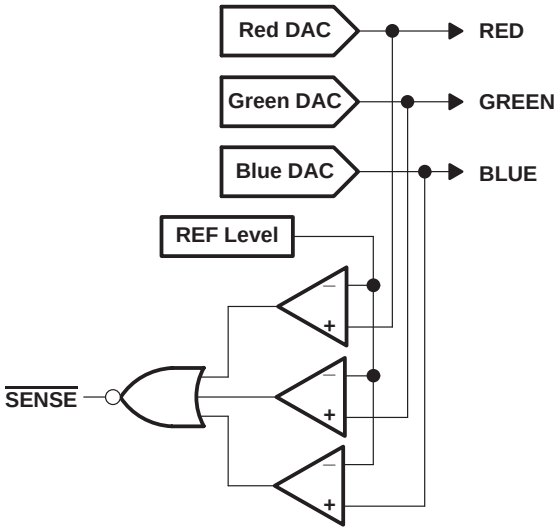


Figure 2–5. DAC Output Comparison Circuitry

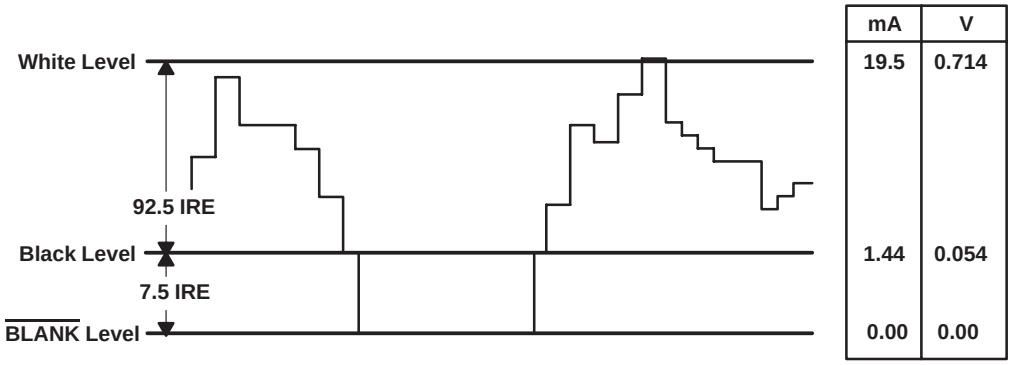


Figure 2–6. RS-343A Composite Video Output Waveforms

Table 2–22. RS-343A Video Output Truth Table (Blank Offset Current to Equal 7.5 IRE)

DAC INPUT DATA	$\overline{\text{BLANK}}$	OUTPUT LEVEL	I_O (mA)
0xFF	H	White	19.05
Data	H	Data	Data + 1.44
0x00	H	Black	1.44
0xXX	L	$\overline{\text{BLANK}}$	0

NOTE 5: This is a 75-Ω doubly terminated load, SETUP = 7.5 IRE, V_{ref} = internal, R_{SET} = 147 Ω.

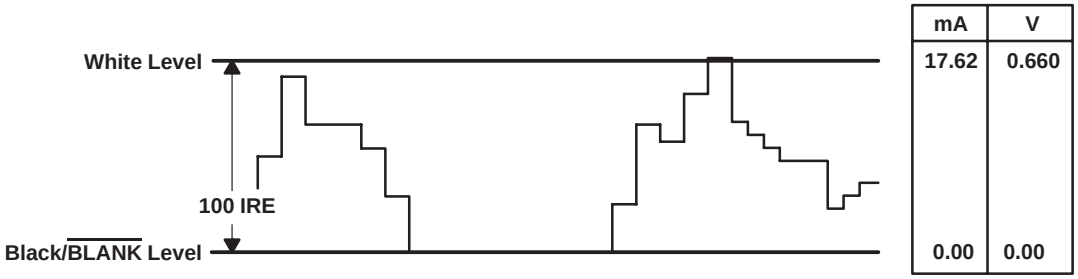


Figure 2–7. RS-343A Composite Video Output Waveforms (No Blank Pedestal)

Table 2–23. RS-343A Video Output Truth Table (No Blank Offset Current)

DAC INPUT DATA	$\overline{\text{BLANK}}$	OUTPUT LEVEL	I_O (mA)
0xFF	H	White	17.62
Data	H	Data	Data
0x00	H	Black	0
0xXX	L	$\overline{\text{BLANK}}$	0

NOTE 6: This is a 75-Ω doubly terminated load, SETUP = 0 IRE, V_{ref} = internal, R_{SET} = 147 Ω.

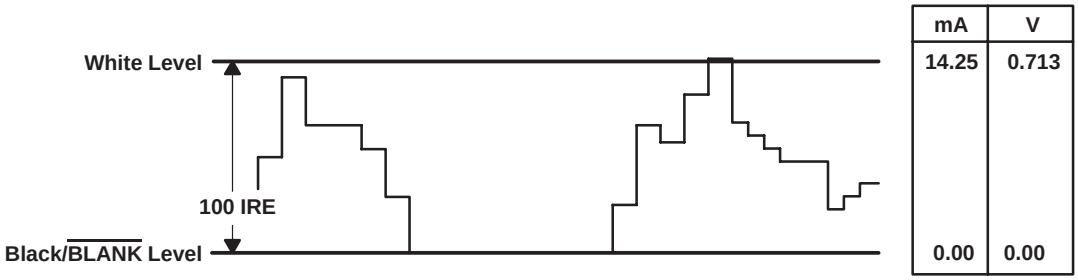


Figure 2–8. PS/2 Composite Video Output Waveforms

Table 2–24. PS/2 Video Output Truth Table (No Blank Offset Current)

DAC INPUT DATA	$\overline{\text{BLANK}}$	OUTPUT LEVEL	I_O (mA)
0xFF	H	White	14.25
Data	H	Data	Data
0x00	H	Black	0
0xXX	L	$\overline{\text{BLANK}}$	0

NOTE 7: This is a 75-Ω doubly terminated load, SETUP = 0 IRE, V_{ref} = internal, R_{SET} = 182 Ω.

3 Electrical Characteristics

3.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (unless otherwise noted)†

Supply voltage, V_{CC} (measured to GND) . . . . . 7 V
Input voltage range V_I (any digital terminal) . . . . . GND – 0.5 to V_{CC} + 0.5 V
Analog output short circuit duration to any power supply or common . . . . . unlimited
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature, T_{stg} . . . . . –65°C to 150°C
Junction temperature, T_J . . . . . 150°C
Case temperature for 10 seconds, T_C: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

3.2 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Power supply voltage, V_{CC}	4.75	5	5.25	V
Reference voltage, V_{ref}	1.15	1.235	1.26	V
High-level digital input voltage, including XIN and XOUT, V_{IH}	2		VCC+0.5	V
Low-level digital input voltage, including XIN and XOUT, V_{IL}	GND–0.5		0.8	V
Crystal input frequency, f_I (200 ppm)		14.318		MHz
Crystal loading	parallel	parallel	parallel	
Crystal series resistance		35		Ω
Output load resistance, R_L		37.5		Ω
White level adjust resistor, R_{SET}		147		Ω
Ambient operating temperature, T_A	0		70	°C

NOTE 1: Other crystal frequencies can be used.

3.3 Electrical Characteristics Over Recommended Full Voltage and Temperature Ranges

3.3.1 DC Characteristics, Total Device (see Note 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level digital output voltage, except OTCLKA and OTCLKB	I_{OH} = –4 mA	2.4			V
V_{OL}	Low-level digital output voltage, except OTCLKA and OTCLKB	I_{OL} = 4 mA			0.4	V
V_{OH}	High-level digital output voltage, OTCLKA and OTCLKB	I_{OH} = –12 mA	2.4			V
V_{OL}	Low-level digital output voltage, OTCLKA and OTCLKB	I_{OL} = 12 mA			0.4	V
I_{IH}	High-level digital input current	V_I = 2.4 V			1	µA
I_{IL}	Low-level digital input current	V_I = 0.4 V			–1	µA
I_{OZ}	Digital high-impedance-state output current				50	µA
C_i	Digital input capacitance	f = 1 MHz, V_I = 2.4 V		4		pF

NOTE 2: Test conditions generate RS-343A video signals unless otherwise specified. The recommended operation condition for generating test signals is R_{SET} = 147 Ω, V_{ref} = 1.235 V.

3.3.2 AC Characteristics, Supply Current, and Pipeline Delay (See Notes 3 and 4)

PARAMETER		TVP3409-170			TVP3409-135			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	V_{CC} supply current		265	285		231	250	mA
$I_{CC(sleep)}$	Sleep current (PCLK = 35 MHz)		55			55		mA

NOTES: 3. The recommended operation condition for generating test signals is R_{SET} = 147 Ω, V_{ref} = 1.235 V. TTL level input values are 0 V to 3 V, with input rise/fall times ≤ 3 ns, measured from 10% to 90% points. Timing reference points are 50% for both inputs and outputs. Analog output load ≤ 10 pF, $\overline{\text{SENSE}}$, D(7–0) output load ≤ 50 pF.

4. Pipeline delay is fixed for each mode (see Table 2–18 for pipeline delay for each mode).

3.4 Operating Characteristics Over Recommended Full Voltage and Temperature Ranges

3.4.1 DC Characteristics, Total Device (see Note 2)

PARAMETER		MIN	TYP	MAX	UNIT
	Resolution (each DAC)	8	8	8	bits
E_L	Integral linearity error (8-bit, each DAC)			±1	LSB
E_D	Differential linearity error (8-bit, each DAC)			±1	LSB
E_G	Gain error			±1%	
C_O	Digital output capacitance		7		pF
	Coding				binary
	Internal reference output voltage	1.15	1.235	1.26	V
	Sense voltage reference	270	340	410	mV
PSRR	Power supply rejection ratio			–6	dB

3.4.2 DC Characteristics, Analog Outputs (see Note 2)

PARAMETER			MIN	TYP	MAX	UNIT
	Output current	Gray scale			20	mA
		White level relative to black	17.69	19.05	20.4	mA
		Black level relative to $\overline{\text{BLANK}}$ (with pedestal)	0.95	1.44	1.9	mA
		Black level relative to $\overline{\text{BLANK}}$ (without pedestal)	0	5	50	µA
		$\overline{\text{BLANK}}$ level	0	5	50	µA
		One LSB		69.9		µA
	DAC-to-DAC matching			2%	5%	
	Output compliance		–0.5		1.2	V
Z_O	Output impedance			50		kΩ
C_O	Output capacitance	f = 1 MHz, I_O = 0 mA		13		pF

NOTE 2: Test conditions generate RS-343A video signals unless otherwise specified. The recommended operation condition for generating test signals is R_{SET} = 147 Ω, V_{ref} = 1.235 V.

3.4.3 AC Characteristics, DAC Performance (see Notes 3 and 5)

PARAMETER	TVP3409-170			TVP3409-135			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	
DAC-to-DAC crosstalk		–20			–20		dB
Clock and data feedthrough (see Note 5)		–20			–20		dB
Glitch impulse		50			50		pV-s

NOTES: 3. The recommended operation condition for generating test signals is R_{SET} = 147 Ω, V_{ref} = 1.235 V. TTL level input values are 0 V to 3 V, with input rise/fall times ≤ 3 ns, measured from 10% to 90% points. Timing reference points are 50% for both inputs and outputs. Analog output load ≤ 10 pF, SENSE, and D(7–0) output load ≤ 50 pF.

5. External voltage reference automatically disabled during power down. Test conditions are 25°C to 70°C, pixel and data ports at 0.4 V.

3.4.4 AC Characteristics, Clock Synthesizer (see Notes 6 and 7)

PARAMETER		TVP3409-170			TVP3409-135			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
t_1	Edge jitter, OTCLKA or OTCLKB (6 sigma)		300			300		ps

NOTES: 6. TTL level input values are 0 V to 3 V, with input rise/fall times ≤ 3 ns, measured from 10% to 90% points. Timing reference points are 50% for both inputs and outputs. Digital output load ≤ 15 pF. Crystal or reference frequency = 14.318 MHz, OTCLKA or OTCLKB loading ≤ 15 pF.

7. Output phase and duty cycle jitter excludes the reference clock or crystal oscillator jitter.

3.5 Timing Requirements

3.5.1 Total Device (see Note 3)

PARAMETER			TVP3409-170			TVP3409-135			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{max1}	Internal 2X clock frequency (for reference only)				170			135	MHz
f_{max2}	PCLK frequency	2X clock disabled			110			110	MHz
f_{max2x}	PCLK frequency	2X clock enabled	0		85	0		67.5	MHz
t_{cyc}	PCLK cycle time		9.09			9.09			ns
	PCLK duty cycle		30%	50%	70%	30%	50%	70%	

3.5.2 Pixel and Control Timing (see Note 3)

PARAMETER		TVP3409-170		TVP3409-135		UNIT
		MIN	MAX	MIN	MAX	
t_{su1}	Setup time, P(15–0), $\overline{\text{BLANK}}$	2		2		ns
t_{h1}	Hold time, P(15–0), $\overline{\text{BLANK}}$	2		2		ns

NOTE 3. The recommended operation condition for generating test signals is R_{SET} = 147 Ω, V_{ref} = 1.235 V. TTL level input values are 0 V to 3 V, with input rise/fall times ≤ 3 ns, measured from 10% to 90% points. Timing reference points are 50% for both inputs and outputs. Analog output load ≤ 10 pF, $\overline{\text{SENSE}}$, and D(7–0) output load ≤ 50 pF.

3.5.3 Microprocessor Port (see Note 8)

PARAMETER		TVP3409-170		TVP3409-135		UNIT
		MIN	MAX	MIN	MAX	
t_{su2}	Setup time, RS(1,0)	10		10		ns
t_{h2}	Hold time, RS(1,0)	10		10		ns
t_{su4}	Setup time, Write D(7–0)	10		10		ns
t_{h4}	Hold time, Write D(7–0)	10		10		ns
t_{w1}	Pulse duration, $\overline{\text{RD}}$, $\overline{\text{WR}}$ low	50		50		ns
t_{w2}	Pulse duration, $\overline{\text{RD}}$, $\overline{\text{WR}}$ high	3		3		PCLK periods

NOTE 8. TTL level input values are 0 V to 3 V, with input rise/fall times ≤ 3 ns, measured from 10% to 90% points. Timing reference points are 50% for both inputs and outputs.

3.5.4 Clock Synthesizer (see Notes 6)

PARAMETER		TVP3409-170		TVP3409-135		UNIT
		MIN	MAX	MIN	MAX	
f_{max3}	Maximum synthesizer frequency for OTCLKA or OTCLKB (external)		85		85	MHz
	Input duty cycle, Fref, XIN, and XOUT	45%	55%	45%	55%	
	Duty cycle, OTCLKA or OTCLKB	45%	55%	45%	55%	
t_{w3}	Pulse duration, high or low, $\overline{\text{STROBE}}$	20		20		ns
t_{su5}	Setup time, FS(1,0) to $\overline{\text{STROBE}}$	2		2		ns
t_{h5}	Hold time, FS(1,0) to $\overline{\text{STROBE}}$		4		4	ns

NOTE 6. TTL level input values are 0 V to 3 V, with input rise/fall times ≤ 3 ns, measured from 10% to 90% points. Timing reference points are 50% for both inputs and outputs. Digital output load ≤ 15 pF. Crystal or reference frequency = 14.318 MHz, OTCLKA or OTCLKB loading ≤ 15 pF.

3.6 Switching Characteristics

3.6.1 DAC Performance (see Note 3)

PARAMETER		TVP3409-170			TVP3409-135			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{d1}	Delay time, analog output (see Note 11)		9			9		ns
t_{r1}	Rise time, analog output (see Note 9)		3			3		ns
t_s	Settling time, analog output (see Note 10)		6			6		ns
	Delay SENSE output		1			1		µs
	Analog output skew			2			2	ns

NOTES: 3. The recommended operation condition for generating test signals is R_{SET} = 147 Ω, V_{ref} = 1.235 V. TTL level input values are 0 V to 3 V, with input rise/fall times ≤ 3 ns, measured from 10% to 90% points. Timing reference points are 50% for both inputs and outputs. Analog output load ≤ 10 pF, $\overline{\text{SENSE}}$, and D(7–0) output load ≤ 50 pF.

9. Measured between 10% to 90% of the full-scale transition.
10. Measured from the 50% point of the full-scale transition to the point at which the output has settled within ±1 LSB (settling time does not include clock and data feed through).
11. Measured from 90% point of PCLK rising edge to 50% point of full-scale transition.

3.6.2 Microprocessor Port (see Note 8)

PARAMETER		TVP3409-170		TVP3409-135		UNIT
		MIN	MAX	MIN	MAX	
t_{d2}	Delay time, $\overline{\text{RD}}$ asserted to D(7–0) driven	5		5		ns
t_{en}	Enable time, $\overline{\text{RD}}$ asserted to D(7–0) valid		40		40	ns
t_{dis}	Disable time, $\overline{\text{RD}}$ negated to D(7–0) 3-stated		20		20	ns
t_{v1}	Valid time, D(7–0) valid after $\overline{\text{RD}}$ high	5		5		ns

NOTE 8. TTL level input values are 0 V to 3 V, with input rise/fall times ≤ 3 ns, measured from 10% to 90% points. Timing reference points are 50% for both inputs and outputs.

3.6.3 Clock Synthesizer (see Note 6)

PARAMETER		TVP3409-170			TVP3409-135			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{d3}	Delay time, frequency select to OTCLKA or OTCLKB unstable (see Note 12)			0			0	ns
t_{d4}	Delay time, frequency select to OTCLKA or OTCLKB stable (see Note 12)		1	10		1	10	ms
	Delay time, power up to OTCLKA or OTCLKB stable			10			10	ms
t_{r2}, t_{f2}	Rise or fall time, OTCLKA or OTCLKB (see Note 13)			3			3	ns

NOTES: 6. TTL level input values are 0 V to 3 V, with input rise/fall times ≤ 3 ns, measured from 10% to 90% points. Timing reference points are 50% for both inputs and outputs. Digital output load ≤ 15 pF. Crystal or reference frequency = 14.318 MHz, OTCLKA or OTCLKB loading ≤ 15 pF.

12. Frequency select can refer to the FS(1,0) terminals or control register bits CC(5,4) or CC(1,0).
13. Rise and fall time measured from 10% to 90% points using 0 V and 3 V levels.

3.7 Timing Diagrams

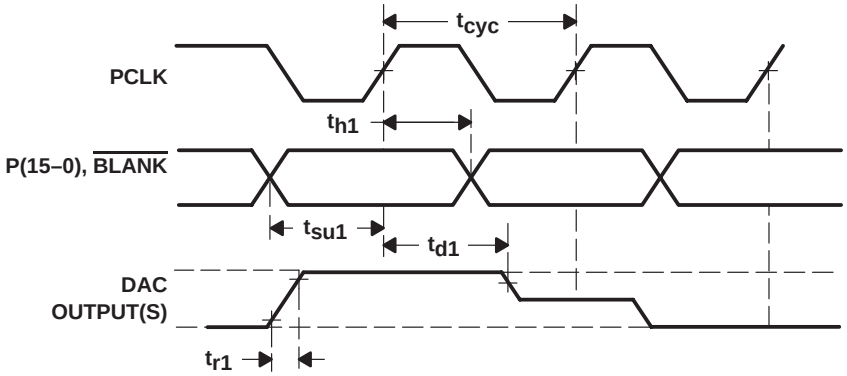


Figure 3–1. Pixel Input and Video Output Timing

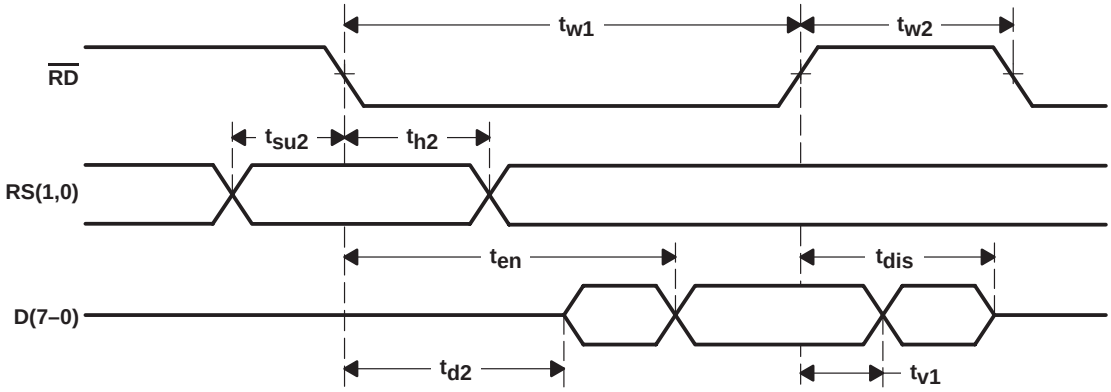


Figure 3–2. Basic Read-Cycle Timing

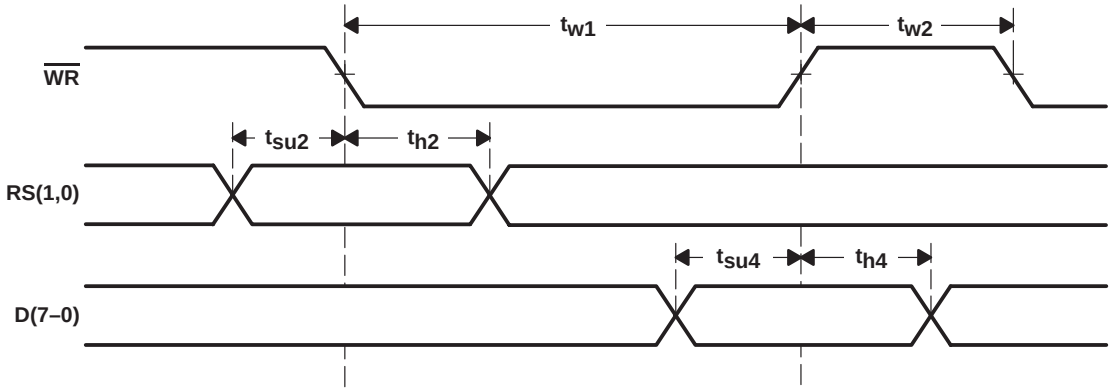


Figure 3–3. Basic Write-Cycle Timing

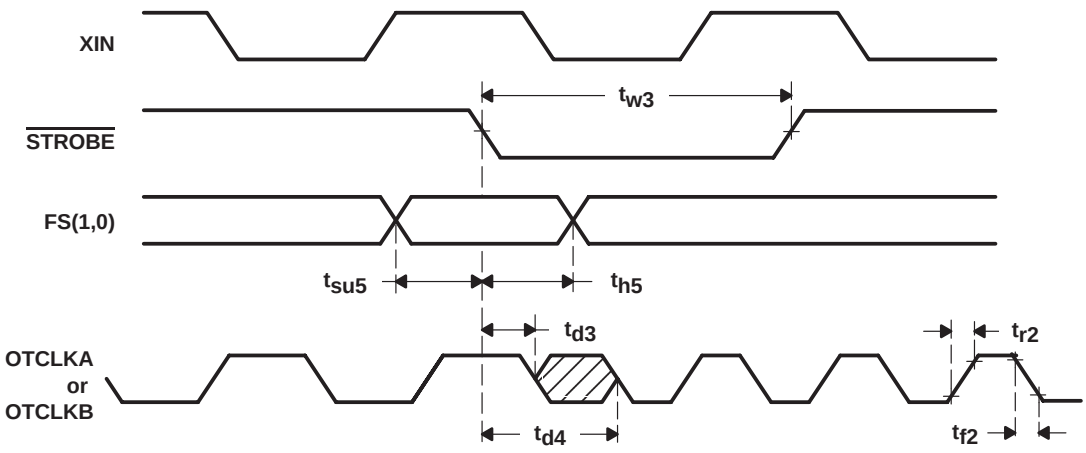


Figure 3–4. Clock Synthesizer (OTCLKA or OTCLKB) Timing

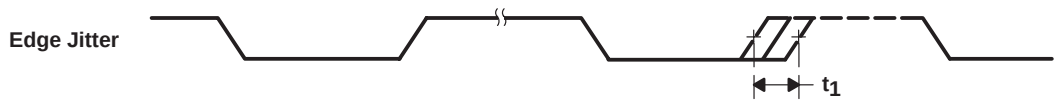


Figure 3–5. Clock Synthesizer Waveform Specifications (OTCLKA or OTCLKB)

Appendix A
Application Information

Board Layout

Careful configuration and placement of supply planes, components, and signal traces ensure a low-noise board. This helps ensure proper functionality and low signal emissions in restricted frequency bands as mandated by regulatory agencies.

A 4-layer PC board with separate power and ground planes should result in a board with quieter signals and supplies.

The TVP3409 should be placed close to the video output connector and between the video output connector and the edge card connector (see Figure A–1). This keeps the high-speed DAC output traces short and minimizes the amount of circuitry between the RAMDAC and the supply terminals on the edge card connector.

Power Distribution

Separate the power plane into digital and analog areas as illustrated in Figure A–1, A–4, A–5, and A–6. Place all digital components over the digital plane and all analog components over the analog plane. The analog components include the RAMDAC, reference circuitry, comparators, all mixed-signal devices, and any passive support components for analog circuits.

The analog and digital power planes should be connected with at least one ferrite bead across the separation as illustrated in Figures A-1. This bead provides resistance to high frequency currents. Select a ferrite bead with an impedance curve suitable for your design. The ferrite should have a resistance at a higher frequency than the maximum signal frequency on the PC board but lower than the second harmonic (2X) of that frequency. The following beads provide resistances of approximately 75 Ω at 100 MHz, Ferroxcube VK20019-4B, Fair-Rite 2743001111, or Philips 431202036690. The power and ground traces to the RAMDAC should be at least 50 mils wide. This is especially important on the TVP3409 because the device has only two V_{CC} terminals.

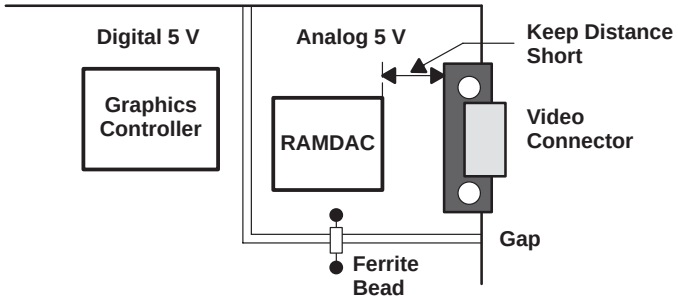


Figure A–1. Isolation of Digital V_{CC} Supply from Analog V_{CC} Supply

Decoupling Capacitors

All decoupling capacitors should be located within 0.25 inch of the device to be decoupled. Chip capacitors are recommended, but radial and axial leads can work. Keep lead lengths as short as possible to reduce inductance and electromagnetic interference (EMI). For leaded capacitors, use devices with a self-resonance above the pixel clock frequency.

For the TVP3409, decouple V_{CC} terminal to ground with a 0.1 F capacitor. For higher frequency pixel clocks (> 110 MHz) use a 0.01 μF capacitor in parallel with the 0.1 μF capacitor to shunt the higher frequency noise to ground. Power supply noise should be less than 200 mV for a good design. About 10% of any noise below 1 MHz is coupled onto the DAC outputs. As illustrated in Figure A–3, the COMP terminal should be decoupled with a 0.1 μF capacitor. For designs showing ghosting or smearing add a parallel COMP capacitance of 2.2 μF.

Digital Signals

The digital inputs should not travel over the analog power plane when possible. The RAMDAC should be located over the analog plane close to the digital-analog supply separation. The RAMDAC can also be placed over the supply separation so the digital pixel inputs are over the digital supply plane. The digital inputs, especially the P(15–0) high-speed inputs, should be isolated from the analog outputs. Placing the digital inputs over the digital supply reduces coupling into the analog supply plane. High-speed signals (both analog and digital) should not be routed under the RAMDAC.

Avoid high slew-rate edges as they can contribute to undershoot, overshoot, ringing, EMI, and noise feed through. Edges can be slowed down using series termination (33 to 150 Ω). Edge noise can result when a digital signal propagates from an impedance mismatch while the signal rises. The reflection noise is particularly troublesome in the TTL threshold region. For a 2-ns edge, the trace length must be less than 4 inches.

The clock signal trace should be as short as possible and should not run parallel to any high-speed signals. To ensure a quality clock signal without high frequency noise components, decouple the supply terminals on the clock driver. When necessary, transmission line techniques should be used on the clock by providing controlled impedance striplines and parallel termination. The 2x clock doubler in the TVP3409 helps to reduce signal quality problems and EMI radiations by reducing the frequency of the clock signal to the device.

Analog Signals

The load resistor should be as close as possible to the DAC outputs. The resistor should equal the destination termination which is usually a 75-Ω monitor. Unused analog outputs should be connected to ground. The DAC output traces should be as short as possible to minimize any impedance mismatch in the trace or video connector.

Match the impedance of the R, G, B traces with the termination (75 Ω). The width of the traces are determined by the distance from the ground plane and the dielectric constant of the PC board material. Keep the R, G, B traces at least 20 to 50 mils wide. Series ferrite beads can be added to the analog video signal to reduce high frequency signals coupled onto the DAC outputs or reflected from the monitor.

To reduce the interaction of the analog video return current with board components, a separate video ground return trace can be added to the ground plane or signal layer. This trace connects directly to the ground of the edge card connector (see Figure A–2). Using a separate video ground return path ensures that the RAMDAC ground is not corrupted with video return current.

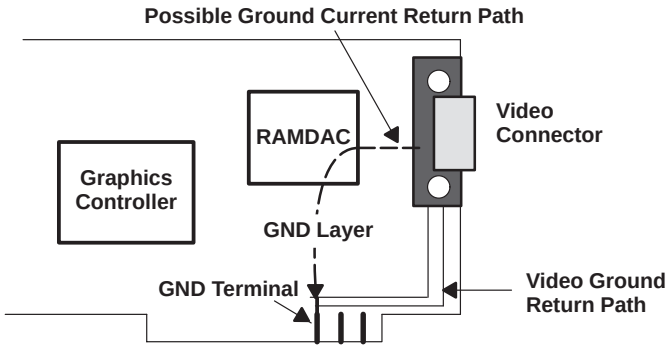


Figure A–2. Video Ground Return Current Path

Clock Synthesizer

The clock synthesizer should be connected to its own power and ground. The supply for the synthesizer must be quiet to reduce clock jitter. A 5.1 V zener diode can be used on the V_{CCS} input (terminal 50) to ensure a quiet voltage source. The analog PLL clock multiplier terminal (V_{CCM}) can also be connected to the same circuit (see Figure A–4).

DAC Outputs

The TVP3409 analog outputs should be protected against high-energy discharges, such as those from monitor arc-over or from hot-switching ac coupled monitors.

The diode protection circuit shown in Figure A–3 can prevent latch-up under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 are low-capacitance, fast-switching diodes.

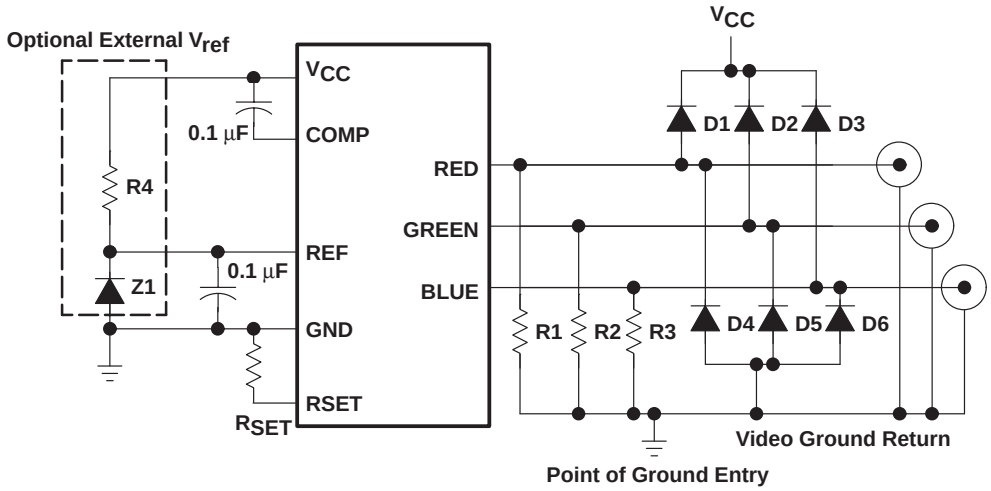


Figure A–3. Internal and External Voltage Reference Typical Connection Diagram

Power Circuits

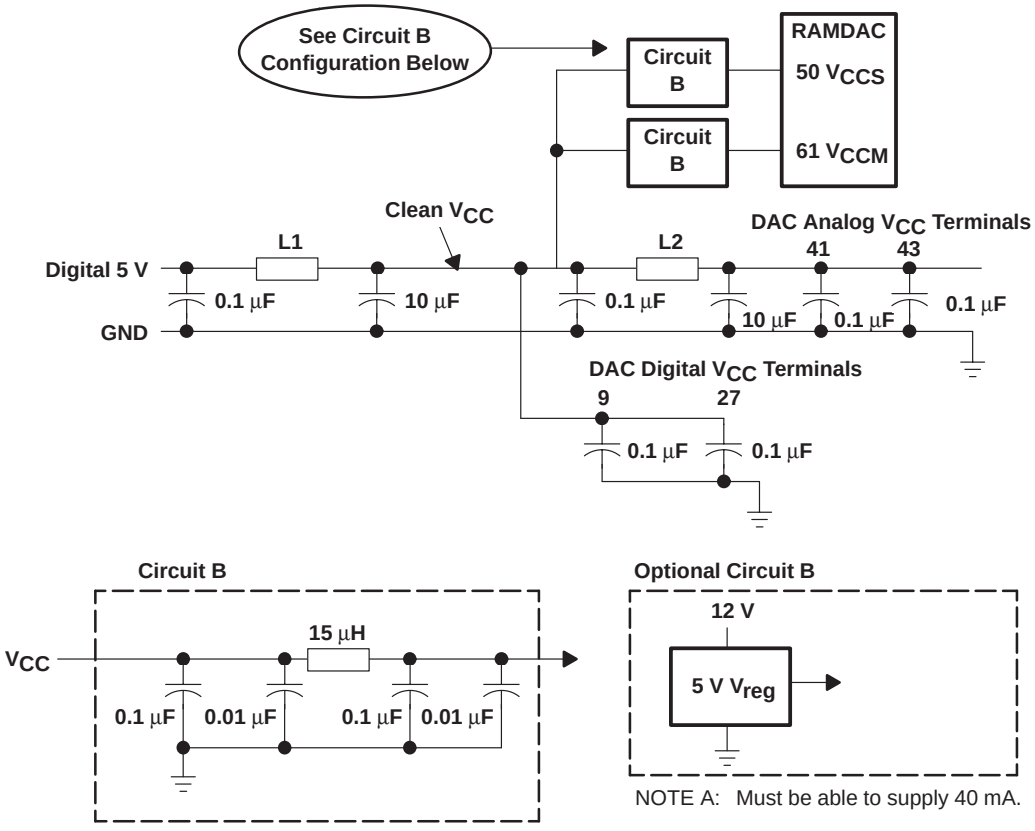


Figure A–4. Split Power Supply
(Connection Diagram for a Split Supply to the Device Showing the Clock Synthesizer and Multiplier Power Terminals, and DAC Digital and Analog Power Terminals)

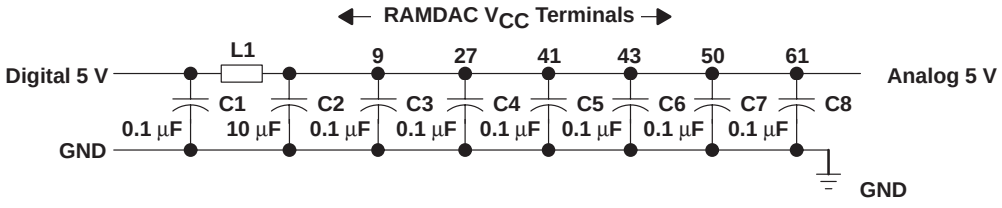


Figure A–5. Combined Power Supply
(Optional Power Filtering Circuit for Combined Power Supply)

Table A–1. Internal or External Voltage Reference Parts List

LOCATION	DESCRIPTION
L1, L2	Ferrite bead
R1–R3	75 Ω, 1% metal film resistor
R_{SET}	1% metal film resistor
D1–D6	Fast-switching diodes
Z1 (see Note 1)	1.2 V voltage reference 1 kΩ,
R4 (see Note 1)	5% resistor

NOTE 1: Optional for external V_{ref}.

Terminal Layout

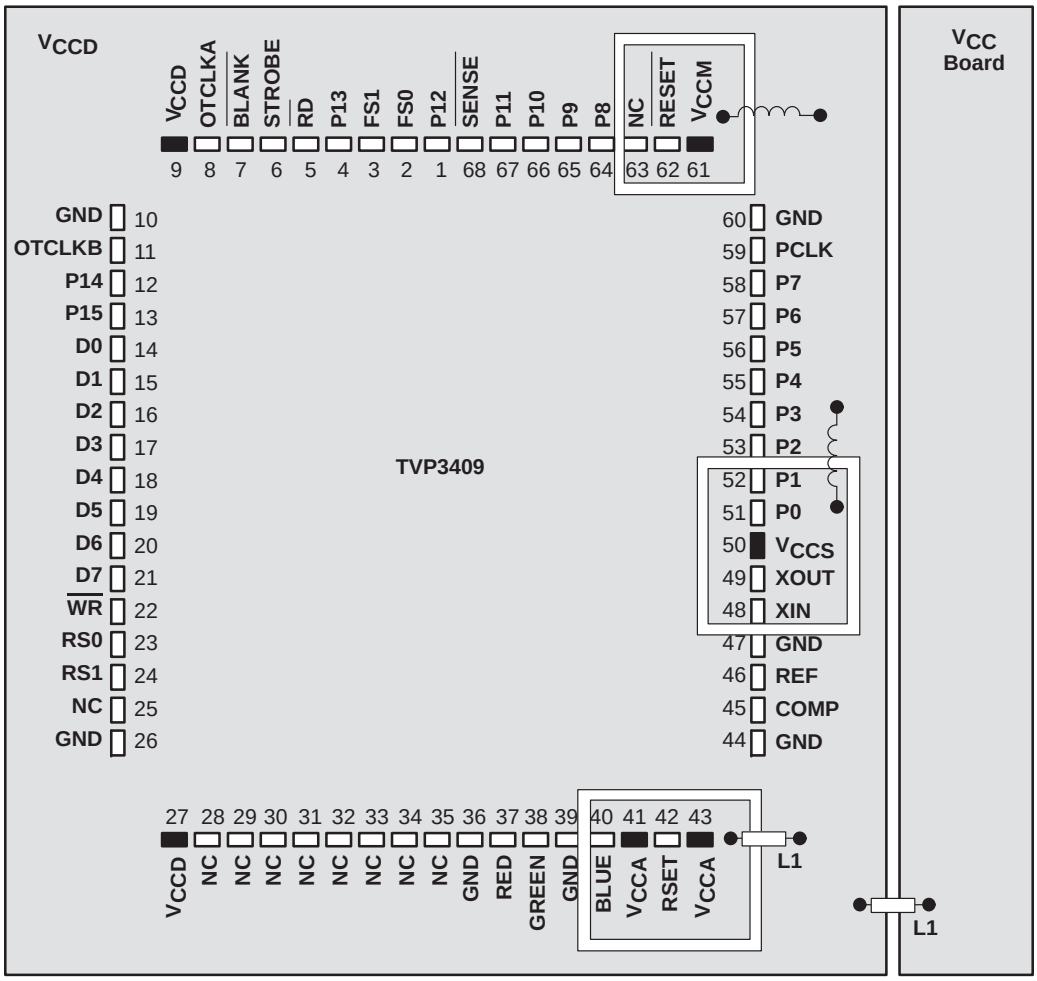


Figure A–6. Physical Layout for TVP3409 (Power Moats for V_{CCD}, V_{CCS}, V_{CCM}, and V_{CCA})

Appendix B
Register Summary

This section briefly shows the internal registers and the control they have on the RAMDAC functions.

Address Registers

WRITE-MODE ADDRESS (WMA) REGISTER							
7	6	5	4	3	2	1	0
Write Mode Address							

Address register 1 (write function)
Read/write, RS(1,0) = LL, Not reset
7–0 address to write RAMDAC color RAM

READ-MODE ADDRESS (RMA) REGISTER							
7	6	5	4	3	2	1	0
Read Mode Address							

Address register 1(read function)
Read/write, RS(1,0) = HH, Not reset
7–0 address to read RAMDAC color RAM

Control Registers

CONTROL REGISTER 0 (CR0)							
7	6	5	4	3	2	1	0
Color Mode				PD	Reserved	8/6	Ext Acc

Control register 0 (CR0)
Read/write, RS(1,0) = HL, Index (WMA) = 0x01
Reset = 0x00
7–4 color mode:
- 0000 8-bit pseudocolor
- 0001 15-bit
- 0010 2x 8-bit pseudocolor
- 0011 16-bit 5–6–5
- 0100 8-bit in two clocks
- 0101 24-bit true-color on 16 terminals, two clocks
- 0110 16-bit 5–6–5 on 8 terminals in two clocks
- 0111 24-bit true-color on 8 terminals in three clocks
- 1000 Reserved
- 1001 Reserved
- 1010 Reserved
- 1011 Reserved
- 1100 Reserved
- 1101 Reserved
- 1110 2x 24-bit true-color packed on 16 terminals in three clocks
- 1111 Reserved

3 Power down (1)
2 Reserved
1 Bit select
- 0 6-bit
- 1 8-bit

0 Extended register access (1)

CONTROL REGISTER 1 (CR1)							
7	6	5	4	3	2	1	0
Reserved	Reserved		Blank En	ClkA PD	ClkB PD	Sense Dis	Reserved

Control register 1 (CR1)
Read/write, RS(1,0) = HL, Index (WMA) = 0x05
Reset = 0x00
7 Reserved
6,5 Reserved
4 Blank pedestal enable (1)
3 OTCLKA power down (1)
2 OTCLKB power down (1)
1 SENSE disable (1)
0 Reserved

CLOCK SYNTHESIZER CONTROL (CC) REGISTER							
7	6	5	4	3	2	1	0
ClkA Contr	Reserved	Clock A Freq Select		ClkB Contr	Reserved	Clock B Freq Select	

Clock control register 0 (CC0)
Read/write, RS(1,0) = HL, Index (WMA) = 0x06,
Reset = 0x00
7 Clock A control
0 Input terminals FS(1,0)
1 Bits CC(5,4)
6 Reserved
5,4 Clock A frequency select
00 25.057
01 28.189
10 Register set C, (after reset = 50.114 MHz)
11 Register set D, (after reset = 75.170 MHz)
3 Clock B control
0 Input terminals FS(1,0)
1 Bits CC(1,0)
2 Reserved
1,0 Clock B frequency select
00 29.979 MHz
01 40.091 MHZ
10 50.114 MHz
11 Register set D, (after reset = 59.957 MHz)

RMR, ID, and TEST Registers

PIXEL READ MASK REGISTER (RMR)							
7	6	5	4	3	2	1	0
8-Bit Read Mask Value							

Read mask register (RMR)
Read/write, RS(1,0) = HL, Index (WMA) = 0x00 or CR0(0) = 0, or use state machine
Not Reset = 0x00
7–0 8-bit read mask value

MANUFACTURER IDENTIFICATION REGISTER (MIR)							
7	6	5	4	3	2	1	0
1	0	0	1	0	1	1	1

Manufacturer identification register (MIR)
Read only, RS(1,0) = HL, Index (WMA) = 0x02
7–0 Value = 0x97

DEVICE IDENTIFICATION REGISTER (DIR)							
7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	1

Device identification register (DIR)
Read only, RS(1,0) = HL, Index (WMA) = 0x03
7–0 Value = 0x09

TEST REGISTERS (TST)							
7	6	5	4	3	2	1	0
Reserved							

Test registers (TST)
Read only, RS(1,0) = HL, Index (WMA) = 0x04
Not reset
7–0 Data returned is indeterminate.
Registers are included only for compatibility with ATT20C409

Color RAMS

LOOK-UP TABLE (LUT) DATA REGISTER							
7	6	5	4	3	2	1	0
Red, Green, Blue Sequential 8-Bit Values							

Look-up table (LUT) data register
Read/write, RS(1,0) = LH, modulo three
Direct read/write, auto–incrementing, Not reset
7–0 Red (7–0), Green (7–0), Blue (7–0) pixel color

Synthesizer Registers

FEEDBACK DIVIDER (M)							
7	6	5	4	3	2	1	0
8-Bit M Value							

Feedback divider term
Read/write, RS(1,0) = LH, Index (WMA) =0x48, 0x4C, 0x6C
Reset to produce the reset frequencies in Table 2–19
7–0 8-bit divider term for the feedback circuit

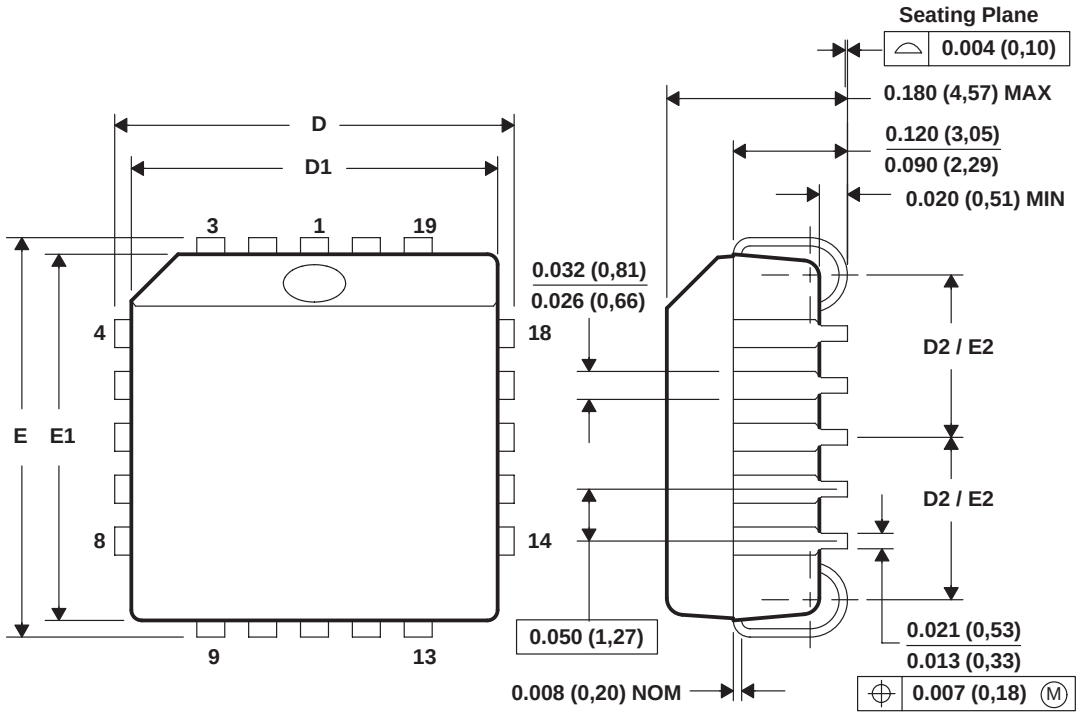
POSTSCALER AND REFERENCE DIVIDERS (P,N)							
7	6	5	4	3	2	1	0
2-Bit P Value		6-Bit N Value					

Postscalar and reference divider terms
Multiple registers some read/write and some read only,
Reset to produce the reset frequencies in Table 2–19, RS(1,0) = HL
Index (WMA) = 0x49, 0x4D, 0x6D,
7,6 2-bit postscaler divider
5–0 6-bit input reference divider

Appendix C
Mechanical Data

FN (S-PQCC-J)** **PLASTIC J-LEADED CHIP CARRIER**

20 PIN SHOWN



NO. OF PINS **	D / E		D1 / E1		D2 / E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

4040005/B 10/94

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

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