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AK4542

AC'97™ Multimedia Audio CODEC

Features:

- **AC'97 Rev. 2.0 Compliant**
- **Exceeds PC98 Performance Requirements:**
  - **A/D..... 90dBA**
  - **D/A..... 90dBA**
  - **A-A..... 95dBA**
- **Analog Inputs:**
  - **4 Stereo Inputs: LINE, CD, VIDEO, AUX**
  - **Speakerphone and PC BEEP Inputs**
  - **2 Independent MIC Inputs**
- **Analog Output:**
  - **Stereo LINE Output with volume control**
  - **True Line Level with volume control**
  - **Mono Output with volume control**
- **3D Stereo Enhancement**
- **Low Power Consumption 240 mW**
- **Power Supplies: Analog 5.0V, Digital 3.3V or 5.0V**
- **48 Pin QFP Package**

General Description

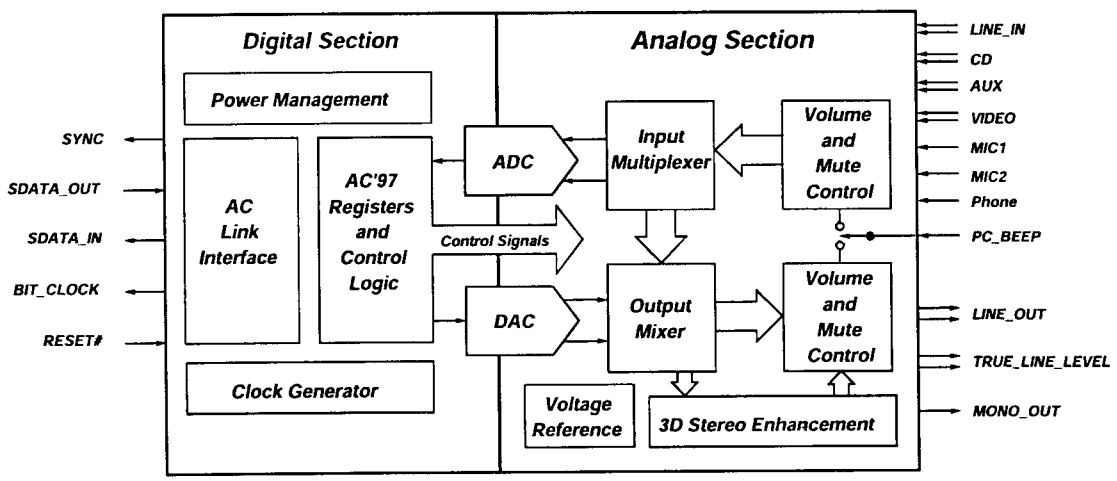
The AK4542 is a high performance codec compliant with Audio Codec'97 Rev2.0 requirements. The simple fivdine AC Link serial interface allows the AK4542 to be used with DC97 digital controllers as well as custom logic accelerators to meet full PC98 requirements for a PCI audio solution.

The AK4542 provides two pairs of stereo outputs with independent volume controls, a mono output, and multiple stereo and mono inputs, along with flexible mixing, gain and mute functions to provide a complete integrated audio solution for PCs.

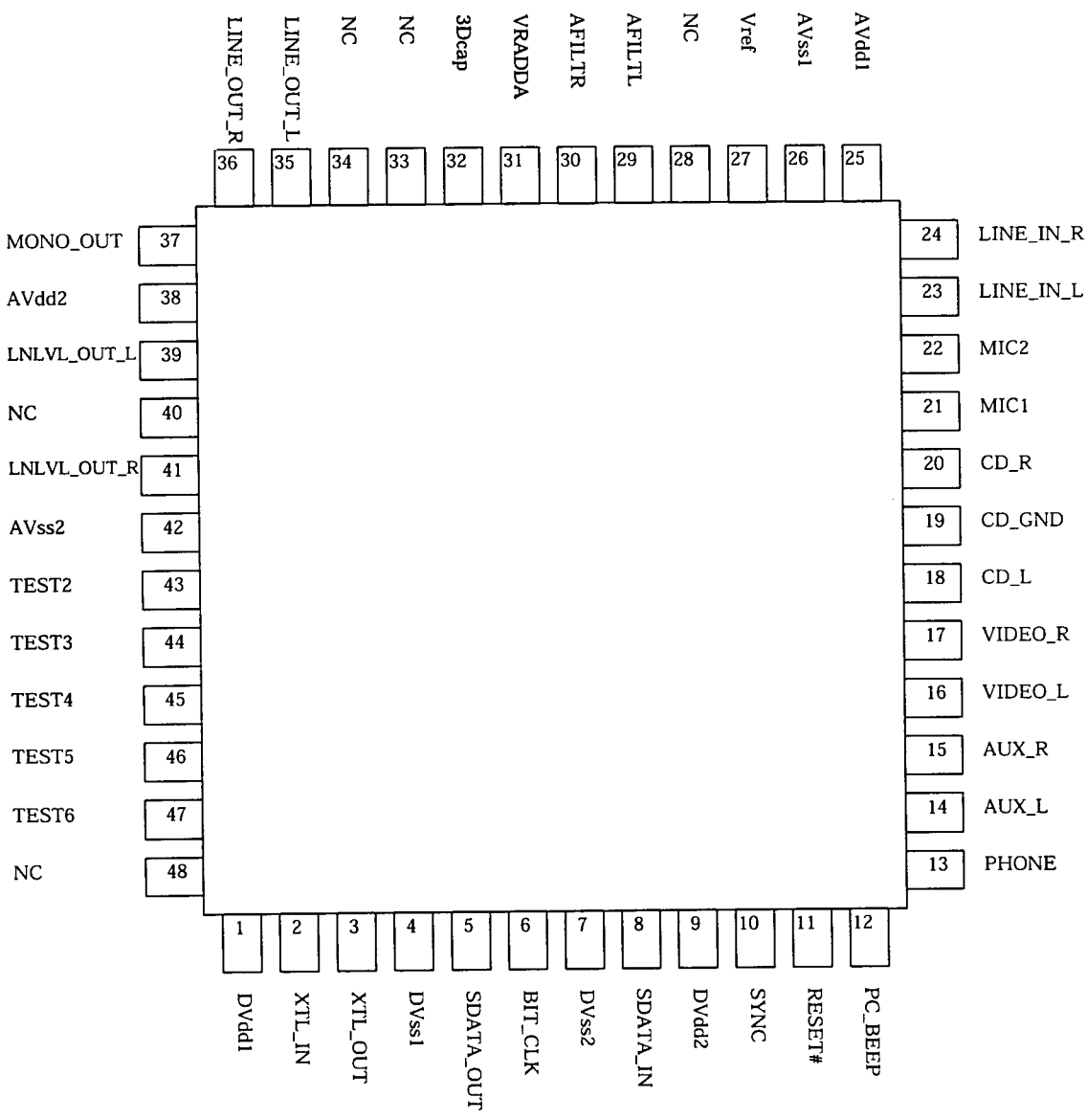
Sampling at 48kHz, the AK4542 provides excellent audio performance, meeting or exceeding all standard requirements. It has low power consumption and flexible power-down modes for use in laptops as well as desktop PCs and add-in boards.

Like the earlier pin-compatible AK4540, the AK4542 is available in a compact 48-lead QFP package.

■Block Diagram



* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.


LINE_OUT_R 36
LINE_OUT_L 35
NC 34
NC 33
3Dcap 32
VRADDA 31
AFILTR 30
AFILTL 29
NC 28
Vref 27
AVss1 26
AVdd1 25
MONO_OUT 37
AVdd2 38
LNLVL_OUT_L 39
NC 40
LNLVL_OUT_R 41
AVss2 42
TEST2 43
TEST3 44
TEST4 45
TEST5 46
TEST6 47
NC 48
24 LINE_IN_R
23 LINE_IN_L
22 MIC2
21 MIC1
20 CD_R
19 CD_GND
18 CD_L
17 VIDEO_R
16 VIDEO_L
15 AUX_R
14 AUX_L
13 PHONE
1 DVdd1
2 XTL_IN
3 XTL_OUT
4 DVss1
5 SDATA_OUT
6 BIT_CLK
7 DVss2
8 SDATA_IN
9 DVdd2
10 SYNC
11 RESET#
12 PC_BEEP

Pin/Function

No.	Signal Name	I/O	Description
1	DVdd1	-	Digital power supply; 3.3V or 5.0V.
2	XTL_IN (MCLKI)	I	24.576MHz(512fs) Crystal is normally connected. If crystal is not connected, external clock can be used.
3	XTL_OUT (open)	O	24.576MHz(512fs) Crystal If external clock is used, this pin should be open.
4	DVss1	-	Digital Ground; 0V
5	SDATA_OUT	I	Serial 256-bit AC'97 data stream from digital controller
6	BIT_CLK	O	12.288MHz(256fs) serial data clock
7	DVss2	-	Digital Ground; 0V
8	SDATA_IN	O	Serial 256-bit AC'97 data stream to digital controller
9	DVdd2	-	Digital power supply; 5.0V or 3.3V.
10	SYNC	I	AC'97 Sync Clock, 48kHz(1fs) fixed rate sampling rate
11	RESET#	I	AC'97 Master Hardware Reset
12	PC_BEEP	I	PC Speaker beep pass through
13	PHONE	I	From telephony subsystem speakerphone
14	AUX_L	I	Aux Left Channel
15	AUX_R	I	Aux Right Channel
16	VIDEO_L	I	Video Audio Left Channel
17	VIDEO_R	I	Video Audio Right Channel
18	CD_L	I	CD Audio Left Channel
19	CD_GND	I	CD Audio analog ground; 0V CD_GND or analog ground should be connected.
20	CD_R	I	CD Audio Right Channel
21	MIC1	I	Desktop Microphone Input
22	MIC2	I	Second Microphone Input
23	LINE_IN_L	I	Line In Left Channel
24	LINE_IN_R	I	Line In Right Channel
25	AVdd1	-	Power supply; 5.0V
26	AVss1	-	Analog Ground; 0V
27	Vref	O	Reference Voltage Output; 0.1μF +4.7μF capacitors should be connected to analog ground.
28	NC	-	No Connection
29	AFILTL	O	Anti-Aliasing Filter Cap Connected to analog ground with 1nF capacitor.
30	AFILTR	O	Anti-Aliasing Filter Cap Connected to analog ground with 1nF capacitor.
31	VRADDA	O	Vref for ADC and DAC; 0.1μF +4.7μF capacitors should be connected to analog ground.
32	3Dcap	O	3D Stereo Enhancement Cap; 27nF capacitor should be connected to analog ground.
33	NC	-	No Connection
34	NC	-	No Connection
35	LINE_OUT_L	O	Line Out Left Channel
36	LINE_OUT_R	O	Line Out Right Channel
37	MONO_OUT	O	To telephony subsystem speakerphone
38	AVdd2	I	Power supply; 5.0V This pin should be directly connected to AVdd1 on board.
39	LNLVL_OUT_L	O	True Line Level Out Left Channel
40	NC	-	No Connection
41	LNLVL_OUT_R	O	True Line Level Out Right Channel
42	AVss2	-	Analog Ground
43	TEST2	I	Test pin (This pin should be open for normal operation)
44	TEST3	I	Test pin (This pin should be open for normal operation)
45	TEST4	I	Test pin (This pin should be open for normal operation)
46	TEST5	I	Test pin (This pin should be open for normal operation)
47	TEST6	I	Test pin (This pin should be open for normal operation)
48	NC	-	No Connection

Absolute Maximum Rating

AGND, DGND=0V (Note 1)

Parameter		Symbol	min	max	Units
Power Supplies					
Analog(AVDD1 & AVDD2)	(Note 2)	VA	-0.3	6.0	V
Digital(DVDD1 & DVDD2)	(Note 3)	VD	-0.3	6.0	V
Input Current (any pins except for supplies)		IIN	-	±10	mA
Analog Input Voltage	(Note 4)	VINA	-0.3	6.0 or (VA+0.3)	V
Digital Input Voltage	(Note 4)	VIND	-0.3	6.0 or (VA+0.3)	V
Ambient Temperature		Ta	-10	70	°C
Stroge Temperature		Ta	-65	150	°C

Note 1. All voltages with respect to ground
2. AVdd1 and AVdd2 should be connected internally and derived from AVdd through the substrate.
3. Digital supplies means DVDD1 and DVDD2, and they are not connected internally.
4. Max value is higher voltage of 6.0V or VA+0.3V

Warning: Operation at or beyond these limits may results in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

Recommended Operating Condition

AGND, DGND=0V (Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies	AK4542					
Analog		VA	4.75	5.0	5.25	V
Digital		VD	3.0	-	5.25	V

Note 1 : All voltages with respect to ground.

AK4542 Analog Characteristics

Ta=25°C,AVdd=DVdd=5.0V±5%, fs=48KHz, Signal Frequency =1kHz
All volume setting for ADC/DAC performance measurement is 0dB.

Parameter	min	typ	max	Units
Audio-ADC				
Resolution			16	Bits
S/N (A weight)	85	90		dB
S/(N+D) (-1dB analog input)	70	80		dBFS
Inter Channel Isolation	70	83		dB
Inter Channel Gain Mismatch			0.5	dB
Full Scale Input Voltage	0.88	1.0	1.12	Vrms
Power Supply Rejection		50		dB
Audio DAC: measured at AOUTL/AOUTR via MIXER path				
Resolution			16	Bits
S/N (A weighted) : mixer+DAC measured at AOUT	85	90		dB
S/(N+D) (-1dB digital input)	75	85		dBFS
Inter Channel Isolation	75	95		dB
Inter Channel Gain Mismatch			1.0	dB
Full Scale Output Voltage	0.88	1.0	1.12	Vrms
Total Out-of-Band Noise (28.8kHz - 100kHz)		-65		dB
Power Supply Rejection		50		dB
MIC Amplifier / MUX				
Gain : 20dB is selected	18	20	22	dB
Master volume (Mono, Stereo, True Line Level Out) : 1.5dB x 32 step				
Step Size		-1.5		dB
Attenuation Control Range	-46.5		0	dB
Load Resistance	10			kΩ
PC Beep : 3dB x 16 step				
Step Size		-3.0		dB
Attenuation Control Range	-45		0	dB
Analog Mixer : 1.5dB x 32 step				
Step Size		-1.5		dB
Gain Control Range	-34.5		+12	dB
Record Gain : 1.5dB x 16 step				
Step Size		+1.5		dB
Gain Control Range	0		+22.5	dB
Mixer				
Input Voltage (except for MIC)		1.0		Vrms
Input Voltage MIC : Gain = 0dB MIC : Gain = 20dB		1 0.1		Vrms Vrms
S/N(A weighed) : 0dB setting, 1 path is selected at Mixer CD to AOUT: Other analog input to AOUT	88	95 95		dB dB
Input Impedance (Input gain=0dB,Rec_MUTE=off) PC_BEEP only Others(PHONE, LINE, CD, AUX, VIDEO) Input Impedance (MIC1 and MIC2)	(10) (10) (10)	÷ 100 50 30		kΩ kΩ kΩ
Power Supplies				
Power Supply Current(Total) All ON mode(all PR_bit are 0) Cold Reset Status (RESET#=L,Vref is ON.) All OFF mode(all PR_bits are 1.)		48 4 0	70 7 0.2	mA mA mA

Filter Characteristics

Ta=25°C,AVdd,DVdd=5.0V±5%, fs=48KHz(fixed)

Parameter	min	typ	Max	Units
ADC Digital Filter (Decimation LPF)				
Passband (±0.2dB) Note)	0		19.2	kHz
Stopband	28.8			kHz
Stopband Attenuation	70			dB
Group Delay			0.5	ms
ADC Digital Filter (HPF)				
Frequency Response; -3dB -0.5dB -0.1dB		7.5 21 49		Hz
DAC Digital Filter				
Passband (±0.2dB)	0		19.2	kHz
Stopband	28.8			kHz
Group Delay			0.5	ms
Stopband Rejection	70			dB
DAC Post filter				
Passband Frequency Response (0 - 19.2kHz)		±0.1		dB

Note) This frequency scales with the sampling frequency (fs).

AK4542 DC Characteristics

Ta=10~70°C, Avdd1= Avdd2=5.0V±5%, 50pF external load

Parameter	Symbol	min	typ	Max	Units
"H" level input voltage XTAL_IN All pins except for XTAL_IN and TEST pins	VIH	 0.7xVA 2.2	-	-	V
"L" level input voltage XTAL_IN All pins except for XTAL_IN and TEST pins	VIL	-	-	 0.3xVA 0.8	V
"H" level output voltage Iout= -1mA	VOH	2.6	-	-	V
"L" level output voltage Iout= 1mA	VOL	-	-	0.55	V
Input leakage current(AC-link inputs)	Iin	-	-	±10	µA

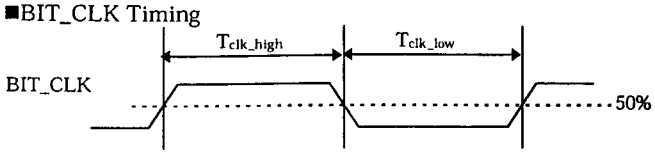
Switching Characteristics

Ta=25°C,Avdd1=Avdd2=5.0V, 50pF external load

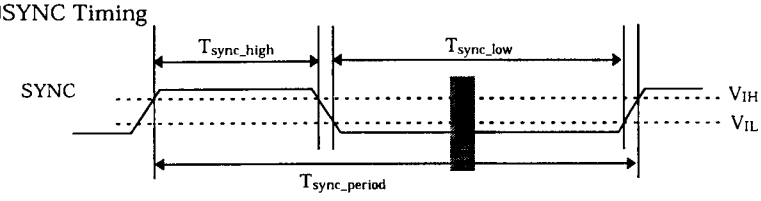
Parameter	Symbol	min	Typ	max	Units
Master Clock Frequency Note)	Fmclk	-	24.576	-	MHz
If Crystal is not used.		45	50	55	%
AC link Interface Timing					
BIT_CLK frequency	Fbclk		12.288		MHz
BIT_CLK clock Period(Tbclk=1/Fbclk)	Tbclk	-	81.38		ns
BIT_BLK low pulse width	Tclk_low	32.56	40.7	48.84	ns
BIT_BLK low pulse width	Tclk_high	32.56	40.7	48.84	ns
BIT_CLK rise time	Trise_clk	-	-	6	ns
BIT_CLK fall time	Tfall_clk	-	-	6	ns
SYNC frequency		-	48	-	kHz
SYNC low pulse width	Tsync_low	-	19.5 (240 cycle)	-	µs (Tbclk)
SYNC high pulse width	Tsync_high	-	1.3 (16 cycle)	-	µs (Tbclk)
SYNC rise time	Trise_sync	-	-	6	ns
SYNC fall time	Tfall_sync	-	-	6	ns
Setup time(SDATA_IN,SDATA_OUT)	Tsetup	15.0	-	-	ns
Hold time(SDATA_IN,SDATA_OUT)	Thold	25.0	-	-	ns
SDATA_IN rise time	Trise_din	-	-	6	ns
SDATA_IN fall time	Tfall_din	-	-	6	ns
SDATA_OUT rise time	Trise_dout	-	-	6	ns
SDATA_OUT fall time	Tfall_dout	-	-	6	ns
Cold Rest (SDATA_OUT=L, SYNC=L)					
RESET# active low pulse width	Trst_low	1.0	-	-	µs
RESET# inactive to BIT_CLK delay	Trst2clk	162.8 (2 cycle)			ns (Tbclk)
Warm Rest Timing					
SYNC active low pulse width	Tsync_high	1.0	1.3 (16 cycle)	-	µs (Tbclk)
SYNC inactive to BIT_CLK delay	Tsync2clk	162.8 (2 cycle)			ns (Tbclk)
AC-link Low Power Mode Timing					
End of Slot 2 to BIT_CLK, SDATA_IN Low	Ts2_pdwn	-	-	1.0	µs
Activate Test Mode Timing					
Setup to trailing edge of RESET#	Tsetup2rst	15.0	-	-	ns
Hold from RESET# rising edge	Thold2rst	100	-	-	ns
Rising edge of RESET# to Hi-Z	Toff	-	-	50	ns
Falling edge of RESET# to"L"	Tlow	-	-	50	ns

Note) The use of crystal is recommended. Master Clock should be continued supply or fixed to "H" state or "L" state during power down state. If Master Clock is supplied from controller (or if a external oscillatoris used), Master Clock should be input to XTAL_IN, meanwhile XTAL_OUT should be open.

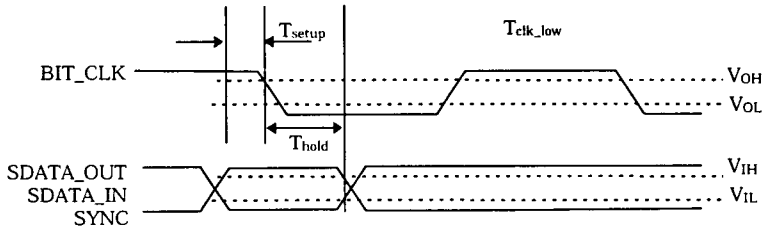
■BIT_CLK Timing



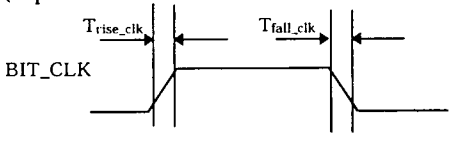
■SYNC Timing

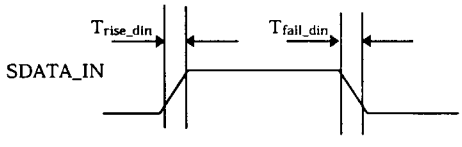


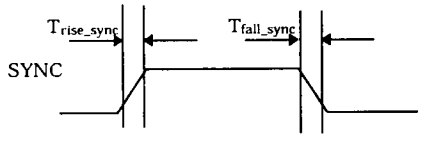
■Setup and Hold Timing

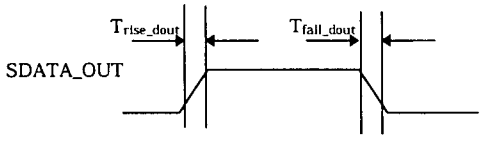


■Signal Rise and Fall Times
(50pF external load : from 10% 90% of DVdd)

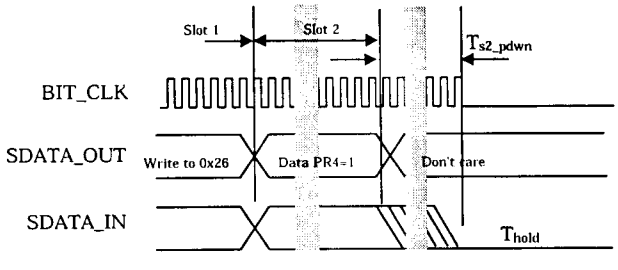




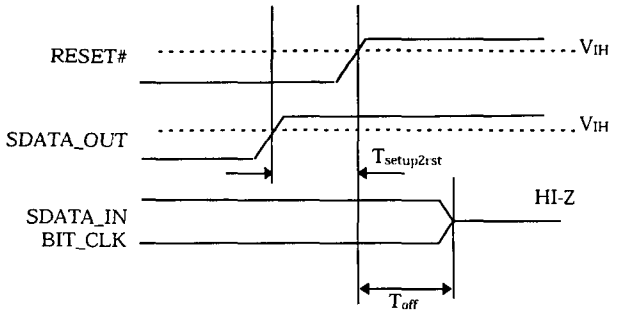




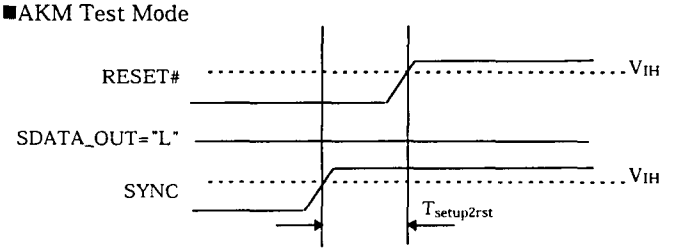
■AC-link Low Power Mode Timing



■Activate Test Mode



■AKM Test Mode



Notes:[1]

1. All AC-link signals are normally low through the trailing edge of RESET#. Bringing SDATA_OUT high for the rising edge of RESET# causes the AK4542 AC-link outputs to go high impedance which is suitable for ATE in circuit testing. Note that the AK4542 enters in the ATE test mode regardless SYNC is high or low.

2. Bringing both SYNC high and SDATA_OUT low for the rising edge of RESET# causes AKM test mode.

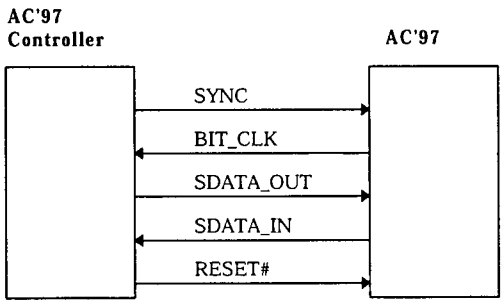
3. Once test modes have been entered, the only way to return to the normal operating state is to issue "cold reset" which issues RESET# with both SYNC and SDATA_OUT low.

[1] All the following sentences written with small italic font in this document quote the AC97 component specification.

General Description

■AC '97 Connection to the Digital AC '97 controller

[2]AC '97 communicates with its companion AC '97 controller via a digital serial link, AC-link". All digital audio streams, and command/status information are communicated over this point to point serial interconnect. A breakout of the signals connecting the two is shown in the following figure.



■Digital Interface

The AK4542 incorporates a 5 pin digital serial interface that links it to the AC '97 controller. AC-link is a bi-directional, fixed rate(48kHz), serial PCM digital stream. It handles multiple input, and output audio streams, as well as control register accesses employing a time division multiplexed (TDM) scheme. The AC-link architecture divides each audio frame into 12 outgoing and 12 incoming data streams, each with 20-bit sample resolution. DAC and ADC resolution of the AK4542 is 16 bit resolution. The data streams currently defined by the AC '97 specification include:

- ***PCM Playback*** ***2 output slots***

2 channel composite PCM output stream

- ***PCM Record data*** ***2 input slots***

2 channel composite PCM input stream

- ***Control*** ***2 output slot***

Control register write port

- ***Status*** ***2 input slots***

Control register read port

SYNC, fixed at 48 KHz, is derived by dividing down the serial bit clock (BIT_CLK). BIT_CLK, fixed at 12.288 MHz, provides the necessary clocking granularity to support 12, 20-bit outgoing and incoming time slots. AC-link serial data is transitioned on each rising edge of BIT_CLK. The receiver of AC-link data, the AK4542 for outgoing data and AC '97 controller for incoming data, samples each serial bit on the falling edges of BIT_CLK.

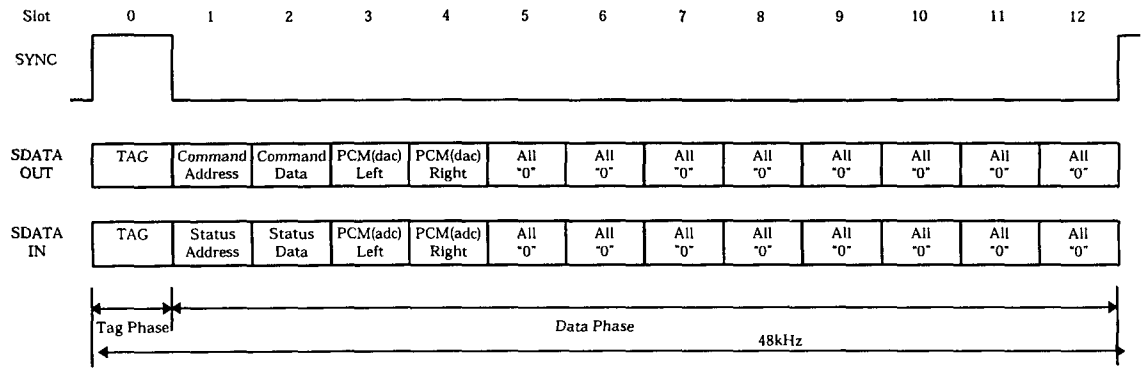
The AC-link protocol provides for a special 16-bit slot (Slot 0) wherein each bit conveys a valid tag for its corresponding time slot within the current audio frame. A "1" in a given bit position of slot 0 indicates that the corresponding time slot within the current audio frame has been assigned to a data stream, and contains valid data. If a slot is "Tagged" invalid, it is the responsibility of the source of the data, (The AK4542 for the input stream, AC '97 controller for the output stream), to stuff all bit positions with 0's during that slot's active time.

SYNC remains high for a total duration of 16 BIT_CLKs at the beginning of each audio frame. The portion of the audio frame where SYNC is high is defined as the "Tag Phase". The remainder of the audio frame where SYNC is low is defined as the "Data Phase".

Note that SDATA_OUT and SDATA_IN data is delayed one BIT_CLK because AC'97 controller causes SYNC signal high at a rising edge of BIT_CLK which initiates a frame.

"Output" stream means the direction from AC97 controller to the AK4542 and "Input" stream means the direction from the AK4542 to AC97 controller

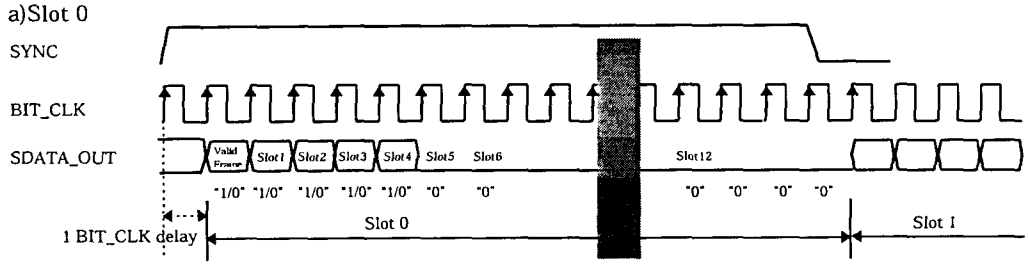
[2]All the following sentences written with small italic font in this document quote the AC97 component specification.



There are 13 slots in one frame. The frequency of the frame (sync) is fixed to 48kHz. Only Slot 0, which is Tag phase, is 16bits, and other slots are 20bits.

AC-link Audio Output Frame (SDATA_OUT)

a)Slot 0



First the AK4542 checks the Valid Frame bit first. Note that when valid frame bit is "1", at least one of slot 1,slot 2,slot3,and slot 4 are valid, other slots (5- 12 slots) are ignored.
If the bit is "0", the AK4542 ignores the following all other TAG bits and each slots.
Next, the AK4542 checks the validity of each slot in the TAG phase (slot 0).
If each bit regarding to slots is "0", then the AK4542ignores the slot regarding to the bit.
If "1", the slot is valid.
All bit in slot 5-12 is "0".

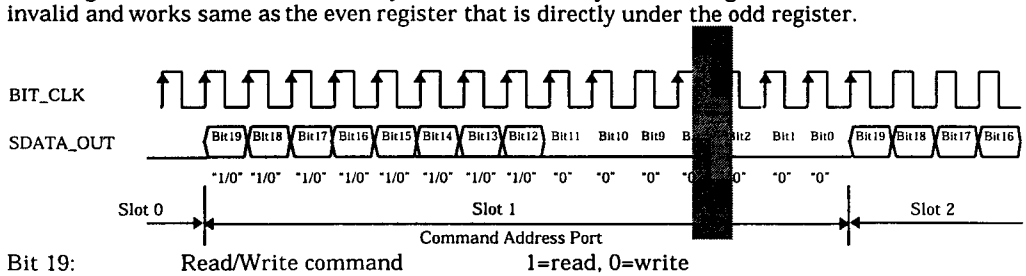
A new audio output frame begins with a low to high transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. On the immediately following falling edge of BIT_CLK, the AK4542 samples the assertion of SYNC. This falling edge marks the time when both sides of AC-link are aware of the start of a new audio frame. On the next rising of BIT_CLK, the AC '97 controller transitions SDATA_OUT into the first bit position of slot 0 (Valid Frame bit). Each new bit position is presented to AC-link on a rising edge of BIT_CLK, and subsequently sampled by the AK4542 on the following falling edge of BIT_CLK. This sequence ensures that data transitions, and subsequent sample points for both incoming and outgoing data streams are time aligned.

Data is output from the AC'97 controller with MSB first through SDATA_OUT pin

Valid frame bit in the slot 1 is 1 if at least 1 slot is valid("1"). If all of slot1, slot2, slot 3, and slot4 are invalid, valid frame bit should be "0". The following table shows the relationship of valid bits and the Read/Write operation.

Slot 1 Valid Bit (Command Address)	Slot 2 Valid Bit (Command Data)	Read/Write Operation
1	1	Read/Write (Normal Operation)
0	1	Ignore
1	0	Read: Normal Operation, Write: Ignore
0	0	Ignore

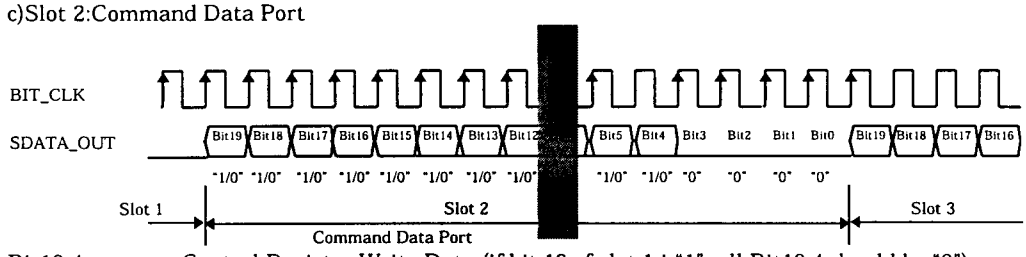
b)Slot 1:Command Address Port
This slot shows the address of command data, which is showed in the slot 2. The AK4542 has 19 words of 16-bit valid registers, addressable on even byte boundaries. Only the even registers are valid, the access to odd register is invalid and works same as the even register that is directly under the odd register.



Bit 19: Read/Write command 1=read, 0=write
Bit 18:12 Control Register Index (see "Mixer Registers for the detail)
Bit 11:0 Reserved ("0")

Bit 18 is equivalent to the most significant bit of the index address data.
The AK4542 ignore the bits which are from bit 11 to bit 0.

c)Slot 2:Command Data Port



Bit19:4 Control Register Write Data (if bit 19 of slot 1 is"1", all Bit19:4 should be "0")
Bit3:0 Reserved("0")

If the bit 19 in the slot 1 is "0",AC'97 controller must output Command Data Port data to the slot ***in the same frame***. If the bit 19 in the slot 1 is "1", the AK4542 discard Command Data Port data.

Bit 19 is equivalent to D15 bit of mixer register value.

d)Slot 3 PCM Playback Left Channel (16bits)
Playback(DAC) data format is MSB first. Data format is 2's complement. As the resolution of the AK4542 is 16bit, lower 4 bits are ignored. AC97 controller should stuff bit3-0 with"0". If valid bit (slot 3) in the slot 0is invalid ("0"), the AK4542 interprets the data as all "0".
Bit19:4 Playback data
Bit 3:0 "0"

e)Slot 4 PCM Playback Right Channel (16bits)
Playback data format is MSB first. Data format is 2's complement. As the resolution of the AK4542 is 16bit, lower 4 bits are ignored. AC97 controller should stuff bit3-0 with"0". If valid bit (slot 4) in the slot 0 is invalid ("0"), the AK4542 interprets the data as all "0".
Bit19:4 Playback data
Bit 3:0 "0"

f)Slot6-12 Reserved
The AK4542 ignores these slots. All bits should be stuffed with"0" by the AC'97 controller.

AC-link Input Frame(SDATA_IN)

Each AC-link frame consists of 12 20-bit slots and 1 16-bit special tag phase.

a)Slot 0

Slot 0 is a special time frame, and consists of 16 bit. Slot 0 is also named as Tag phase. The AK4542 supports from Bit 0 to Bit 4. Each bit means "1"=valid(normal operation) or ready,"0"=invalid(abnormal operation) or not ready. If the first bit in the slot 0 is valid, the AK4542 is ready for normal operation.[3] If the "Codec Ready" bit is invalid, the following bits and remaining slots are all "0". AC'97 controller should ignore the following bits in the slot 0 and all other slots. If the bit is "1", the next 12 bits corresponding 12 slots are valid.

Bit 1 means that Slot 1(Status Address) output is valid or invalid. And Bit 2 means that Slot 2(Status Data) is valid or invalid.

The following table shows the relationship between Bit 1,2 and each Status of the AK4542.

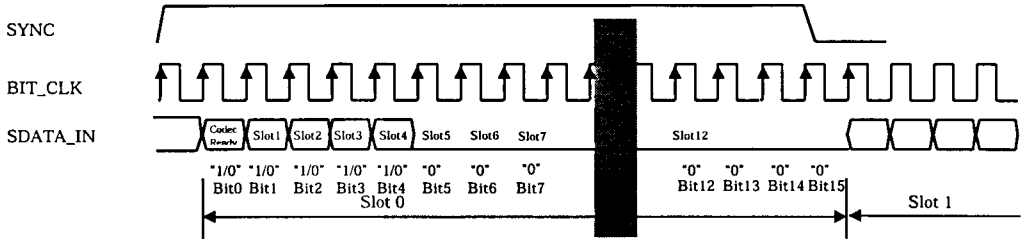
Bit 1 (Status Address)	Bit 2 (Status Data)	Status
1	1	There is a Read Command in the previous frame. Then both Slot 1 and Slot 2 output the normal data.
1	0	Though there is a Read Command in the previous frame, thepointed Register is not supported. Slot 1 outputs the StatusAddress(Echo of Register index for which data is being returned). Slot 2 is stuffed with All "0"'s.
0	0	There is no Read Command in the previous frame. Both Slot 1 and Slot 2 output All"0".
0	1	Prohibited or non-existing

Note 1). In case of Status Address of odd number (N=2n+1) is pointed out to read, the AK4542responds Status Address of even number(N=2n). In this case, the AK4542 judges that this Read Command is CORRECT, and outputs Bit 1 ="1".

2). The above Read sequence isdone as response for just one frame previous read command. That is, if the previous frame is the Write Command, AK4542 outputs Bit 1 ="0", Bit 2 ="0" and Slot 1&2 = All"0".

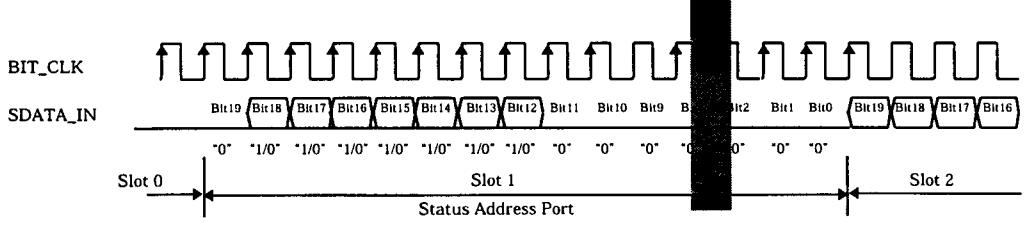
Bit 3 means the output of Slot 3(PCM(adc) Left) is valid or invalid. And Bit 4 means the output of Slot 4(PCM(adc)Left) is valid or invalid.

A new audio input frame begins with a low to high transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. On the immediately following falling edge of BIT_CLK, the AK4542 samples the assertion of SYNC. This falling edge marks the time when both sides of AC-link are aware of the start of a new audio frame. On the next rising of BIT_CLK, the AK4542 transitions SDATA_IN into the first bit position of slot 0 ("Codec Ready" bit). Each new bit position is presented to AC-link on a rising edge of BIT_CLK, and subsequently sampled by the AC '97 controller on the following falling edge of BIT_CLK. This sequence ensures that data transitions, and subsequent sample points for both incoming and outgoing data streams are time aligned.



b)Slot 1 Status Address Port

Audio input frame slot 1's stream echoes the control register index, for historical reference, for the data to be returned in slot 2 (Assuming that slots 1 valid bit and slot 2 valid bit in the slot 0 had been tagged "valid" by the AK4542)



[3] When the AC'97 is not ready for normal operation, output bits are not specified in the documents.

This address shows register index for which data is being returned in the slot 2.
This address port is the copy of slot 1of output frame, and index address input to SDATA_OUT is loop backed to AC'97 controller through SDATA_IN.

b)Slot 2:Status Data Port
Status data addressed by command address port of Output Stream is output through SDATA_IN pin.
If slot 2 bit in the Tag Phase is invalid, all bits are stuffed with"0".
Bit19:4 Control Register Read Data (the contents of indexed address in the slot 1)
Bit3:0 "0"

Note that the address of Status Data Port data are consistent with Status Address Port data of the slot 1 ***in the same frame***. If the read operation is issued inthe frame N by AC'97 controller, Status Data Port data is output through SDATA_IN in the frame N+1. **Note that data is output in only this frame, only one time and that the following frames are invalid if the next read operation is not issued.**

c)Slot 3 PCM Record Left Channel
Record(ADC) data format is MSB first. Data format is 2's complement. As the resolution of the AK4542 is 16bit, lower 4 bits are ignored. If ADC block is powered down, slot-3 valid bit in the slot 0 is invalid ("0"), and data is output as all "0".

Bit19:4 Audio ADC left channel output
Bit3:0 "0"

d)Slot 4 PCM Record Right Channel
Record(ADC) data format is MSB first. Data format is 2's complement. As the resolution of the AK4542 is 16bit, lower 4 bits are ignored. If ADC block is powered down, slot-4 valid bit in the slot 0 is invalid ("0"), and data is output as all "0".
Bit19:4 Audio ADC right channel output
Bit3:0 "0"

e)Slot 5 Modem Line Codec
As the AK4542 does not incorporate modemcodec, all bits are stuffed with"0".
Bit19:0 "0"

f)Slot 6 Microphone Record Data
As the AK4542 does not incorporate 3d ADC codec, all bits are stuffed with"0".
Bit19:0 "0"

g)Slot 7-12 Reserved
Bits19:0"0"

■Mixer Registers
Each Register is 16 bit wide.
Note: The AK4542 outputs all "0" if the controller reads an unused or invalid register address

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	Reset	0	"0"	"1"	"0"	"1"	"1"	"0"	"0"	"0"	"0"	"0"	"1"	"0"	"0"	"0"	"0"	2C10h
02h	Master Volume	Mute	X	ML5	ML4	ML3	ML2	ML1	ML0	X	X	MR5	MR4	MR3	MR2	MR1	MR0	8000h
04	LINVL Volume	Mute	X	ML5	ML4	ML3	ML2	ML1	ML0	X	X	MR5	MR4	MR3	MR2	MR1	MR0	8000h
06h	Master Volume Mono	Mute	X	X	X	X	X	X	X	X	X	MR5	MR4	MR3	MR2	MR1	MR0	8000h
0Ah	PC_BEEP Volume	Mute	X	X	X	X	X	X	X	X	X	X	PV3	PV2	PV1	PV0	X	0000h
0Ch	Phone Volume	Mute	X	X	X	X	X	X	X	X	X	X	GN4	GN3	GN2	GN1	GN0	8008h
0Eh	Mic Volume	Mute	X	X	X	X	X	X	X	X	20dB	X	GN4	GN3	GN2	GN1	GN0	8008h
10h	Line In Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
12h	CD Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
14h	Video Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
16h	Aux Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
18h	PCM Out Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
1Ah	Record Select	X	X	X	X	X	SL2	SL1	SL0	X	X	X	X	X	SR2	SR1	SR0	0000h
1Ch	Record Gain	Mute	X	X	X	GL3	GL2	GL1	GL0	X	X	X	X	GR3	GR2	GR1	GR0	8000h
20h	General Purpose	POP	X	3D	X	X	X	MIX	MS	LPBK	X	X	X	X	X	X	X	0000h
22h	3D Control	X	X	X	X	X	X	X	X	X	X	X	X	X	X	DP1	DP0	0000h
26h	Powerdown Ctrl/Stat	X	PR6	PR5	PR4	PR3	PR2	PR1	PR0	X	X	X	X	REF	ANL	DAC	ADC	na
7Ch	Vendor ID1	"0"	"1"	"0"	"0"	"0"	"0"	"0"	"1"	"0"	"1"	"0"	"0"	"1"	"0"	"1"	"1"	414Bh
7Eh	Vendor ID2	"0"	"1"	"0"	"0"	"1"	"1"	"0"	"1"	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"1"	4D01h

*) Vender ID of AKM is "AKM" :This ID has been approved by Microsoft.
*) The AK4542 outputs "X" bits as "0".
*) A write to "Invalid" registers does not affect operation of the AK4542.
*) ANL, DAC, ADC Bit in register 26h are all "0" just after Cold Reset. When each section is ready for normal operation, the coresponding bit becomes "1". The Powerdown register(26h) is not affected by a write to Reset register(0h). See "Mixer Registers" in AC'97 specification for details. Vref is controlled only by PR3.

■Reset Register (Index 00h)
<Write>
When any value is written to the AK4542, all registers in the AK4542 except for 26h Powerdown/Control Register are reset to default values. The value of this register is not altered.
<Read>
Reading this register returns "2C10h" composed of the ID code of the part and a code for the type of 3D enhancement and a code for True Line Level Out.
*Setting D14 – D10 "01011" means AKM 3D enhancement which is registered in AudioCodec '97 Component Specification Rev 1.03 .
*Setting D4 "1" means True Line Level Out is supported with Volume Control(Index 04h).

■ Play Master Volume Registers (Index 02h, 06h)

The following table shows the relationship between bits and the attenuation value. Attenuation step is 1.5dB.
The AK4542 does not support optional MX5 bit. The AK4542 detects when that bit is set and set all 4 LSBs to 1s.
Example: When the driver writes a "1xxxxx" the AK4542 interpret that as "011111". When this register is read, the return value is "01111".

Mute	MX5	MX4	MX3	MX2	MX1	MX0	Att.
0	0	0	0	0	0	0	0dB
0	0	0	0	0	0	1	-1.5dB
0	0	0	0	0	1	0	-3.0dB
0	0	0	0	0	1	1	-4.5dB
0	0	1	1	1	1	0	-45.0dB
0	0	1	1	1	1	1	-46.5dB
0	1	X	X	X	X	X	-46.5dB
1	X	X	X	X	X	X	Mute

■ Play LINVL(True Line Level Out)Volume Registers (Index04h)

The following table shows the relationship between bits and the attenuation value. Attenuation step is 1.5dB.

The AK4542 does not support optional MX5 bit. The AK4542 detects when that bit is set and set all 4 LSBs to 1s. Example: When the driver writes a "1xxxxx" the AK4542 interpret that as "011111". When this register is read, the return value is "01111".

Mute	MX5	MX4	MX3	MX2	MX1	MX0	Att.
0	0	0	0	0	0	0	0dB
0	0	0	0	0	0	1	-1.5dB
0	0	0	0	0	1	0	-3.0dB
0	0	0	0	0	1	1	-4.5dB
0	0	1	1	1	1	0	-45.0dB
0	0	1	1	1	1	1	-46.5dB
0	1	X	X	X	X	X	-46.5dB
1	X	X	X	X	X	X	Mute

■ PC Beep Register (Index 0Ah)

The following table shows the relationship between bits and the attenuation value. Attenuation step is 3dB. PC_BEEP of the AK4542 is mute off at default state.

The PC Beep is routed to L & R Line outputs directly when AK4542 is in a RESET State(Reset# is "L"). This is so that Power on Self Test(POST) codes can be heard by the user in case of a hardware problem with the PC. After Reset# goes "H", direct PC beep pass thru becomes OFF.

Mute	PV3	PV2	PV1	PV0	Att.
0	0	0	0	0	0dB
0	0	0	0	1	-3.0dB
0	0	0	1	0	-6.0dB
0	1	1	1	1	-45.0dB
1	X	X	X	X	Mute

■ Analog Mixer Input Gain Registers (Index 0Ch-18h)

The following table shows the relationship between bits and the gain/attenuation value. Attenuation step is 1.5dB.

Mute	Gx4	Gx3	Gx2	Gx1	Gx0	Att.
0	0	0	0	0	0	+12dB
0	0	0	0	0	1	+10.5dB
0	0	1	0	0	0	0dB
0	0	1	0	0	1	-1.5dB
0	1	1	1	1	0	-33.0dB
0	1	1	1	1	1	-34.5dB
1	X	X	X	X	X	Mute

■ Record Select Control Register (Index 1Ah)

SR2	SR1	SR0	Att.
0	0	0	Mic
0	0	1	CD In (R)
0	1	0	Video In (R)
0	1	1	Aux In (R)
1	0	0	Line In (R)
1	0	1	Stereo Mix (R)
1	1	0	Mono Mix
1	1	1	Phone

SR2	SL1	SL0	Att.

0	0	0	Mic
0	0	1	CD In (L)
0	1	0	Video In (L)
0	1	1	Aux In (L)
1	0	0	Line In (L)
1	0	1	Stereo Mix (L)
1	1	0	Mono Mix
1	1	1	Phone

■ Record Gain Register (Index 1Ch)

Mute	Gx3	Gx2	Gx1	Gx0	Gain
0	0	0	0	0	0dB
0	0	0	0	1	1.5dB
0	0	0	1	0	3.0dB
0	1	1	1	1	22.5dB
1	X	X	X	X	Mute

■ General Purpose Register (Index 20h)

The following table shows the relationship between the bit and control for several miscellaneous functions of the AK4542.

Bit	Function
POP	PCM(DAC) Bypass 3D 0= Via 3D Pass, 1= 3D Bypass
3D	3D Stereo Enhancement 0=Off, 1=On
MIX	Mono Output Select 0=Mix, 1=Mic
MS	Mic Select 0=Mic1, 1 =Mic2
LPBK	ADC/DAC Loopback Mode 1= Loopback

The POP bit controls the routes of PCM out(DAC) by way of 3D Pass and by 3D Bypass.
And the 3D bit is to control the AKM 3D enhancement on and off.
LINVL_OUT_L/R is true line_out from DAC which does not pass through 3D Stereo Enhancement Circuit.
In addition, note that PCM out(DAC) is not output from LINVL_OUT_L/R when POP bit is 1.

■ 3D Control Register (Index 22h)

The following table shows the relationship between the bit and 3D Depth.

DP1	DP0	Depth	Recommended Application
0	0	0%	Off
0	1	50%	Audio
1	0	70%	Audio
1	1	100%	Game

■ Powerdown Control/Status Register (Index 26h)

Bit	Function
REF	Vrefs up to normal state 0=NOT ready, 1=ready,
ANL	Analog mixers, etc ready 0=NOT ready, 1=ready
DAC	DAC section ready to accept data 0=NOT ready, 1=ready
ADC	ADC section ready to transmit data 0=NOT ready, 1=ready

Any write to this register does not affect the state of the above bits.

Bit	Function

PR0	PCM in ADC's & Input Mux Powerdown
PR1	PCM out DACs Powerdown
PR2	Analog Mixer Powerdown (Vref still on)
PR3	Analog Mixer Powerdown (Vref off)
PR4	Digital Interface (AC-link) Powerdown
PR5	Internal Clk disable
PR6	True Line Level Out Powerdown

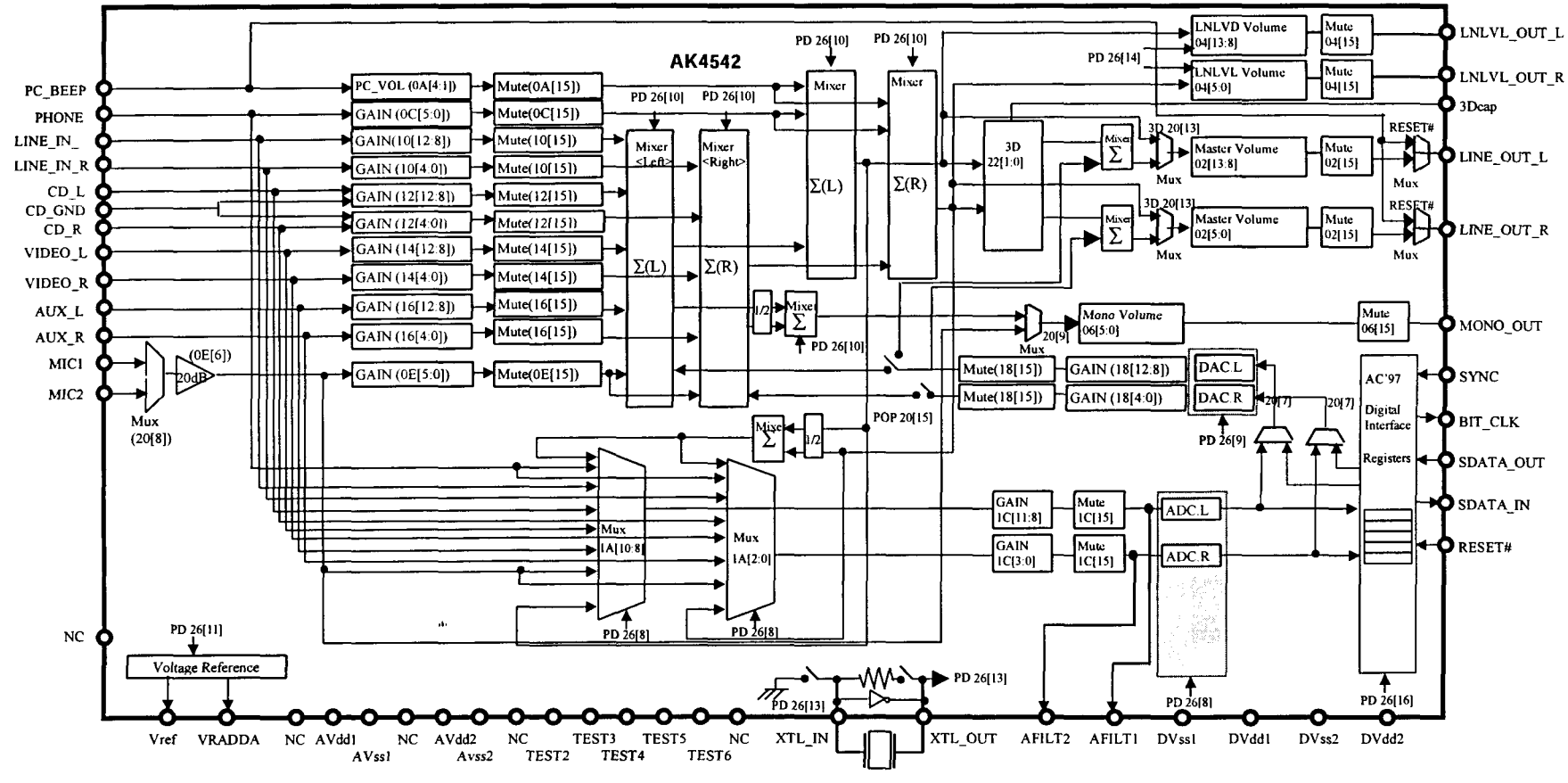
When PR3 bit is set to "1", ADC, DAC, Mixer, and VREF are powered down even if any PRx bit are "0". When PR3 bit is reset to "0", the AK4542 resumes the previous state by referencing PRx bit. In this case, the AK4542 outputs corresponding slot-x valid bits in the slot 0 as "0" until the AK4542 is power-up.

■ Vendor ID Registers (Index 7Ch 7Eh)

This register is for specific vendor identification if so desired. The ID method is Microsoft Plug and Play Vendor ID code with upper byte of 7Ch register, the first character of that id, lower byte of 7Ch register, the second character and upper byte of 7Eh register the third character. These three characters are ASCII encoded. Lower byte of 7E register is for the Vendor Revision number.

AKM's vender ID is "AKM", and revision number is 0. As ASCII code "A" is 41h, "K" is 4Bh, and "M" is 4Dh, Vendor ID registers are 414Bh and 4D0h respectively.

AK4542 Block Diagram



■Power Management/Low Power Modes

The AK4542 is capable of operating at reduced power when no activity is required. The state of power down is controlled by the Powerdown Register (26h). There are 7 commands of separate power down. See the table below for the different modes. As the AK4542 operate at static mode, the registers will not lose their values even if the clock is stopped .

Powerdown Mode Truth Table

	ADC	DAC	Mixer	VREF	ACLINK	Internal CLK	LNLVL_OUT
PR0="1"	PD	don't care	don't care	don't care	don't care	don't care	don't care
PR1="1"	don't care	PD	don't care	don't care	don't care	don't care	don't care
PR2="1"	don't care	don't care (No DAC out)	PD	don't care	don't care	don't care	PD
PR3="1"	PD	PD	PD	PD	don't care	don't care	PD
PR4="1"	PD	PD	don't care	don't care	PD	don't care	don't care
PR5="1"	PD	PD	don't care	don't care	PD	PD	don't care
PR6="1"	don't care	don't care	don't care	don't care	don't care	don't care	PD

*: PD means Powerdown .

*: No DAC out means that there is no PCM out because mixer stops.

From normal operation sequential writes to the Powerdown Register are performed to power down the AK4542 a piece at a time. After everything has been shut off, a final write (of PR4) can be executed to shut down the AC '97 digital interface (AC-link). The part will remain in sleep mode with all its registers holding their static values. To wake up, the AC '97 controller will send pulse on the sync line issuing a warm reset. This will restart the AK4542 digital (resetting PR4 to zero). The AK4542 can also be woken up with a cold reset. A cold reset will cause a loss of values of the registers as a cold reset will set them to their default states. When a section is powered back on the Powerdown Control/Status register (index 26h) should be read to verify that the section is ready (i.e. stable) before attempting any operation that requires it.

The above table shows the transition of powerdown and powerup states.
When PR3 bit is set to "1", ADC, DAC, Mixer, and VREF are powered down even if any PRx bit are "0". When PR3 bit is reset to "0", the AK4542 resumes the previous state by referencing PRx bit. In this case, the AK4542 outputs "0" (invalid) for corresponding slot-x valid bits in the slot 0 until the corresponding block of the AK4542 is power-up.
Setting PR4 bit cause the Powerdown mode of AK4542 and AC-Link of AK4542 shut down. In this case, when Warm reset is executed, PR4 bit is cleared and AC-Link is reactivated. Meanwhile Cold reset is selected, AK4542 is restored to the operation with default register setting.
In addition, setting PR5 bit causes the Powerdown mode of AK4542 and the internal clock of AK4542 is stopped. When Warm reset is done in this case, PR5 bit is cleared to 0 and internal clock and AC-Link are reactivated. When Cold reset is executed, AK4542 is set up to the operation with default register setting.

■**Testability**

Activating the Test Modes

AC '97 has two test modes. One is for ATE in circuit test and the other is for vendor specific tests. AC '97 enters the ATE in circuit test mode regardless of SYNC signal (high or low) if SDATA_OUT is sampled high at the trailing edge of RESET#. If AC '97 enters AKM test mode when coming out of RESET if SYNC is high with SDATA_OUT low. These cases will never occur during standard operating conditions.

Regardless of the test mode, the AC '97 controller must issue a "Cold" reset to resume normal operation of the AC '97 Codec.

Test Mode Functions

ATE in circuit test mode

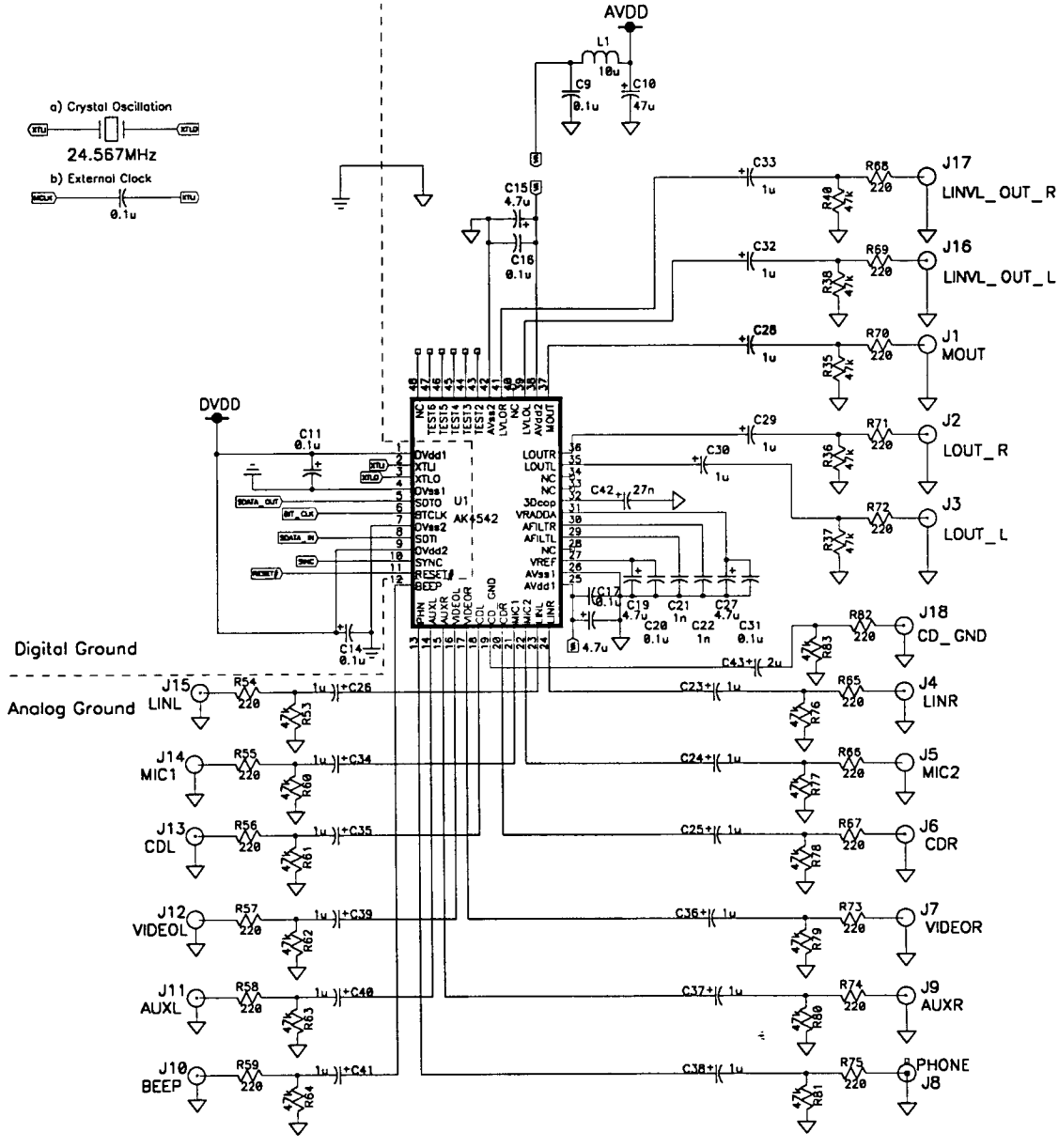
When AC '97 is placed in the ATE test mode, its digital AC-link outputs (i.e. BIT_CLK and SDATA_IN) are driven to a high impedence state. This allows ATE in circuit testing of the AC '97 controller.

Vendor Specific test mode

To be left up to the individual vendors.

System Design

The following figure shows the system connection diagram.



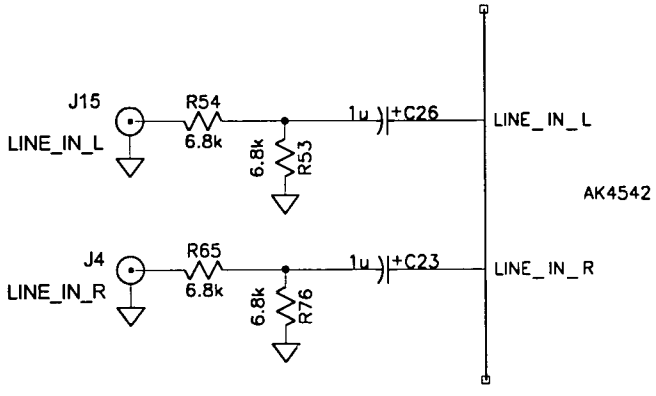
1.Grounding and Power SupplyDecoupling

AVdd1 and AVdd2 should be connectedand derived fromsame AVdd. Analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit boardDecoupling capacitors should be as near to the AK4542 as possible, with the small value ceramic capacitor being the nearest.

2. On-chip Voltage Reference
The on-chip voltagereference are output on the VRADDA,Vref pins fordecoupling. A electrolytic capacitor less than 10uF in parallel with a 0.1 uF ceramic capacitor attached to these pins eliminates the effects of high frequency noise. No load current may be drawn from VRADDA, andVref pins. All signals, especially clocks, should be kept away from the VRADDA, andVref pins in order to avoid unwanted coupling into modulators.

3. Master Clock
If the digital controller which operates at 3.3 volt supplies AK4542's master clock as external clock, insert AC-coupling capacitor(0.1μF) between XTAL_IN pin of the AK4542 and clock output pin of the digital controller. In this case, PR5 Bit should be set before the external clock stops.

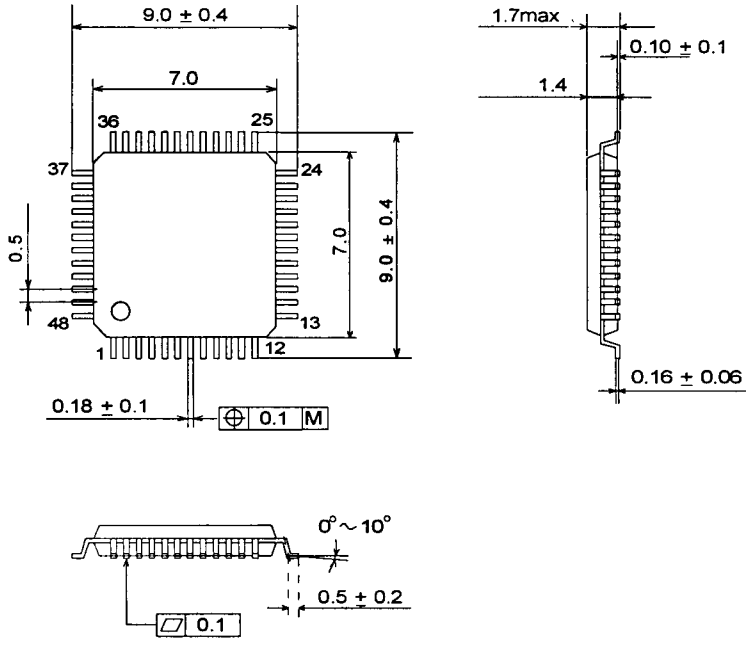
4.Anlog input
Since many analog levels can be as long as 2Vrms, the circuit shown below can be used to attenuate the analog input 2Vrms to 1Vrms which is the maximum voltage allowed for all the stereo line-level inputs.



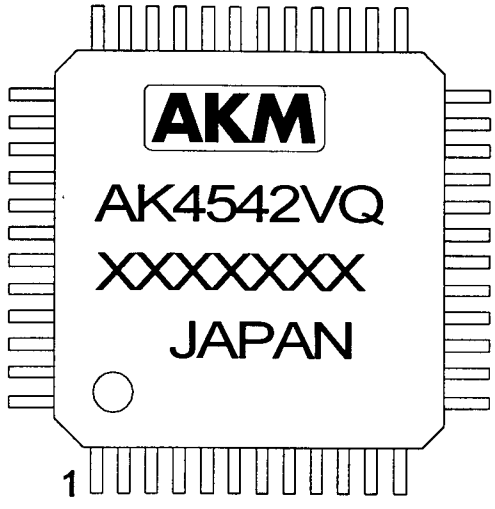
Analog Input

Package

48pin LQFP(Unit:mm)



Marking



1) Pin #1 indication
2) Date Code : XXXXXXX (7 digits)
3) Marketing Code : AK4542-VQ
4) Country of Origin
5) Asahi Kasei Logo

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  (b) A critical component is one whose failure to function or perform may reasonably be expected to result, whether directly or indirectly, in the loss of the safety or effectiveness of the device or system containing it, and which must therefore meet very high standards of performance and reliability.
- It is the responsibility of the buyer or distributor of an AKM product who distributes, disposes of, or otherwise places the product with a third party to notify that party in advance of the above content and conditions, and the buyer or distributor agrees to assume any and all responsibility and liability for and hold AKM harmless from any and all claims arising from the use of said product In the absence of such notification.