Product Brief

Intel® Ethernet Controller I211

Low-power, small-footprint, single-port gigabit network connectivity with advanced performance features.

Key Features

- One-Time Programmable Integrated Non-Volatile Memory and Integrated Switching Voltage Regulators for simplified board design and cost reduction
- Immutable firmware code built into the ROM inside the I211 eliminates firmware tampering or firmware replacement
- Innovative power management features including Energy Efficient Ethernet (EEE) and DMA Coalescing for increased efficiency and reduced power consumption
- Supports hardware-based timestamping of IEEE 1588 and 802.1AS packets enabling high-precision time synchronization over Ethernet
- Extended lifecycle support protects system investment by providing 7-year manufacturing availability for customers
- Low-Halogen[1], high-performance, low-power, small package, PCI Express 10/100/1000 Ethernet Connection

Overview

The Intel® Ethernet Controller I211-AT provides an ideal GbE solution for customers looking for a full-featured Gigabit Ethernet Media Access Control (MAC) and Physical-Layer (PHY) solution. With support for advanced features such as 802.3az Energy Efficient Ethernet (EEE), 802.1AS precision timestamping, ECC Packet Buffers and Integrated Non-Volatile Memory, the I211-AT provides an ideal GbE solution for Desktop, Consumer Electronics, and other small form-factor Embedded Applications.

The I211-AT uses a PCIe 2.1 one lane (x1) interface operating at 2.5 GT/s. This controller provides fully integrated GbE MAC/PHY capabilities that can be configured for either 1000 Mb/s or 10/100 Mb/s modes of operation.

Performance Optimization Capabilities

The Intel® Ethernet Controller I211-AT contains two transmit and two receive queues for the single port. These queues offer Error Correcting Memory (ECC) protection for improved data reliability. The controller efficiently manages packets with minimum latency by combining parallel and pipelined logic architectures optimized for these independent transmit and receive queues.

These queues, combined with Receive Side Scaling (RSS) and Message Signal Interrupt Extension (MSI-X) support, provide a toolset for optimizing the performance on multi-core processor designs.

Advanced interrupt-handling features to manage multiple interrupts simultaneously, combined with intelligent filtering, ordering, and directing of packets to specific queues and cores, enables load-balancing the network traffic flows to improve throughput in Multi-core platforms.

Advanced Features

IEEE 1588/802.1AS Timestamping
Supports hardware-based IEEE 1588/802.1AS to enable high-precision time synchronization over the Ethernet.

Software Definable Pins
Four Software Definable Pins (GPIOs) enable additional design customization for embedded platforms. SDPs can be used for IEEE 1588 auxiliary device connections, enable/disable of the device, and for other miscellaneous hardware or software-control purposes. These pins can be individually configured to act as either standard inputs, General-Purpose Interrupt (GPI) inputs or output pins, as well as the default value of all pins configured as outputs.

Energy Efficient Ethernet (EEE)
Supports the IEEE 802.3az EEE standard. During periods of low network activity, EEE reduces the power consumption of an Ethernet connection by negotiating with the switch port to transition to a low power idle (LPI) state.

Power is reduced to approximately 50 percent of its normal operating power, which saves power on both the network and the switch ports.

When increased traffic is detected, the controller and the switch quickly come back to full power to handle the increased traffic. EEE is supported for both 1000BASE-T and 100BASE-TX.

The I211-AT also has excellent thermal characteristics, supporting commercial temperature ranges from 0 °C to 70 °C, and operates at less than 730 mW.

Flexible Design Configurations

With its small size, reduced power control circuitry, and integrated NVM capability, this controller can be used for small form-factor embedded designs as well as consumer devices.

Packaged in an Environmentally Friendly Design

The I211-AT is low halogen and lead-free in its silicon and package design to reduce the potential for environmental impact.

Features	Description
External Interfaces	
PCI Express 2.1	• 2.5GT/s Support for x1 width (Lane)
Network Interfaces	• MDI (Copper) standard IEEE 802.3 Ethernet interface for 1000BASE-T, 100BASE-TX, and 10BASE-T applications (802.3, 802.3u, and 802.3ab)
BOM Cost Reduction	
On-chip integrated Switched Voltage Regulator (iSVR)	• Removes need for a higher cost onboard voltage regulator
Ethernet Features	
IEEE 802.3 autonegotiation	• Automatic link configuration for speed duplex and flow control
1Gb/s Ethernet IEEE 802.3, 802.3u, 802.3ab PHY specifications compliant	• Robust operation over installed base of CAT5 twisted-pair cabling
Integrated PHY for 10/100/1000 Mb/s for multi-speed, full, and half-duplex	• Smaller footprint and lower power dissipation compared to multiple discreet MAC and PHYs
IEEE 802.3x and IEEE 802.3z compliant flow control support with software-controllable Rx thresholds and Tx pause frames	• Local control of network congestion levels
Automatic cross-over detection function (MDI/ MDI-X)	• Frame loss reduced from receive overruns
IEEE 1588 protocol and 802.1AS implementation	• The PHY automatically detects which application is being used and configures itself accordingly • Timestamping and synchronization of time sensitive applications • Distribute common time to media devices
Power Management Features	
Controller is designed for low power consumption	• <730 mW S0-Max (state) 1000BASE-T Active 70 °C
IEEE 802.3az - Energy Efficient Ethernet (EEE)	• Power consumption by the PHY is reduced by approximately 50%; link transitions to low power Idle (LPI) state as defined in the IEEE 802.3az (EEE) standard
Smart power down (SPD) at S0 no link/Sx no link	• PHY powers down circuits and clocks that are not required for detection of link activity
Active State Power Management (ASPM)	• Optionality Compliance bit enables ASPM or runs ASPM compliance tests to support entry to L0s
LAN disable function	• Option to disable the LAN Port and/or PCIe Function.
Full wake up support	• Advanced Power Management (APM) Support [formerly Wake on LAN] - APM: Designed to receive a broadcast or unicast packet with an explicit data pattern (Magic Pack) and assert a signal to wake up the system • Advanced Configuration and Power Interface (ACPI) specification v2.0c - ACPI: PCIe power management based wake-up that can generate system wake-up events from a number of sources • Magic Packet wake-up enable with unique MAC address
ACPI register set and power down functionality supporting D0 and D3 states	• Power-managed speed control lowers link speed/power when highest link performance is not required
MAC Power Management controls	• Power management controls in the MAC /PHY enable the device to enter a low-power state
Low Power Link Up - Link Speed Control	• Enables a link to come up at the lowest possible speed in cases where power is more important than performance
Stateless Offloads and Performance Features	
TCP/UDP, IPv4 checksum offloads (Rx/ Tx/Large- send)	• More offload capabilities and improved CPU usage • Checksum and segmentation capability extended to new standard packet type
IPv6 support for IP/TCP and IP/UDP receive checksum offload	• Improved CPU usage
Tx TCP segmentation offload (IPv4, IPv6)	• Increased throughput and lower processor usage; compatible with large-send offload
Transmit Segmentation Offloading (TSO)	• Large TCP/UDP I/O is segmented by to the device it to L2 packets according to the requested MSS
Interrupt throttling control	• Limits maximum interrupt rate and improves CPU usage
Legacy and Message Signal Interrupt (MSI)	• Interrupt mapping
Message Signal Interrupt Extension (MSI-X)	• Dynamic allocation of up to 5 vectors per port
Intelligent interrupt generation	• Enhanced software device driver performance
Receive Side Scaling (RSS) for Windows Scalable I/O for Linux environments (IPv4, IPv6, TCP/UDP)	• Up to two queues per port • Improves the system performance related to handling of network data on multiprocessor systems
Support for packets up to 9.5 KB (Jumbo Frames)	• Enables faster and more accurate throughput of data
Low-Latency Interrupts	• Based on the sensitivity of the incoming data, the controller can bypass the automatic moderation of time intervals between the interrupts

Features	Description
Stateless Offloads and Performance Features (continued)	
Header/packet data split in receive	• Helps the driver to focus on the relevant part of the packet without the need to parse it
PCIe v2.1 TLP Processing Hint Requester	• Provides hints on a per transaction basis to facilitate optimized processing of
Descriptor ring management hardware for Transmit and Receive	• Optimized descriptor fetch and write-back for efficient system memory and PCIe bandwidth usage

Remote Boot Options

Preboot Execution Environment (PXE) flash interface support	• Enables system boot via the EFI (32-bit and 64-bit) • Flash interface for PXE 2.1 option ROM

Supported Operating Systems

The Feature Support Matrix for Intel® Ethernet Controllers includes a complete list of supported network operating systems.

Product Order Code

MM#	Brand Name	Description	Media	Product Order Code
925144	Intel® Ethernet Controller I211-AT	1000BASE-T Commercial Temp	tape and reel	WGI211-AT
925145	Intel® Ethernet Controller I211-AT	1000BASE-T Commercial Temp	tray	WGI211-AT

Warranty

Standard Intel limited warranty, one year. See Intel terms and conditions of sale for more details.

Product Information

For information about Intel® Ethernet Products and technologies, visit: intel.com/ethernetproducts

Customer Support

For customer support options in North America visit:
intel.com/content/www/us/en/support/contact-support.html

1. Low Halogen--Applies only to brominated and chlorinated flame retardants (BFRs/CFRs) and PVC in the final product. Intel components as well as purchased components on the finished assembly meet JS-709A requirements, and the PCB/Substrate meet IEC 61249-2-21 requirements. The replacement of halogenated flame retardants and/or PVC may not be better for the environment.

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