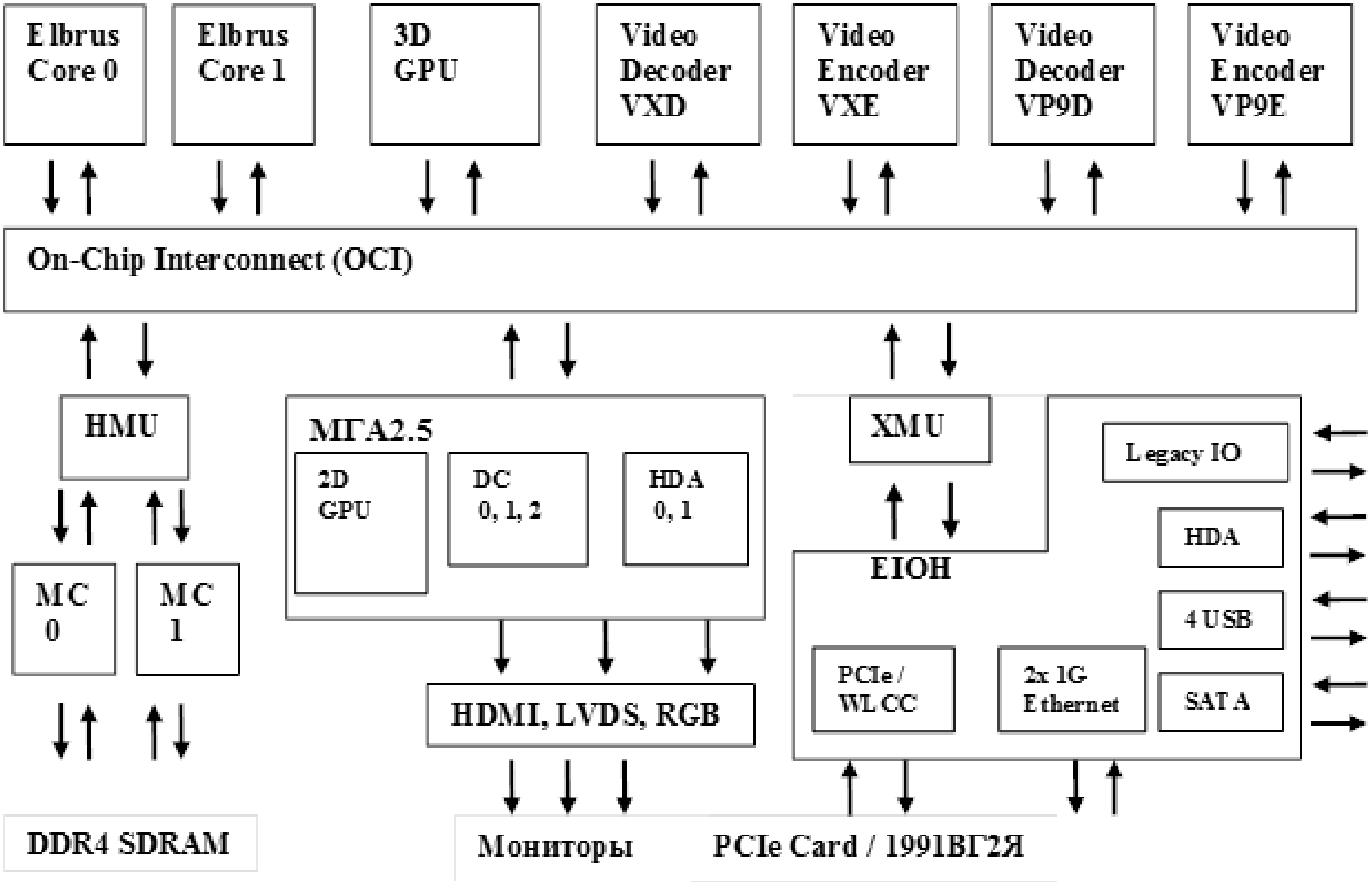
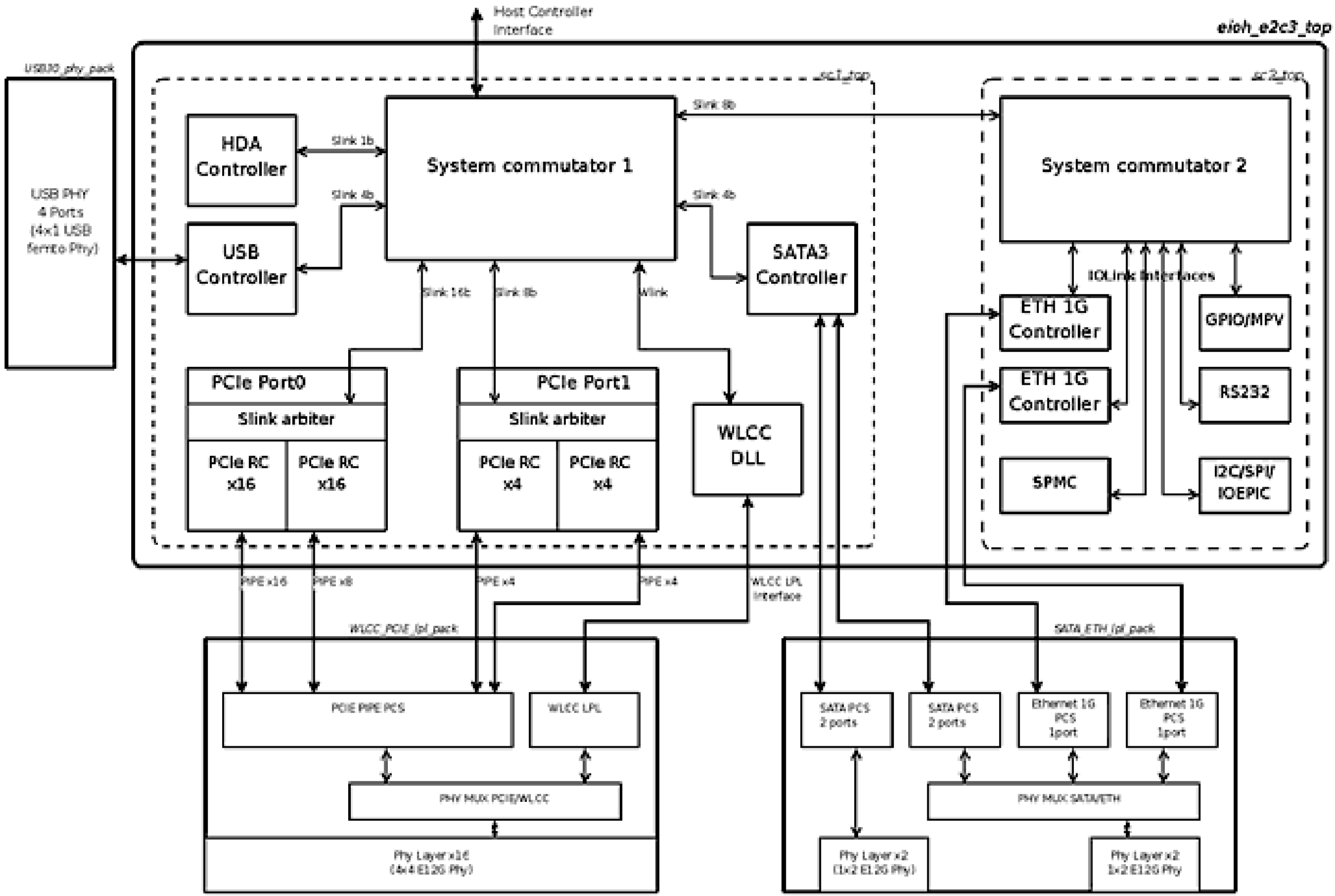
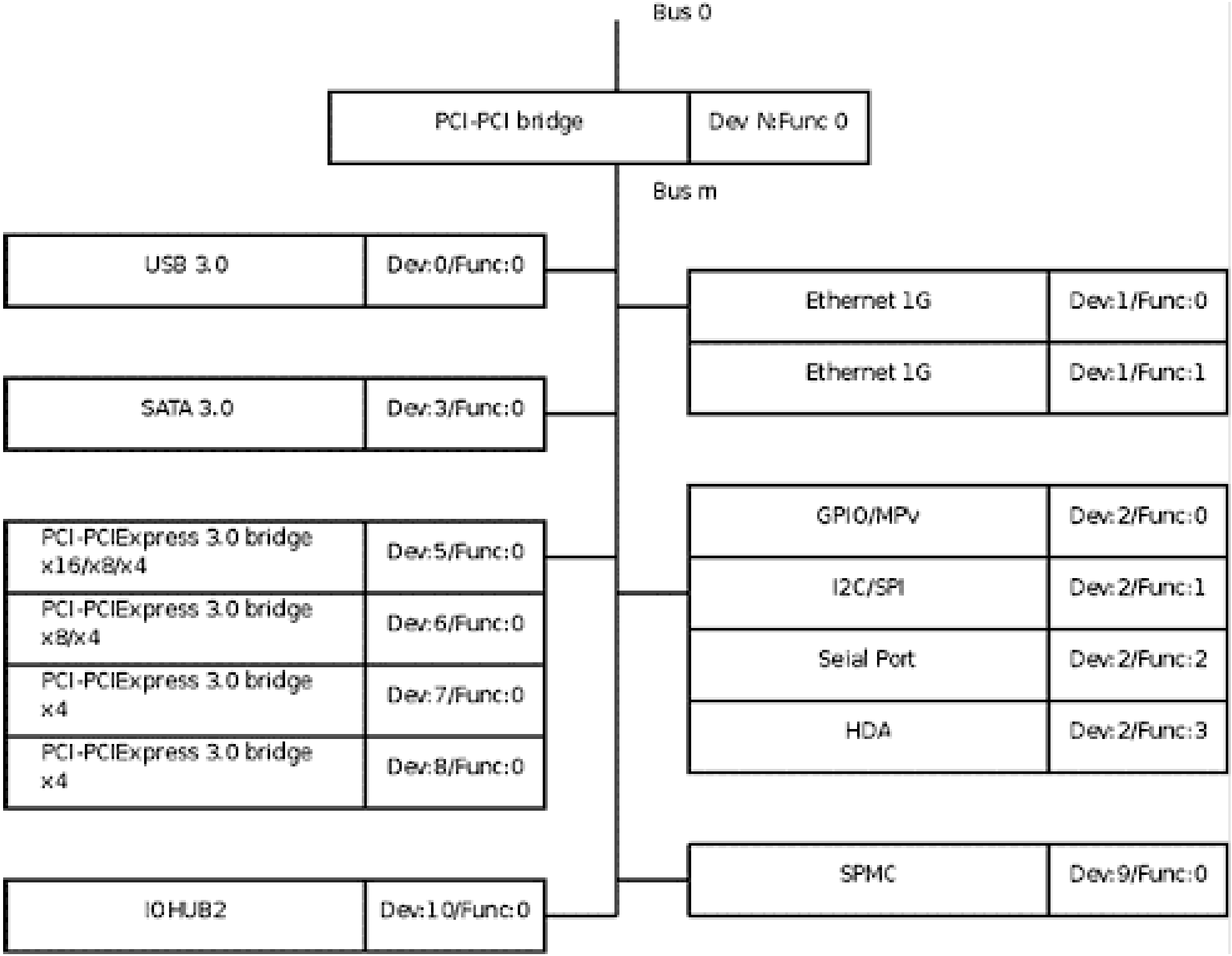
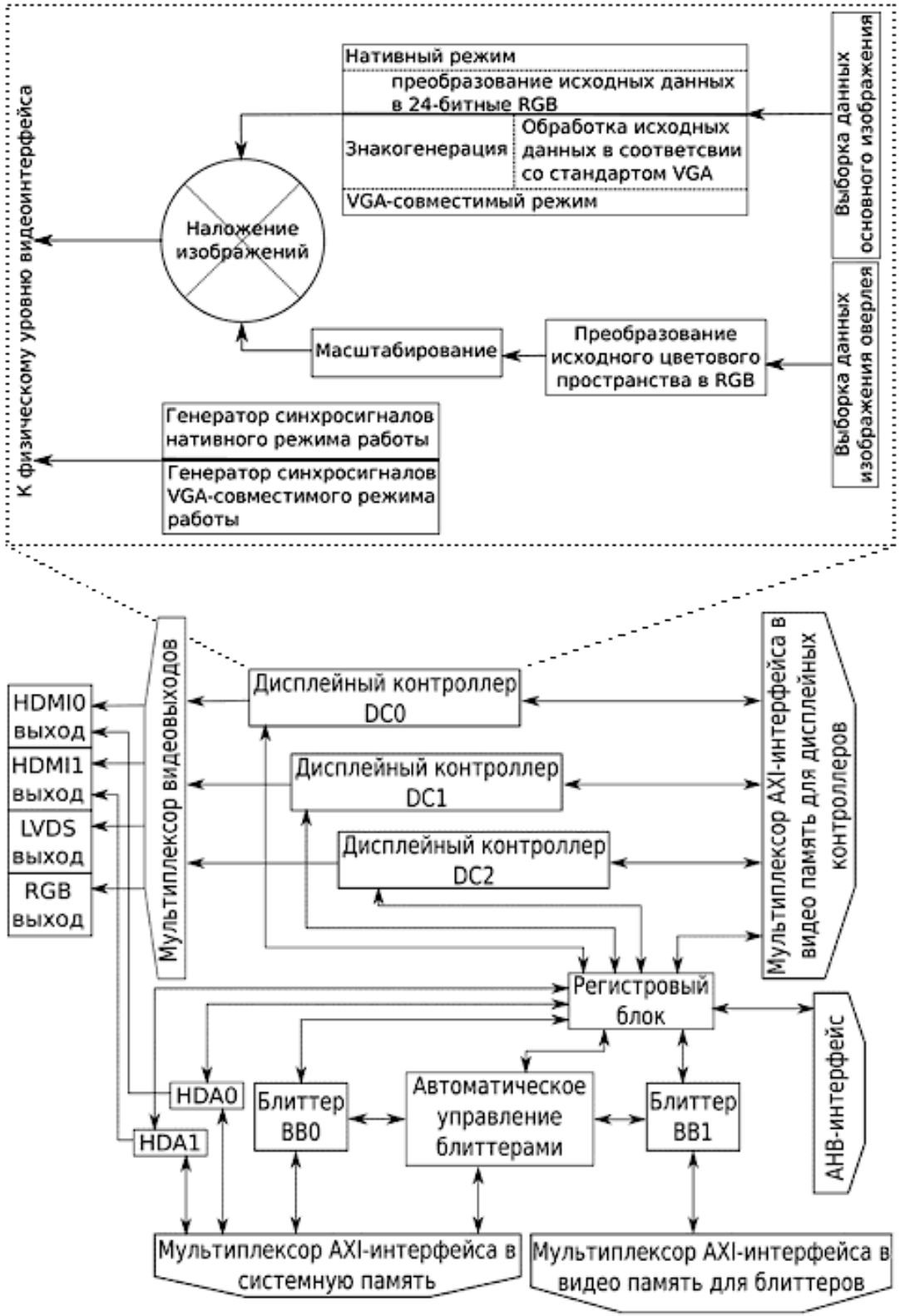
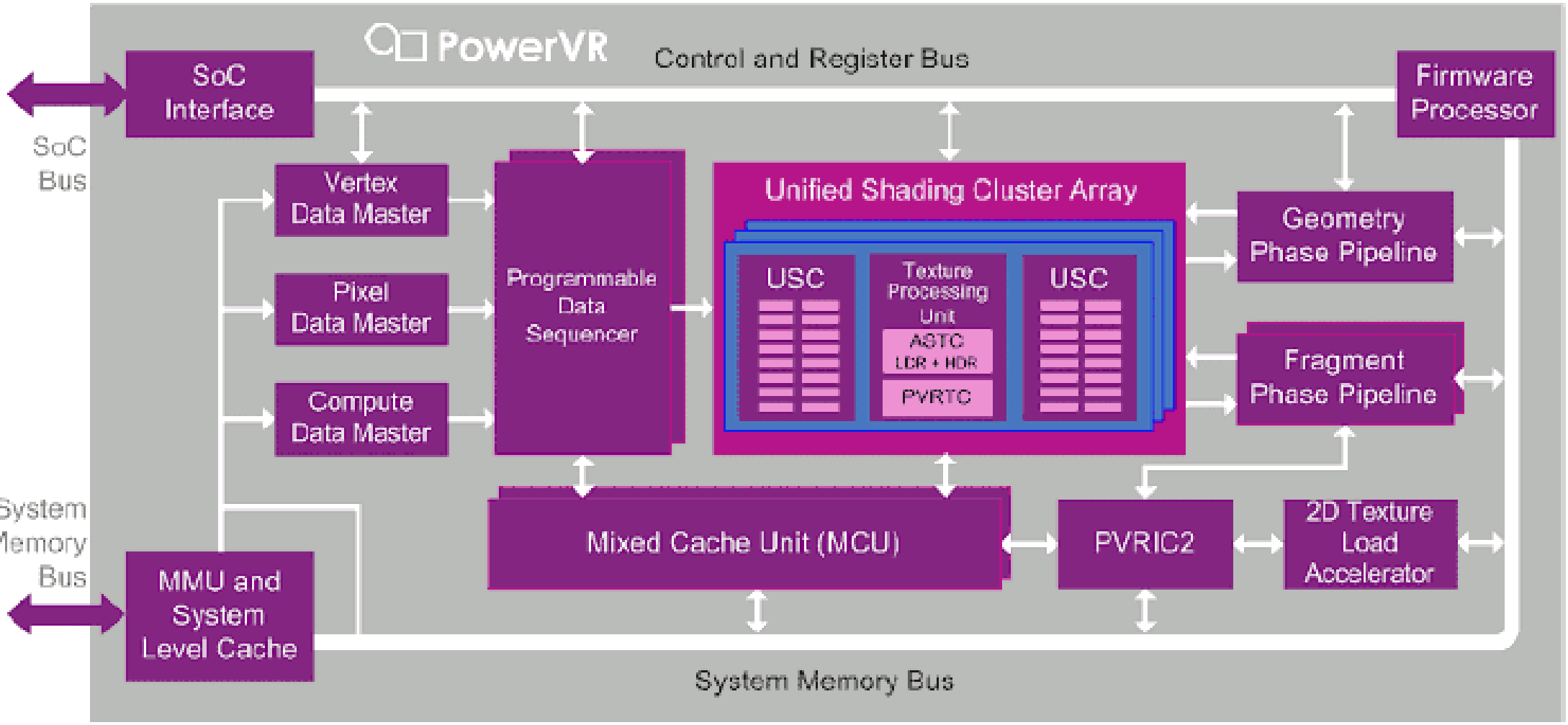
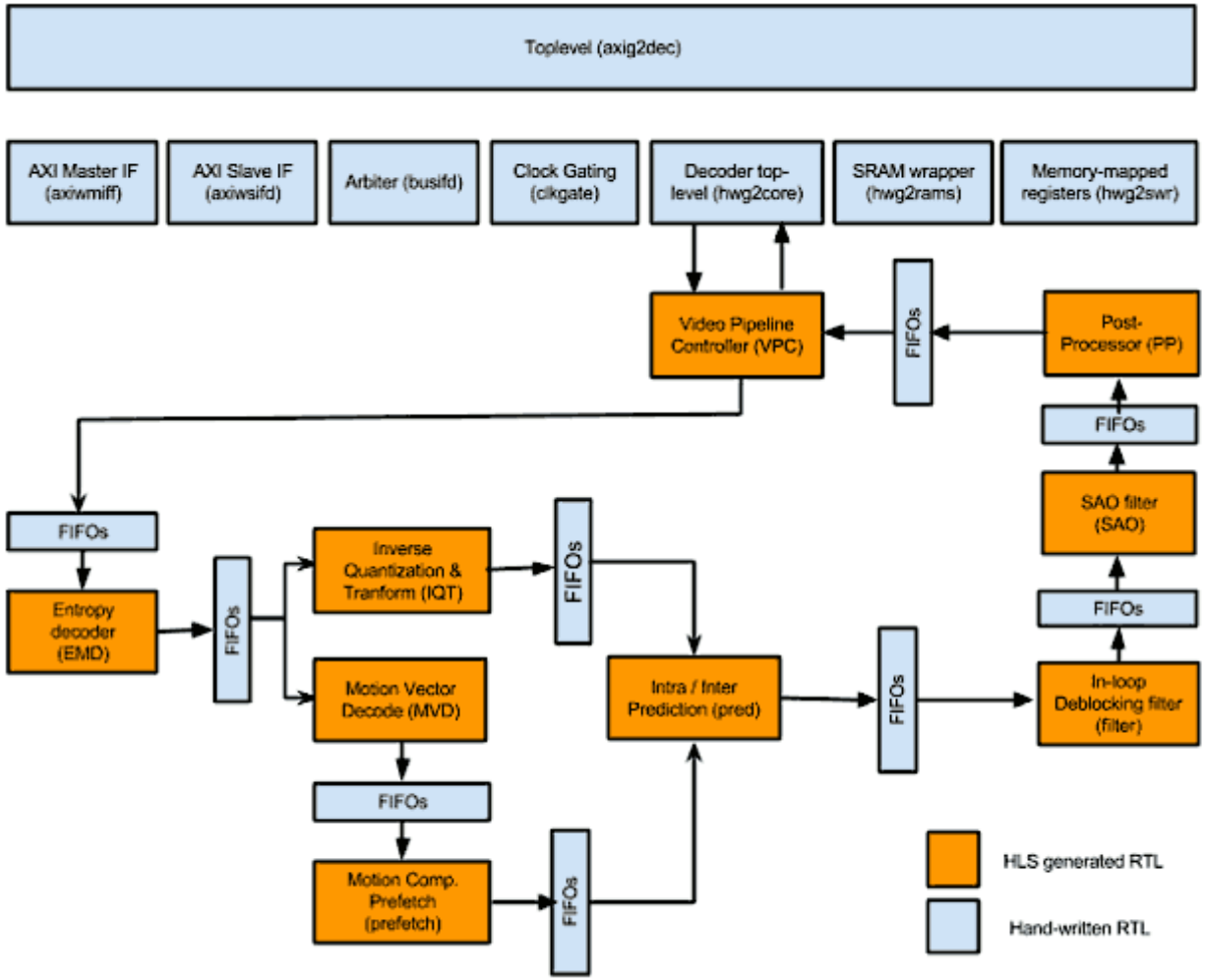

Elbrus Core 0
Elbrus Core 1
3D GPU
Video Decoder VXD
Video Encoder VXE
Video Decoder VP9D
Video Encoder VP9E
On-Chip Interconnect (OCI)
HMU
MC 0
MC 1
DDR4 SDRAM
МГА2.5
2D GPU
DC 0, 1, 2
HDA 0, 1
HDMI, LVDS, RGB
Мониторы
XMU
EIOH
Legacy IO
HDA
4 USB
SATA
PCIe / WLCC
2x 1G Ethernet
PCIe Card / 1991ВГ2Я

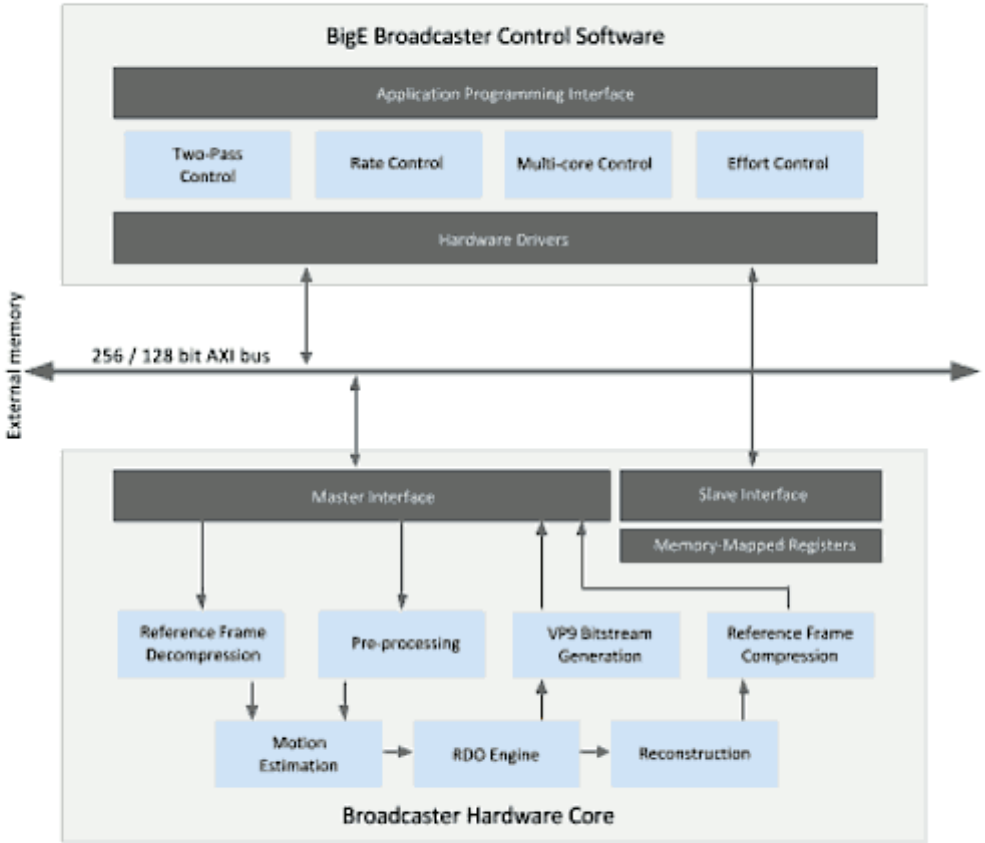

Host Controller Interface
eioh_e2c3_top
USB30_phy_pack
USB PHY 4 Ports (4x1 USB femto Phy)
sc1_top
sc2_top
HDA Controller
Slink 1b
System commutator 1
Slink 8b
System commutator 2
Slink 4b
Slink 4b
USB Controller
SATA3 Controller
IOLink Interfaces
Slink 16b
Slink 8b
Wlink
ETH 1G Controller
GPIO/MPV
ETH 1G Controller
RS232
PCIe Port0
Slink arbiter
PCIe RC x16
PCIe RC x16
PCIe Port1
Slink arbiter
PCIe RC x4
PCIe RC x4
WLCC DLL
SPMC
I2C/SPI/ IOEPIC
PIPE x16
PIPE x8
PIPE x4
PIPE x4
WLCC LPL Interface
WLCC_PCIE_pl_pack
SATA_ETH_pl_pack
PCIE PIPE PCS
WLCC LPL
PHY MUX PCIE/WLCC
Phy Layer x16 (4x4 E12G Phy)
SATA PCS 2 ports
SATA PCS 2 ports
Ethernet 1G PCS 1port
Ethernet 1G PCS 1port
PHY MUX SATA/ETH
Phy Layer x2 (1x2 E12G Phy)
Phy Layer x2 1x2 E12G Phy

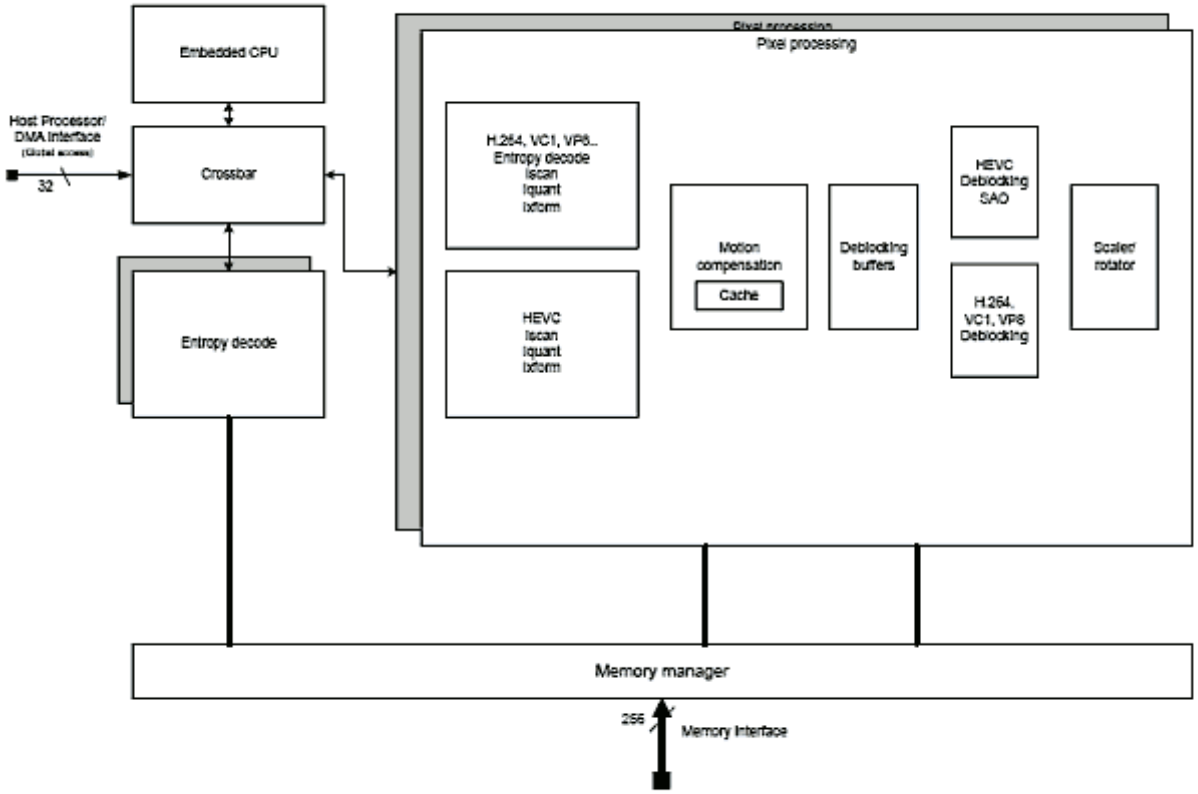

Bus 0
PCI-PCI bridge
Dev N:Func 0
Bus m
USB 3.0
Dev:0/Func:0
SATA 3.0
Dev:3/Func:0
PCI-PCIExpress 3.0 bridge x16/x8/x4
Dev:5/Func:0
PCI-PCIExpress 3.0 bridge x8/x4
Dev:6/Func:0
PCI-PCIExpress 3.0 bridge x4
Dev:7/Func:0
PCI-PCIExpress 3.0 bridge x4
Dev:8/Func:0
IOHUB2
Dev:10/Func:0
Ethernet 1G
Dev:1/Func:0
Ethernet 1G
Dev:1/Func:1
GPIO/MPv
Dev:2/Func:0
I2C/SPI
Dev:2/Func:1
Seial Port
Dev:2/Func:2
HDA
Dev:2/Func:3
SPMC
Dev:9/Func:0

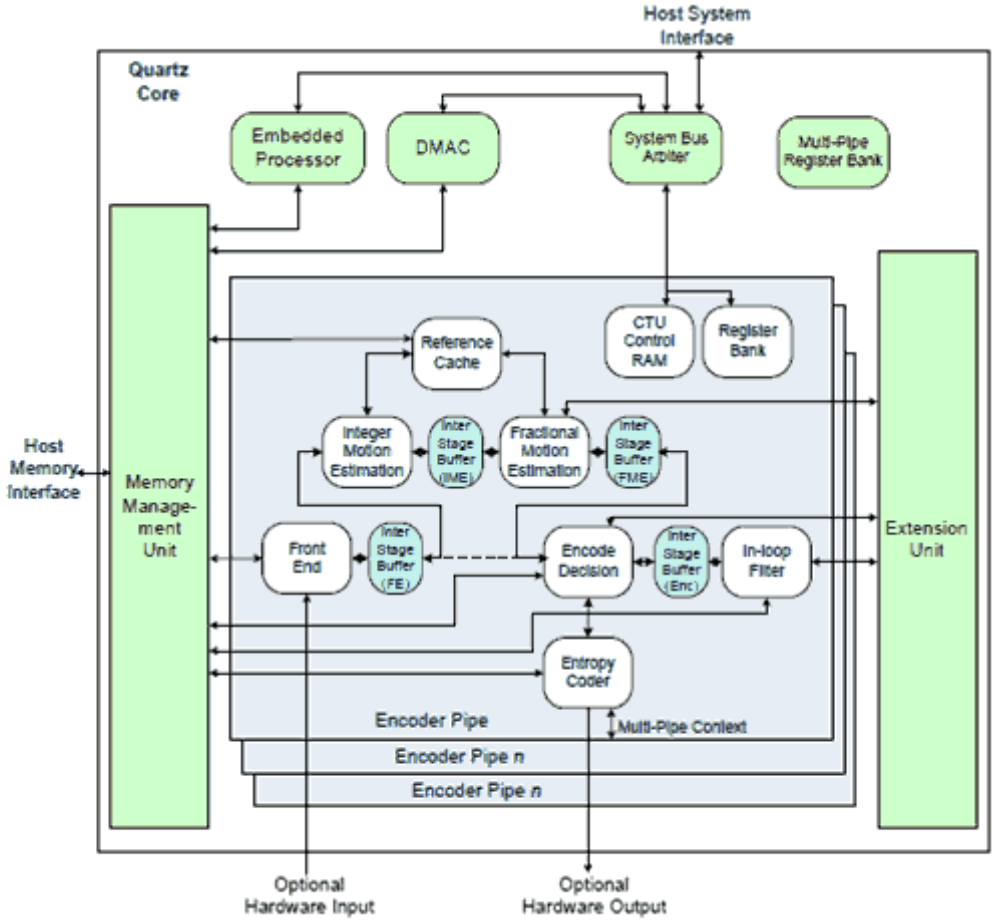

К физическому уровню видеоинтерфейса
Нативный режим
преобразование исходных данных в 24-битные RGB
Знакогенерация
Обработка исходных данных в соответсвии со стандартом VGA
VGA-совместимый режим
Выборка данных основного изображения
Наложение изображений
Масштабирование
Преобразование исходного цветового пространства в RGB
Выборка данных изображения оверлея
Генератор синхросигналов нативного режима работы
Генератор синхросигналов VGA-совместимого режима работы
HDMI0 выход
HDMI1 выход
LVDS выход
RGB выход
Мультиплексор видеовыходов
Дисплейный контроллер DC0
Дисплейный контроллер DC1
Дисплейный контроллер DC2
Мультиплексор AXI-интерфейса в видео память для дисплейных контроллеров
Регистровый блок
AHB-интерфейс
HDA0
HDA1
Блиттер BB0
Автоматическое управление блиттерами
Блиттер BB1
Мультиплексор AXI-интерфейса в системную память
Мультиплексор AXI-интерфейса в видео память для блиттеров


PowerVR
Control and Register Bus
SoC Interface
Firmware Processor
SoC Bus
Vertex Data Master
Pixel Data Master
Compute Data Master
Programmable Data Sequencer
Unified Shading Cluster Array
USC
Texture Processing Unit
ASTC
LDR + HDR
PVRTC
USC
Geometry Phase Pipeline
Fragment Phase Pipeline
System Memory Bus
Mixed Cache Unit (MCU)
PVRIC2
2D Texture Load Accelerator
MMU and System Level Cache
System Memory Bus


Toplevel (axig2dec)
AXI Master IF (axiwmiff)
AXI Slave IF (axiwsifd)
Arbiter (busifd)
Clock Gating (clkgate)
Decoder top-level (hwg2core)
SRAM wrapper (hwg2rams)
Memory-mapped registers (hwg2swr)
Video Pipeline Controller (VPC)
FIFOs
Post-Processor (PP)
FIFOs
SAO filter (SAO)
FIFOs
In-loop Deblocking filter (filter)
FIFOs
Intra / Inter Prediction (pred)
FIFOs
Inverse Quantization & Tranform (IQT)
FIFOs
Motion Vector Decode (MVD)
FIFOs
Motion Comp. Prefetch (prefetch)
FIFOs
FIFOs
Entropy decoder (EMD)
FIFOs
HLS generated RTL
Hand-written RTL


BigE Broadcaster Control Software
Application Programming Interface
Two-Pass Control
Rate Control
Multi-core Control
Effort Control
Hardware Drivers
External memory
256 / 128 bit AXI bus
Master Interface
Slave Interface
Memory-Mapped Registers
Reference Frame Decompression
Pre-processing
VP9 Bitstream Generation
Reference Frame Compression
Motion Estimation
RDO Engine
Reconstruction
Broadcaster Hardware Core


Embedded CPU
Host Processor/
DMA Interface
(Global access)
32
Crossbar
Entropy decode
Pixel processing
H.264, VC1, VP8...
Entropy decode
Iscan
Iquant
Ixform
HEVC
Iscan
Iquant
Ixform
Motion
compensation
Cache
Deblocking
buffers
HEVC
Deblocking
SAO
H.264,
VC1, VP8
Deblocking
Scaler
rotator
Memory manager
256
Memory Interface


Host System
Interface
Quartz
Core
Embedded
Processor
DMAC
System Bus
Arbiter
Multi-Pipe
Register Bank
Host
Memory
Interface
Memory
Manage-
ment
Unit
Reference
Cache
CTU
Control
RAM
Register
Bank
Integer
Motion
Estimation
Inter
Stage
Buffer
(IME)
Fractional
Motion
Estimation
Inter
Stage
Buffer
(FME)
Front
End
Inter
Stage
Buffer
(FE)
Encode
Decision
Inter
Stage
Buffer
(Enc)
In-loop
Filter
Extension
Unit
Entropy
Coder
Encoder Pipe
Multi-Pipe Context
Encoder Pipe n
Encoder Pipe n
Optional
Hardware Input
Optional
Hardware Output