Intel® 845 Chipset: 82845 Memory Controller Hub (MCH) for SDR

Specification Update

May 2002

Notice: The Intel® 82845 MCH for SDR may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

Document Number: 298589-004

Contents

Revision History

Rev.	Draft/Changes	Date
-001	Initial Release.	September 2001
-002	• Changed the document name to add the phrase “for SDR”. • Added B0 stepping information.	January 2002
-003	• Removed Errata #1. This erratum does not apply to the production stepping of the 82845 MCH for SDR and was initially entered as an erratum by mistake. • Renumbered the remaining errata to #1 and #2.	February 2002
-004	• Added Documentation Change #1, Changed Section 5.3.6, AGP FRAME# Transactions on AGP.	May 2002

Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents/Related Documents table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this update document and are no longer published in other documents. This document may also contain information that has not been previously published.

Affected Documents/Related Documents

Document Title	Document Number
Intel® 845 Chipset: 82845 Memory Controller Hub (MCH) for SDR Datasheet	290725-002

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Errata may cause the behavior of the Intel 82845 MCH for SDR to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Component Identification via Programming Interface

The Intel 82845 MCH for SDR may be identified by the following register contents:

Stepping	Vendor ID[1]	Device ID[2]	Revision Number[3]
A3	8086h	1A30h	03h
B0	8086h	1A30h	04h

NOTES:
1. The Vendor ID corresponds to bits 15:0 of the Vendor ID Register located at offset 00–01h in the PCI function 0 configuration space.
2. The Device ID corresponds to bits 15:0 of the Device ID Register located at offset 02–03h in the PCI function 0 configuration space.
3. The Revision Number corresponds t bits 7:0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space.

Component Marking Information

The Intel 82845 MCH for SDR may be identified by the following component markings:

Stepping	Q-Spec	S-Spec	Top Marking	Notes
A3	QC27ES	SL5V7	RG82845	
B0	QC71ES	SL5YQ	RG82845	

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes which apply to the listed Intel 82845 MCH steppings. Intel intends to fix some of the errata in a future stepping of the component and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

Codes Used in Summary Table

X:	Erratum, Specification Change or Clarification that applies to this stepping.
Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future stepping of the component.
Fixed:	This erratum has been previously fixed.
NoFix	There are no plans to fix this erratum.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.
Shaded:	This item is either new or modified from the previous version of the document

NO.	SPECIFICATION CHANGES
	There are no specification changes in this Specification Update revision

NO.	A3	B0	PLANS	ERRATA
1			Fixed	SDR PMOS and NMOS Buffer Strengths Are Weaker Than Expected.
2	X		Fixed	Disabling and Enabling AGP without Issuing a Subsequent PCI Reset Causes SBA Synchronization Errors

NO.	SPECIFICATION CLARIFICATIONS
	There are no specification clarifications in this Specification Update revision

NO.	DOCUMENTATION CHANGES
1	Changed Section 5.3.6, AGP FRAME# Transactions on AGP

This page is intentionally left blank.

Specification Changes

There are no specification changes in this Specification Update revision.

This page is intentionally left blank.

Errata

1. SDR PMOS and NMOS Buffer Strengths Are Weaker Than Expected

Problem: During Analog inspection, it was determined that the measured PMOS and NMOS buffer strengths did not coordinate with documented strength settings.

Implication: An appropriate buffer strength offset is required to obtain the desired symmetrical waveforms.

Workaround: The BIOS must program the appropriate buffer offset value.

Status: Fixed in A3 stepping.

2. Disabling and Enabling AGP without Issuing a Subsequent PCI Reset Causes SBA Synchronization Errors

Problem: With AGP SBA active, when disabling and re-enabling AGP (i.e., AGP Command Register, Device 0, Function 0, Offset A8h, bit 8, set to 0 then 1), the FIFO pointers used for sideband transfers on the AGP interface can lose synchronization, resulting in incorrect AGP transactions.

Implication: When INIT (Soft Reset) is used without PCIRST# being asserted, a system where the GC (Graphic Controller) uses SBA transactions can experience system lock-up and video corruption.

Workaround: During warm reset, system BIOS should ensure that a CF9 PCIRST# is issued.

Status: Fixed in B0 stepping.

This page is intentionally left blank.

Specification Clarifications

There are no specification claraifications in this Specification Update revision.

This page is intentionally left blank.

Documentation Changes

1. Changed Section 5.3.6, AGP FRAME# Transactions on AGP

Section 5.3.6, AGP FRAME# Transactions on AGP, is changed as follows. Beneath Note 1 of Table 17, PCI Commands Supported by the Intel® MCH (When Acting as a FRAME# Target), is a series of bullets defining memory transactions when the MCH is a target of an AGP FRAME# cycle. The first bullet is changed to two bullets. The two new bullets read:

- *Memory Read.* Recommended for reads of 32 bytes or less.
- *Memory Read Line, and Memory Read Multiple*. These commands are supported identically by the MCH and allow the MCH to continuously supply data during MRL and MRM burst. Recommended for reads of more than 32 bytes. The MCH does not support reads of the hub interface bus from AGP.