Intel® 845 Chipset Thermal and Mechanical Design Guidelines for SDR

Design Guide

January 2002

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Revision History

Revision Number	Description	Date
-001	Initial Release.	September 2001
-002	Changed the document name to add the term “for SDR”. Minor edits. No technical changes.	January 2002

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1 Introduction

The objective of thermal management is to ensure that the temperature of all components in a system is maintained within functional limits. The functional temperature limit is the range within which the electrical circuits can be expected to meet specified performance requirements. Operation outside the functional limit can degrade system performance, cause logic errors, or cause component and/or system damage. Temperatures exceeding the maximum operating limits may result in irreversible changes in the operating characteristics of the component. The goal of this document is to provide an understanding of the operating limits of the Intel® 845 chipset for use with Single Data Rate (SDR) memory devices and discuss a generic thermal solution.

1.1 Definition of Terms

Term	Definition
BGA	Ball Grid Array. A package type defined by a resin-fiber substrate where a die is mounted, bonded and encapsulated in molding compound. The primary electrical interface is an array of solder balls attached to the substrate opposite the die and molding compound.
CFD	Computational Fluid Dynamics.
FC-BGA	Flip Chip Ball Grid Array. A package type defined by a plastic substrate where a die is mounted using an underfill C4 (Controlled Collapse Chip Connection) attach style. The primary electrical interface is an array of solder balls attached to the substrate opposite the die. Note that the device arrives at the customer with solder balls attached (see Figure 13)
ICH2	I/O Controller Hub. The chipset component that contains the primary PCI interface, LPC interface, USB, ATA-33, and other legacy functions.
EBGA	Mini Ball Grid Array. A smaller version of the BGA with a ball pitch of 1.00 mm.
MCH	Memory Controller Hub. The chipset component that contains the processor and memory interface.
OLGA	Organic Land Grid Array.
T_{die} , T_{case}	The maximum die temperature. This temperature is measured at the geometric center of the top of the package/ die.
TDP	Thermal Design Power. Thermal solutions should be designed to dissipate this target power level. Thermal Design Power (typical) is specified as the highest sustainable power level of most or all of the real applications expected to be run on the given product, based on extrapolations in both hardware and software technology over the life of the component. Thermal solutions should be designed to dissipate this target power level.
TIM	Thermal Interface Material. This material is designed to fill surface voids between the die and heatsink surfaces in order to facilitate heat transfer.
Lfm	Linear Feet per Minute. Units of mass flow for fluids
SDR	Single Data-Rate SDRAM memory.
TRHS	Thermal Resistance of Heatsink.
TOP	Thermal Operating Point. The TOP is defined as the thermal resistance of the thermal interface material loaded at the design force of the clip and retention mechanism plus the thermal resistance of the heatsink at the specified airflow speed.

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2 Product Specifications

2.1 Package Description

2.1.1 Intel® 82845 MCH Package Dimensions

The MCH is packaged in a 37.5 mm x 37.5 mm, 594 FC-BGA (see Figure 1 and Figure 2).

Figure 1. Intel® 82845 MCH Package (Top and Side View)

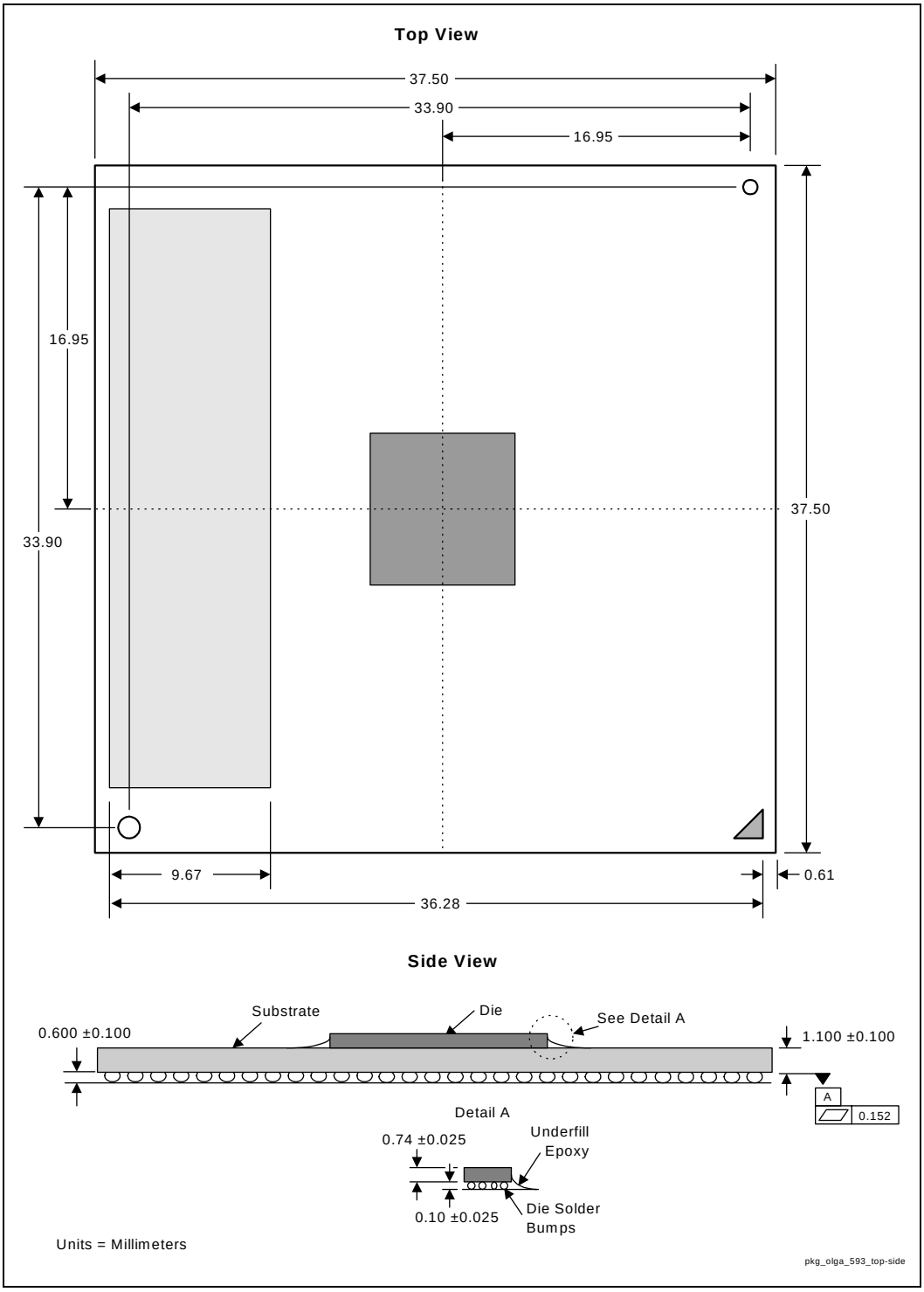
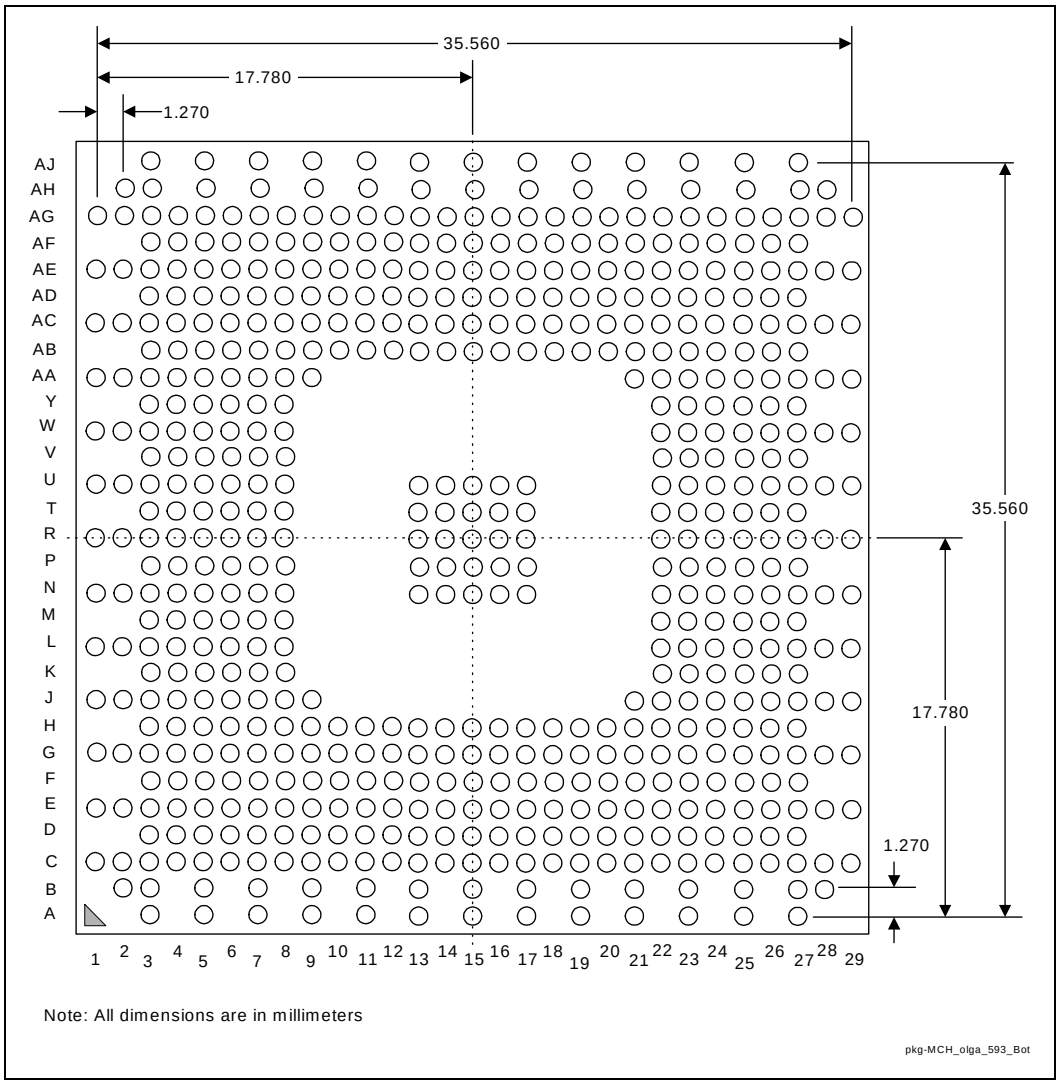


Figure 2. Intel® 82845 MCH Package (Bottom View)



2.1.2 Intel® 82801BA ICH2 Package Dimensions

The ICH2 is packaged in a 23 mm, 4-layer EBGA (see Figure 3 and Figure 4).

Figure 3. Intel® 82801BA ICH2 Package (Top and Side View)

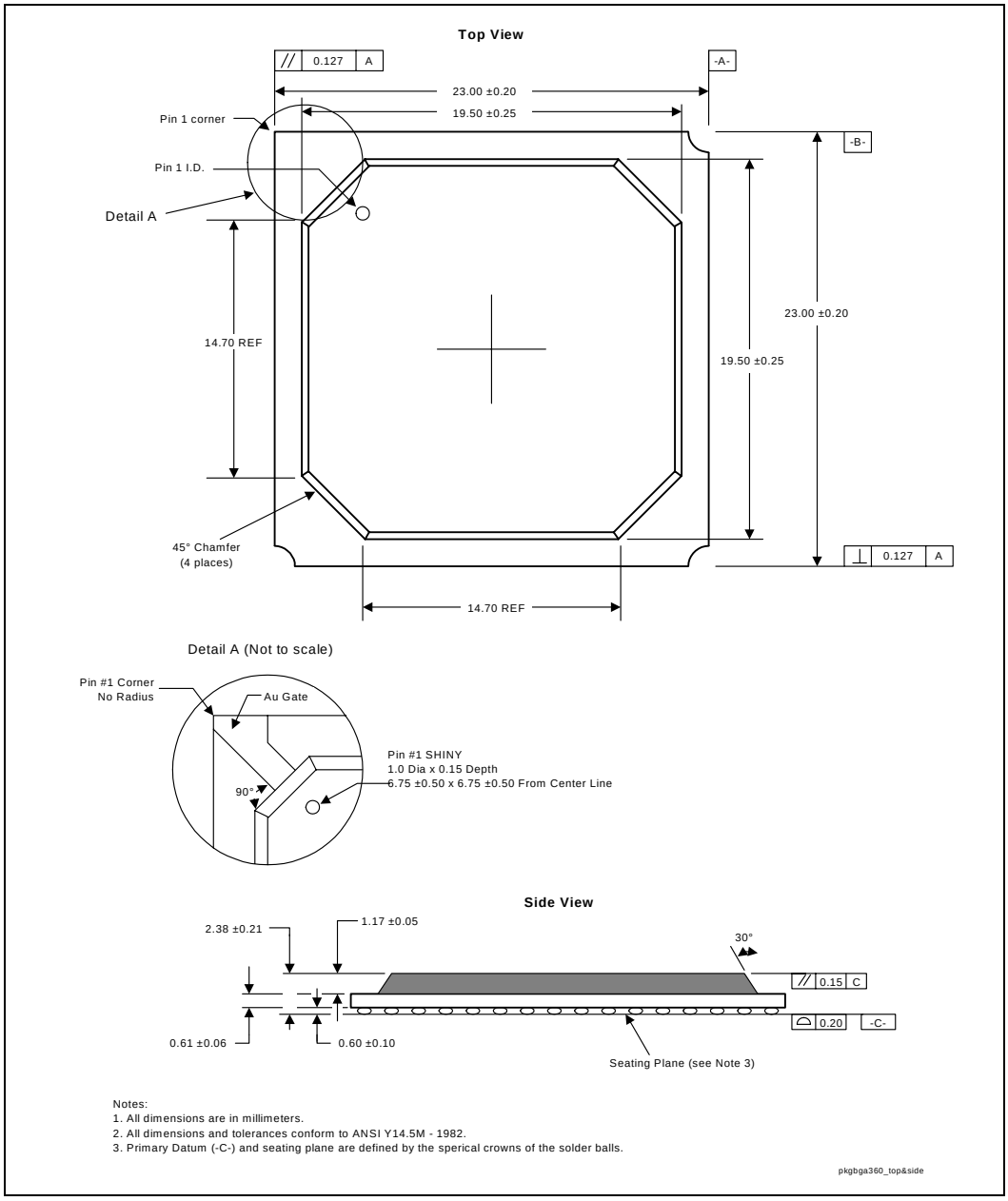
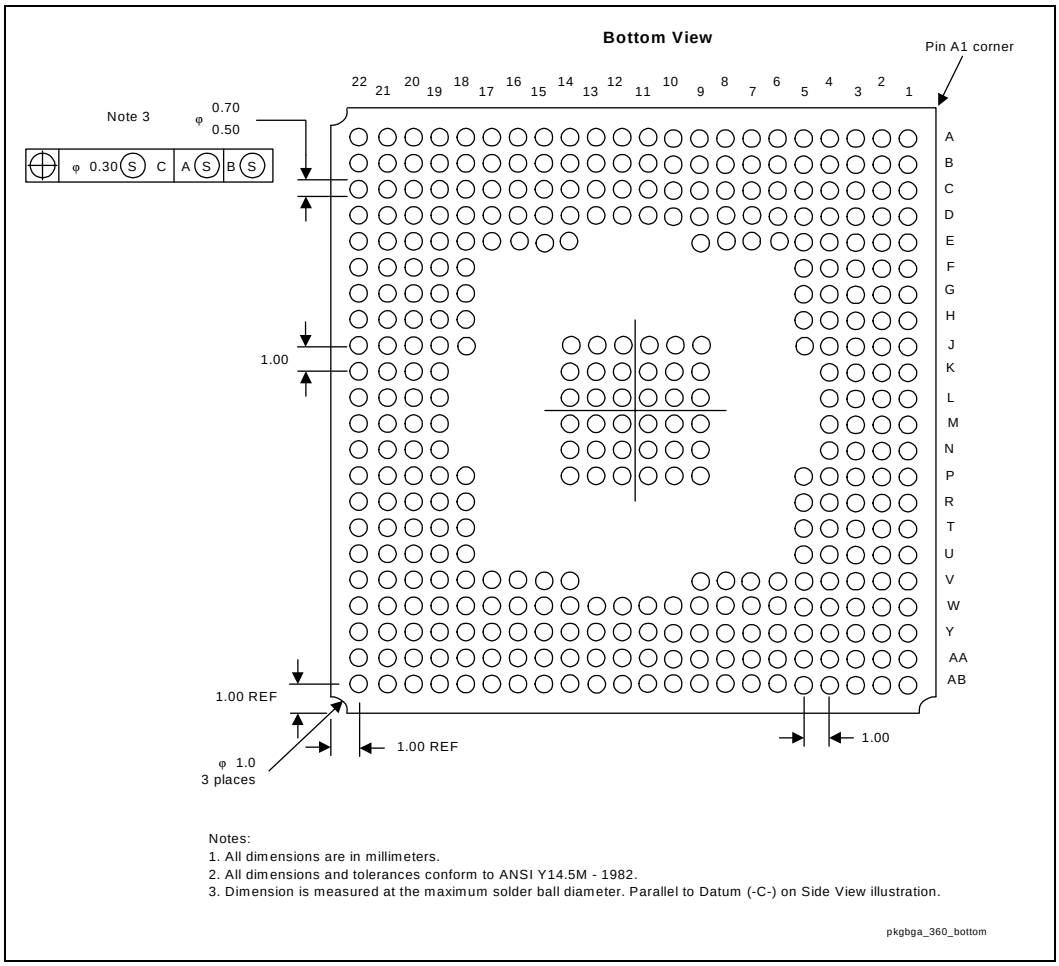


Figure 4. Intel® 82801BA ICH2 Package (Bottom View)



2.2 Heatsink and Clip Mechanical Reference Design

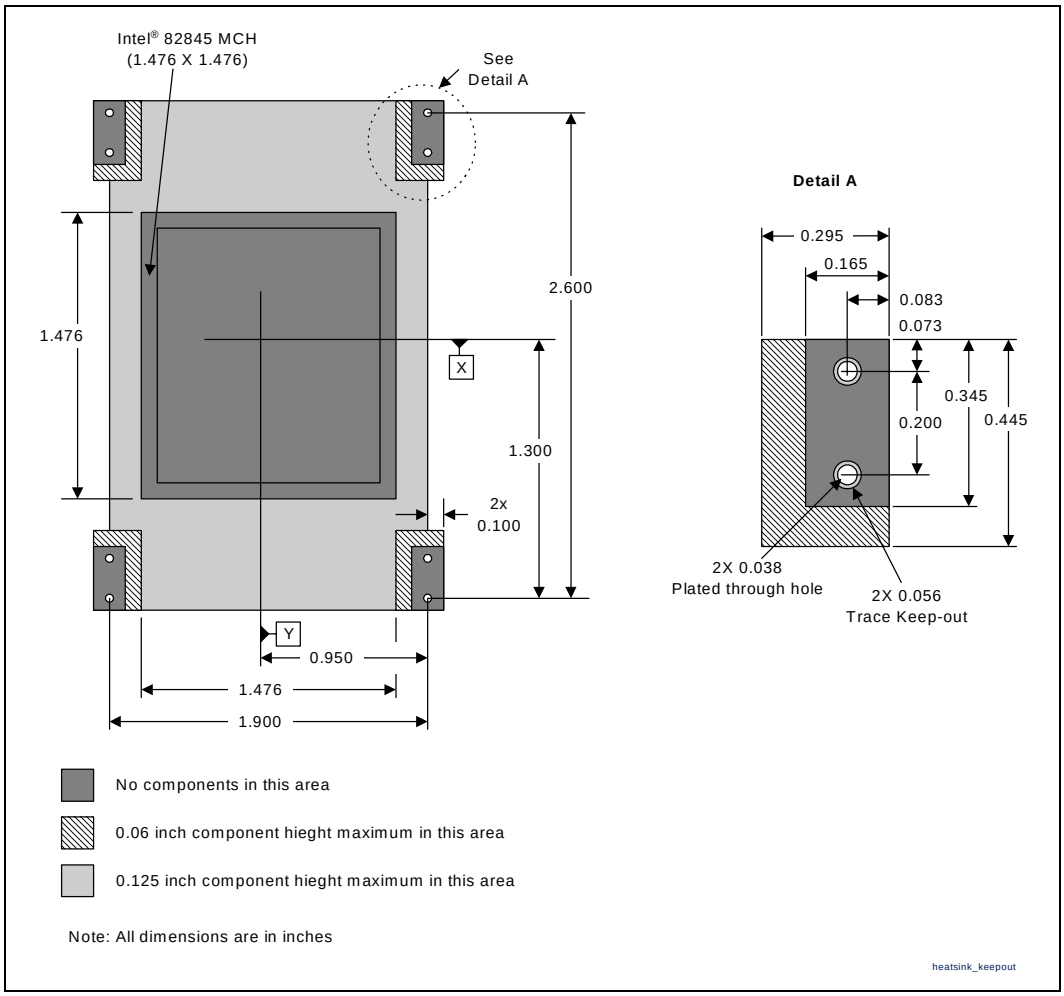
The reference heatsink solution is a passive extruded aluminum heatsink with thermal and mechanical interfaces. It is attached using a clip frame and mechanical advantage lever. The clip frame is secured to the system board via four solder down anchors in four locations around the MCH.

The heatsink clip for the MCH is designed to be used in conjunction with the mechanical attach solution for the Intel® Pentium® 4 processor. The clip provides a mechanical preload applied to the heatsink and package via a mechanical advantage lever. This preload assures minimal bond line thickness and adds rigidity to the heatsink and package assembly. The clip is designed to prevent component damage and potential failures under environmental system loading.

2.2.1 Mechanical Keep-Outs

Figure 5 illustrates the system board keep-out region. The component height restrictions under the clip retention mechanism are also noted.

Figure 5. Heatsink Keep-Out and Solder Down Anchor Location



2.2.2 Heatsink Assembly

The heatsink assembly includes the heatsink (with TIM and mechanical interface gasket), the clip, and clip lever as shown in Figure 6. This clip attaches to solder down anchors located on the system board.

Figure 6. Heatsink Assembly: Heatsink, Clip Frame, Clip Lever

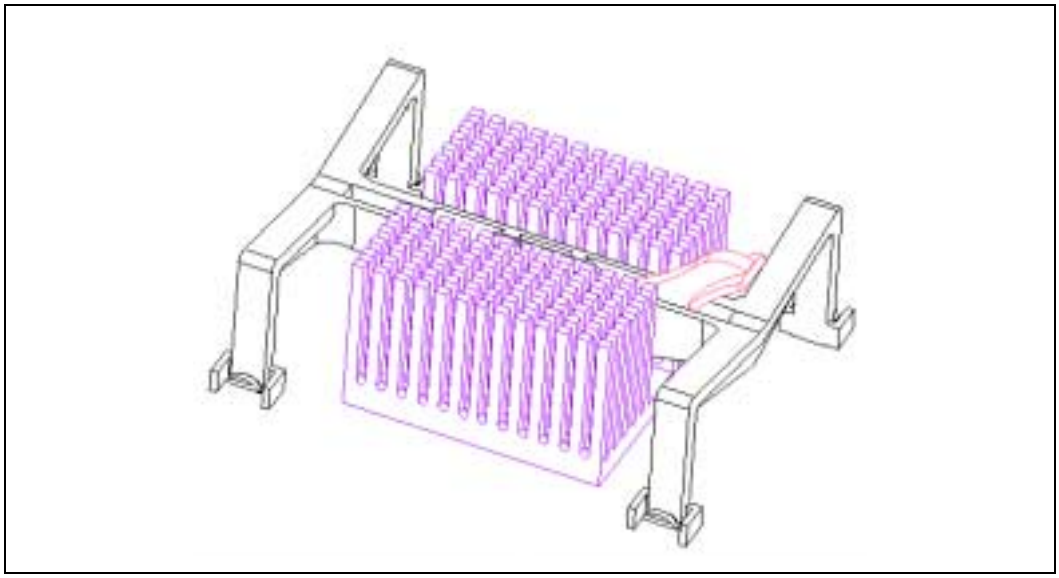
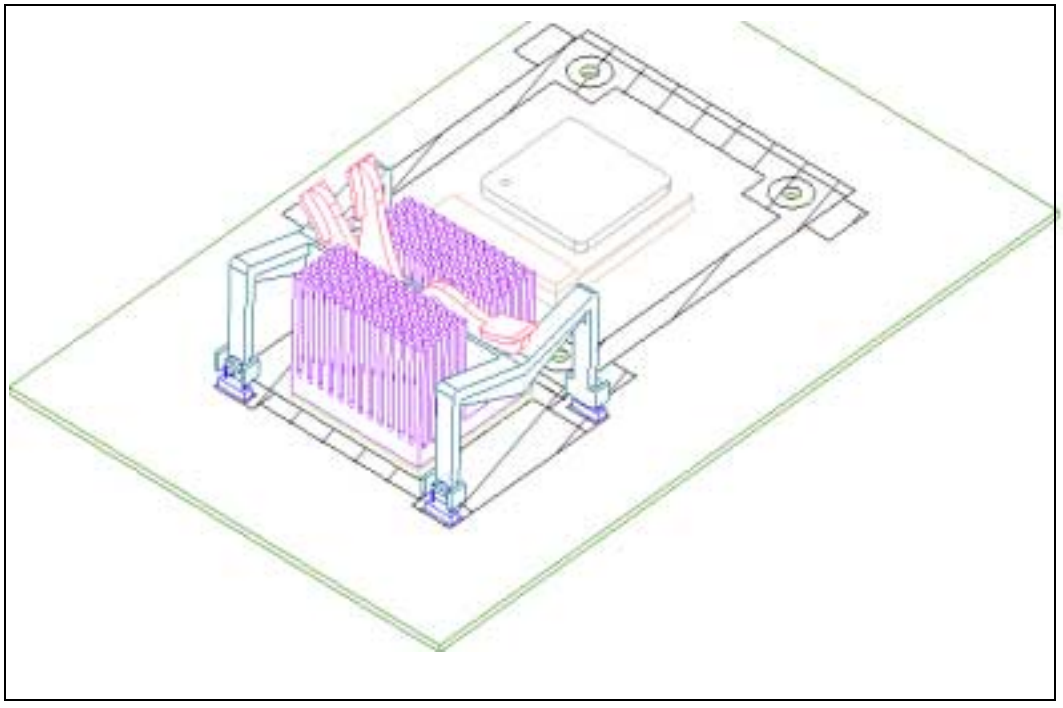


Figure 7. Heatsink Assembly Placement and Actuation



2.3 Thermal and Mechanical Reliability

Recommendations for thermal mechanical reliability testing are shown in Table 1. These should be considered as general guidelines. Validation testing requirements should be defined by the user based on anticipated use conditions.

Table 1. Reliability Validation

Test[1]	Requirement	Pass/Fail Criteria[2]
Mechanical Shock	• Quantity: 3 drops for + and - directions in each of 3 perpendicular axes (i.e., total 18 drops). • Profile: 50 G trapezoidal waveform, 11 ms duration, 170 inches/sec minimum velocity change. • Setup: Mount sample board on test fixture.	Visual\Electrical Check
Random Vibration	• Duration: 10 min/axis, 3 axes • Frequency Range: 5 Hz to 500 Hz • Power Spectral Density (PSD) Profile: 3.13 g RMS	Visual/Electrical Check
Thermal Cycling	• -5 °C to +70 °C, 500 cycles	Visual Check
Unbiased Humidity	• 85 % relative humidity / 55 °C, 1000 hours	Visual Check
Power Cycling	• 7,500 on/off cycles with each cycle specified as 3 minutes on, 2 minutes off 70 °C	Visual Check

NOTES:
1. The above tests should be performed on a sample size of at least 12 assemblies from 3 different lots of material.
2. Additional Pass/Fail Criteria may be added at the discretion of the user.

2.4 Thermal Specifications

2.4.1 External Ambient Conditions

To ensure proper operation and reliability of the MCH, an airflow speed of 50 lfm (linear feet per minute) must be present 1 inch in front of the heatsink air inlet side of the Intel 845 chipset generic thermal solution that is attached to the MCH. Furthermore, the maximum allowable operating air temperature at the MCH heatsink must not exceed 55 °C. The thermal designer must carefully select the location to measure airflow to get a representative sampling. (Note, These environmental specifications are based on a 35°C system external temperature measured at 5000′)

2.4.2 Intel® 845 Chipset Maximum Die Temperatures

To ensure proper operation and reliability of the Intel 845 chipset components, the temperature must be at or below the values specified in Table 2 and Table 3. If the temperature of the component exceeds the maximum temperatures listed, system or component level thermal enhancements are required to dissipate the heat generated. Section 2.5 provides the temperature measurement metrology for die temperature measurements.

Table 2. Intel® MCH Tdie Maximum

Parameter	Maximum MCH Die Temperature
Tdie	92 °C

Table 3. Intel® ICH2 Tcase Maximum

Parameter	Maximum ICH2 Case Temperature
Tcase	109 °C

2.5 Temperature Measurement Metrology

To accurately assess junction temperature for an application or to determine if you are not exceeding a Tdie of 83.6 °C, it is necessary to have a good thermocouple attach. Intel has established guidelines for the proper techniques to be used when measuring the MCH die temperature. Section 2.6 contains information on running an application program that emulates anticipated maximum TDP. The flowchart in Figure 11 offers useful guidelines for thermal performance and evaluation.

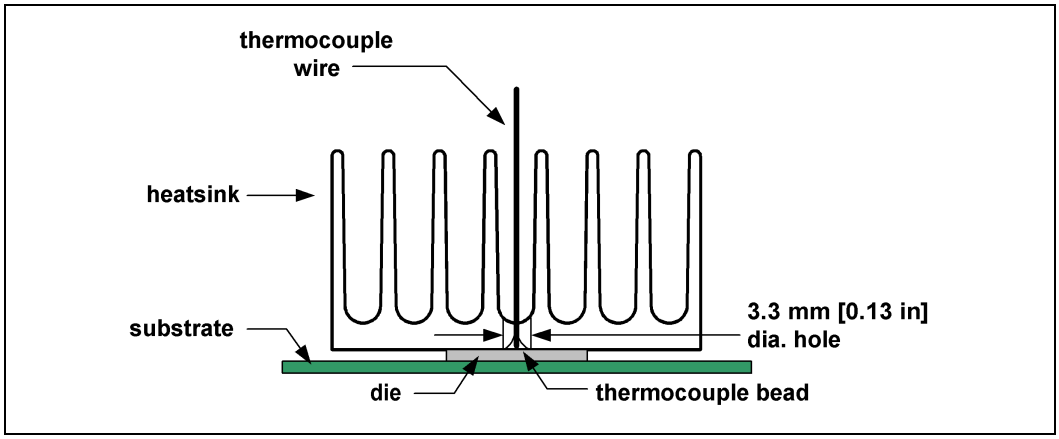
2.5.1 Die Temperature Measurements

To ensure functionality and reliability, the Intel 845 chipset is specified for proper operation when Tdie is maintained at or below its respective temperatures at 50 lfm for the MCH (see Table 2) and ICH2 (see Table 3). The surface temperature at the geometric center of the die corresponds to Tdie.

2.5.2 90 Degree Angle Attach Methodology

1. Use 36 gauge or smaller K-type thermocouples.
2. Ensure that the thermocouples have been properly calibrated.
3. Attach the thermocouple bead or junction to the top surface of the die in the center using high thermal conductivity cement. **It is critical that the thermocouple bead makes contact with the die.**
4. The thermocouple should be attached at a 90 degree angle if there is no interference with the thermocouple attach location or leads (see Figure 8). This is the preferred method and is recommended or use with both bare packages as well as packages employing a thermal solution.
5. The hole size through the heatsink base to route the thermocouple wires out should be smaller than 3.3 mm (0.13 inches) in diameter.
6. Make sure there is no contact between the thermocouple cement and the heatsink base. This contact will affect the thermocouple reading.

Figure 8. 90 Degree Angle Attach Methodology (not to scale)



2.5.3 0 Degree Angle Attach Methodology

1. Mill a 3.3 mm (0.13 inches) diameter hole centered on bottom of the heatsink base (see Figure 9). The milled hole should be approximately 1.5 mm (0.06 inches) deep.
2. Mill a 1.3 mm (0.05 inches) wide slot, 0.5 mm (0.02 inches) deep, from the centered hole to one edge of the heatsink. The slot should be in the direction parallel to the heatsink fins (see Figure 9 and Figure 10).
3. Attach thermal interface material (TIM) to the bottom of the heatsink base.
4. Cut out portions of the TIM to make room for the thermocouple wire and bead. The cutouts should match the slot and hole milled into the heatsink base.
5. Attach a 36 gauge or smaller calibrated K-type thermocouple bead or junction to the center of the top surface of the die using a high thermal conductivity cement. During this step, make sure there is no contact between the thermocouple cement and the heatsink base because any contact will affect the thermocouple reading. **It is critical that the thermocouple bead makes contact with the die** (see Figure 9).
6. Attach heatsink assembly to the MCH and route the thermcouple wires out through the milled slot.

Figure 9. 0 Degree Angle Attach Heatsink Modifications (not to scale)

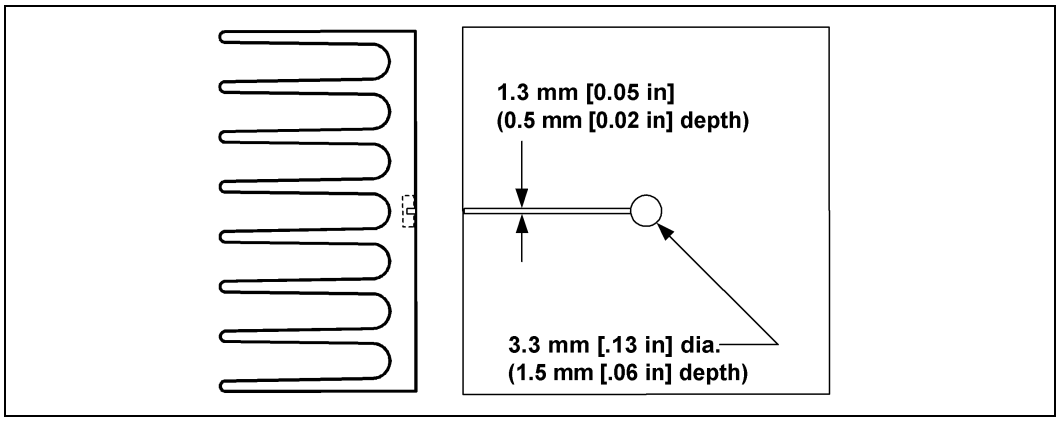
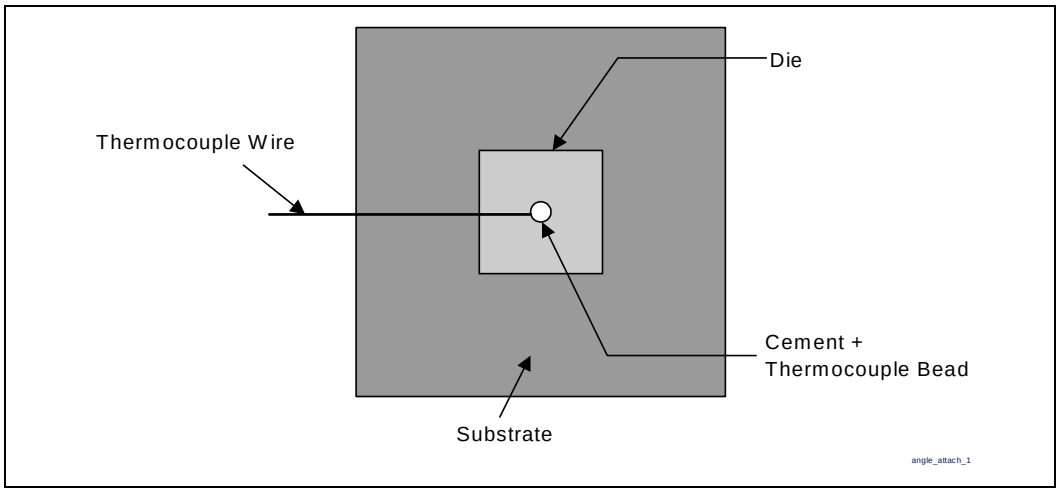


Figure 10. 0 Degree Angle Attach Methodology (not to scale)

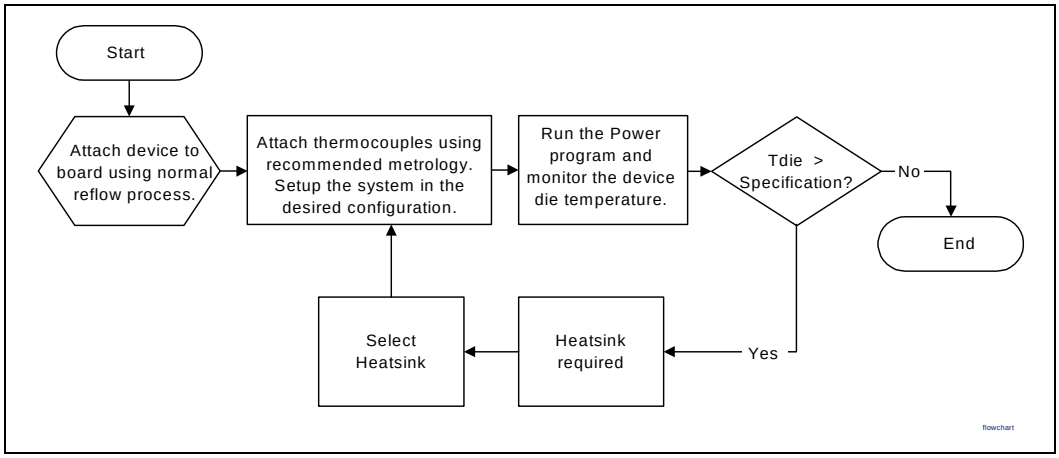


2.6 Power Dissipation Software

The power simulation software is a utility designed to dissipate the Thermal Design Power (TDP) on the MCH when used in conjunction with an Intel Pentium 4 processor. The combination of the Intel Pentium 4 processor and the bandwidth capability of the MCH enable new levels of system performance. To assess the thermal performance of the Intel 845 chipset generic thermal solution during "worst-case realistic application" conditions, Intel has developed a software utility that operates the chipset at near worst-case power dissipation.

The utility has been developed solely for testing customer thermal solutions at or near the thermal design power. Figure 11 shows a decision flowchart for determining thermal solution needs. Real future applications may exceed the thermal design power limit for transient time periods. For power supply current requirements under these transient conditions, refer to each component's datasheet for the I_{CC} (Max Power Supply Current) specification. Contact your Intel Field Sales representative to obtain a copy of this software.

Figure 11. 0 Degree Thermal Solution Decision Flowchart for 0 °C



2.7 Intel® MCH Thermal Design Power (SDRAM)

The Intel 845 chipset for SDR power utility is designed to dissipate the TDPtyp power value through the MCH when a system is populated with the memory listed in Table 4.

Table 4. Intel® MCH Thermal Design Power (SDR)

TDPtyp (Watts)	System Configuration
4.9 W	400 MHz FSB, 133 MHz SDR (6 Rows)

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3 Chipset Generic Thermal Solution

3.1 Generic Thermal Solution Performance

If the thermal designer is able to provide greater than 50 lfm at the air inlet side (upstream) of the heatsink, the Tdie and the junction temperatures of the MCH will decrease. Since the thermal resistance of the package and thermal interface material (TIM) remain constant for all upstream airflow speeds, this behavior is due to the decreased thermal resistance (°C/W) of the Intel 845 chipset generic thermal solution's heatsink. Hence, if a thermal designer can provide greater than 50 lfm upstream of the heatsink, the junction temperature will be reduced. This reduction in junction temperature leads to greater component reliability.

3.2 Generic Thermal Solution TIM Description

A thermal interface material is used to provide improved conductivity between the die and heatsink. The reference thermal solution uses Chomerics* T-710, 0.127 mm (0.005 inches) thick, 12.7 mm x 12.7 mm (0.5 inches x 0.5 inches).

3.2.1 The Effect of Pressure on TIM Performance

As mechanical pressure increases on the TIM, the thermal resistance of the TIM decreases. This phenomenon is due to the decrease of the Bond Line Thickness (BLT). The effect of pressure on the thermal resistance of the Chomerics T710 TIM is shown in Table 5. The heatsink clip (see Figure 6) provides enough pressure for the TIM to achieve a thermal conductivity of 0.9 W/m·K.

Table 5. Chomerics T710 TIM Performance (at 50 °C as a Function of Attach Pressure)

Pressure (psi)	Thermal Resistance ($°C*In^2$)/W
5	0.37
10	0.3
20	0.21
50	0.17

3.3 Generic Thermal Solution Thermal Operating Point

The Thermal Operating Point (TOP) is defined as the thermal resistance of the TIM at the design force of the clip and retention mechanism plus the thermal resistance of the heatsink at the specified airflow speed. The thermal resistance of the heatsink (TRHS) is given by the following equation:

$$TRHS = (T_{die} - T_{local\_ambient}) / (\%\ TDP\ dissipated\ via\ heatsink)$$

Thermal simulation results show that as airflow increases upstream of the Intel 845 chipset generic thermal solution, the percentage of TDP that leaves via the top of the package increases (see Table 6).

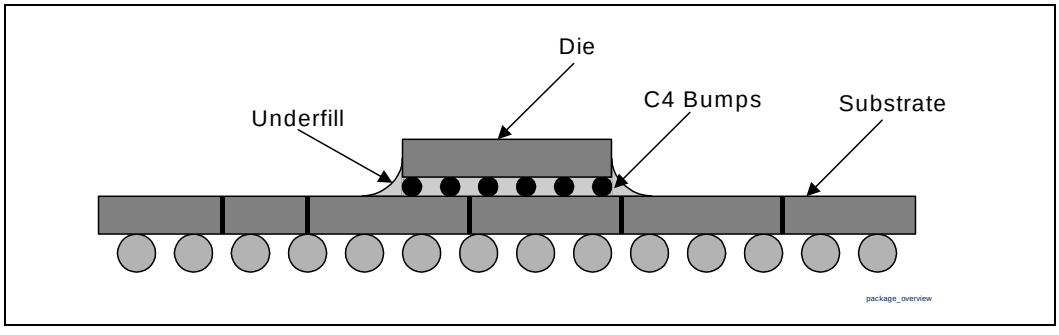
Table 6. TDP Dissipation for Various Airflow Speeds

Upstream Airflow Speed (lfm)	% of TDP Dissipated via Intel Thermal Solution	% of TDP Dissipated via the 4-Layer JEDEC Board
50	70%	30%
100	75%	25%
150	77%	23%

3.4 Generic Thermal Solution Simulation

A Computational Fluid Dynamics (CFD) model of the MCH has been developed for use with the commercially available thermal analysis tool “Flotherm” (version 2.1 or later). This model can be used to evaluate package thermal limits and cooling methods. Modeled MCH components are shown in Figure 12.

Figure 12. Intel® MCH Components Modeled



Contact your Intel Field Sales representative to order the thermal models and user’s guides.

3.4.1 Flotherm Model Implementation in a System Level Analysis

When integrating the MCH model into a system level analysis, two important issues must be considered to ensure that the MCH CFD model correctly predicts thermal behavior. These issues are the proper mating of the model with the motherboard and the thermal solution. Proper mating requires the following:

- Ensure that the solder ball cuboid in the chipset model makes direct contact with the motherboard. Good modeling contact must be specified and the contact should be verified by closely zooming in on the interface between the solder ball cuboid and the motherboard.
- Ensure that the die cuboid in the chipset model is properly mated to the thermal solution. Model the thermal interface material by using a cuboid with the appropriate properties to account for the thermal resistance in the material and the surface contact. Either a non-collapsed or a collapsed cuboid may be used to model the thermal interface material as long as the specified properties of the cuboid remain the same.

3.4.2 System Model Grid

Make sure that a sufficient number of grid cells are used within and around the area of the package to capture sharp thermal gradients. Note that an increase in the number of grid cells may also add to the computation time of model.

3.4.3 Thermal Model Power Dissipation

Based on the system component configuration, use the TDPtyp power values shown in Table 4.

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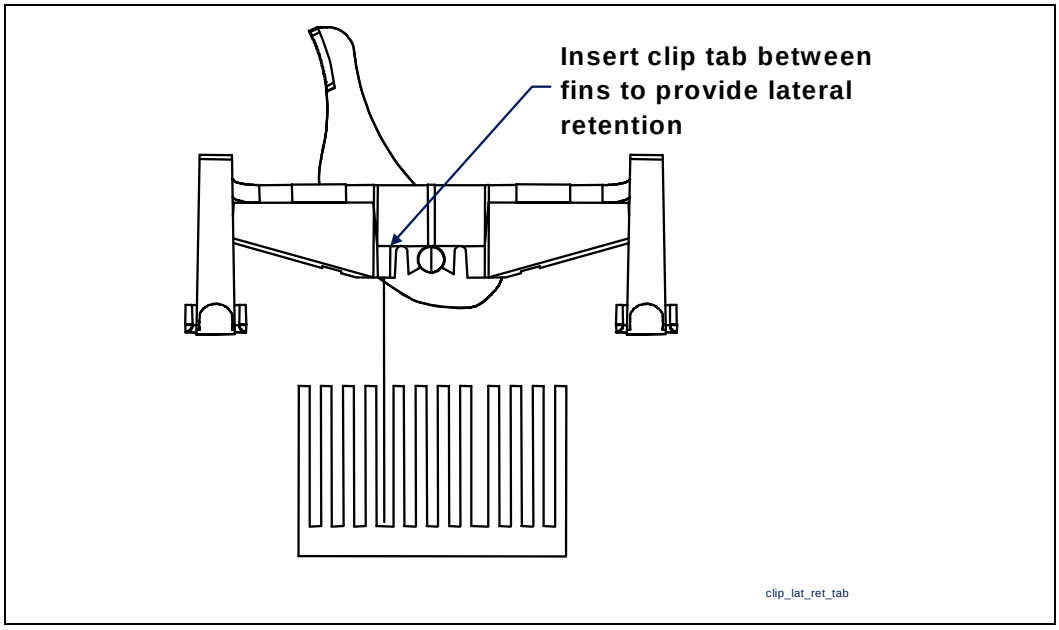
4 Generic Thermal Attach / Mechanical Solution

The heatsink is affixed to the die with a mechanism advantage clip. The clip consists of a clip frame that interfaces to the motherboard through four through-hole mount anchors and an integral lever (see Figure 7). The clip and lever serve three main purposes: to secure the heatsink in intimate contact with the die, to ensure a thermally good bondline between the heatsink and die, and to prevent damage at the package-to-motherboard solder joint during mechanical shock events.

4.1 Heatsink Retention

The heatsink must maintain close contact with the die for the life of the system. The generic clip retention mechanism design holds the heatsink to the die through a single point contact at the center of the heatsink. This ensures that the clip load is centered on the die, thus preventing heatsink tilt that may be caused by unbalanced loading. The clip frame also restrains heatsink lateral motion through tabs located between the heatsink fins (see Figure 13).

Figure 13. Intel® MCH Clip Lateral Retention Tab Feature



4.2 Thermal Bond Line

The thickness of the bond line between the heatsink and die is critical to thermal performance of the TIM. The bond line thickness is dependent on the pressure between the heatsink and the die. The clip retention mechanism is used to generate the pressure required to ensure thermal performance (see Table 5). The generic clip frame and lever design generates more than 50 psi pressure.

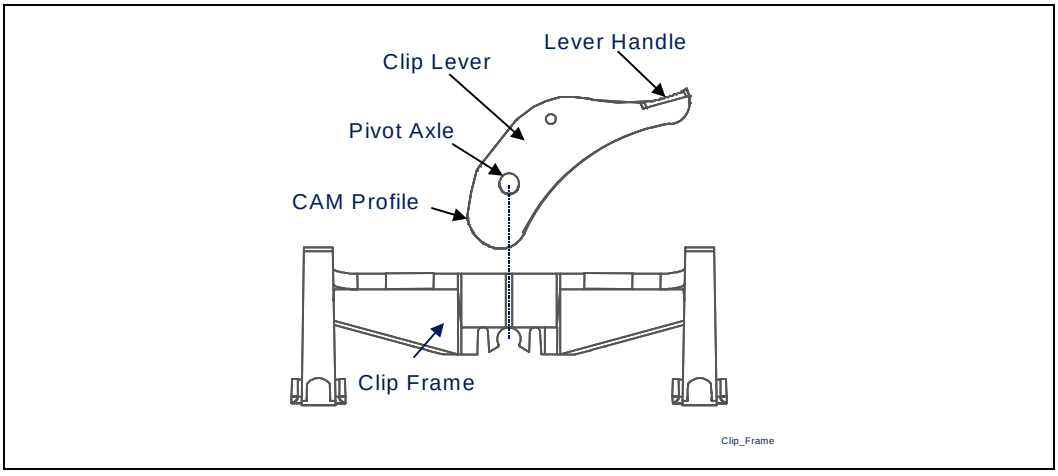
4.3 Solder Joint Protection

The solder joints between the package and the motherboard are susceptible to damage under mechanical shock conditions depending on the mass and proximity of the processor heatsink. Other elements (e.g., motherboard bending rigidity and the size and distribution of other mass components on the motherboard) can also affect solder joint susceptibility to damage.

The generic clip design uses mechanical preload on the package to protect the solder joint against damage under mechanical shock. The design features a rotating cam (see Figure 14) that generates substantial preload between the heatsink and package. The cam has a levered handle that provides a mechanical advantage during installation.

The preload serves to compress the solder ball array between the package and motherboard. The compression in the solder balls delays the onset of tensile load under critical shock conditions, and the magnitude of maximum tensile load is thereby reduced. In this manner, the critical solder balls are protected from tensile loading that may cause damage to the solder joint.

Figure 14. Intel® MCH Clip Frame and Lever



4.4 Intel® MCH Heatsink Drawings

Contact your field representative for additional information.

5 Conclusion

As the complexity of computer systems increases, so do power dissipation requirements. Care must be taken to ensure that the additional power is properly dissipated. Heat can be dissipated using improved system cooling, selective use of ducting, and/or passive heatsinks.

The simplest and most cost-effective method is to improve the inherent system cooling characteristics of the MCH is through careful design and placement of fans, vents, and ducts. When additional cooling is required, component thermal solutions may be implemented in conjunction with system thermal solutions. The size of the fan or heatsink can be varied to balance size and space constraints with acoustic noise.

This document has presented the conditions and requirements to properly design a cooling solution for systems that implement the Intel 845 chipset for SDR. Properly designed solutions provide adequate cooling to maintain the Intel 845 chipset for SDR die temperatures at or below thermal specifications. This is accomplished by providing a low local-ambient temperature, ensuring adequate local airflow, and minimizing the die to local-ambient thermal resistance. By maintaining the Intel 845 chipset for SDR die temperatures at or below those recommended in this document, a system designer can ensure the proper functionality, performance, and reliability of these chipsets.

Table 7. Specification Summary

Package Dimensions	
MCH	37.5 mm x 37.5 mm x 2.54 mm
Handling Keep out on Substrate	
MCH	2 mm from edge of die
Max Allowable Die Pressure	
MCH	400 kPa (this corresponds to 50 lbf load on die)
Heatsink Volume Keep outs	
MCH Heatsink	X:37.5 mm, Y:37.5 mm, Z:40 mm
Operating Environment	
Maximum Temperature Minimum Airflow	55 °C 50 lfm
Thermal Design Power (TDPtyp)	
MCH	4.9 W
Intel® ICH2 Maximum Case Temperature	
ICH2	109 °C
Intel® MCH Maximum Die Temperature	
MCH	92 °C

6 Vendors

6.1 Heatsink BOM Suppliers

Topic	Part	Intel Part Number	Supplier	Supplier Part Number
Extruded Heatsinks	Intel 82845 MCH Pin Fin	A54515-001	Foxconn	
Interface Materials	Intel 82845 MCH TIM (T-710)		Chomerics	69-12-22066-T710
	Intel 82845 MCH Mechanical (Poron)	A61203-001	Boyd	
Attach Hardware	Intel 82845 MCH Clip Frame	A65066-001	Foxconn	
	Intel 82845 MCH Clip Lever	A67031-001	Foxconn	
	Solder-Down Anchor	A13494-005	Foxconn	HB96030-DW
Enabling Assembly	Intel 82845 MCH Enabling Assembly Includes: Heatsink, thermal interface material, mechanical interface material, Clip frame, and Clip lever	A67625-001	Foxconn	PHC029C02012

Some suppliers may be able to provide pre-assembled kits. Contact individual suppliers for information.

Supplier Contact Information

Boyd Corporation	http://www.boydcorp.com
Chomerics, Inc.	http://www.chomerics.com
Foxconn Electronics, Inc.	http://www.foxconn.com