Intel® 810E Chipset Platform

For Use with Universal Socket 370

Design Guide

January 2003

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Revision History

Revision	Version	Description	Date
-001	1.0	Initial Release.	September 2001
-002	1.0	Corrected mis-labeled CPU pins AA33, AA35 in Table 10, Processor Pin Definitions	December 2002
-003	1.0	Corrected mis-labeled CPU pins W3 and W6 AA35 in Table 10, Processor Pin Definitions	January 2003

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1 Introduction

This design guide organizes Intel's design recommendations for the Intel® 810E chipset for use with the universal socket 370 platform. Motherboard design recommendations such as layout and routing guidelines are covered. In addition, this document also addresses system design issues (e.g., thermal requirements for the 810E chipset universal platform).

This design guide contains design recommendations, debug recommendations, and a system checklist. These design guidelines are developed to ensure maximum flexibility for board designers while reducing the risk of board-related issues.

Consult the debug recommendations when debugging a platform based on the 810E chipset for use with universal socket 370. However, these debug recommendations should be understood before completing board design, to ensure that the debug port, in addition to other debug features, are implemented correctly.

The 810E chipset for use with universal socket 370 platform supports the following processors:

- Intel® Pentium® III processor based on 0.18 micron technology (CPUID = 068xh).
- Intel® Celeron® processor based on 0.18 micron technology (CPUID = 068xh). This applies to the Celeron 533A MHz and ≥566 MHz processors
- Future 0.13 micron socket 370 processors

Note: The system bus speed supported by the design is based on the capabilities of the processor, chipset, and clock driver.

Note: The 810E chipset for use with the universal socket 370 is **not** compatible with the Intel® Pentium® II processor (CPUID = 066xh) 370-pin socket.

There are five chipsets in the 810E chipset family:

1. Intel® 810 Chipset. Components are 82810 GMCH and the 82801AA ICH.
2. Intel® 810E Chipset. Components are 82810E GMCH and the 82801AA ICH.
3. Intel® 810E2 Chipset. Components are 82810E GMCH and the 82801BA ICH2.
4. Intel® 810E2 Chipset for use with Universal Socket 370. Components are 82810E GMCH for use with the Universal Socket 370 and the 82801BA ICH2.
5. Intel® 810E Chipset for use with Universal Socket 370. Components are 82810E GMCH for use with the Universal Socket 370 and the 82801AA ICH.

Each of these five chipsets has a separate design guide. This design guide is #5 above. It is intended to allow the use of existing 82810E A0 stepping devices with future 0.13 micron socket 370 processors.

1.1 Terminology

Term	Definition
Aggressor	A network that transmits a coupled signal to another network is called the aggressor network.
AGP	Accelerated Graphics Port
AGTL/AGTL+	Refers to processor bus signals that are implemented using either Assisted Gunning Transceiver Logic (AGTL+) or its lower voltage variant (AGTL), depending on which processor is being used.
Bus Agent	A component or group of components that, when combined, represent a single load on the AGTL+ bus.
Core power rail	A power rail that is only on during *full-power* operation. These power rails are on when the PSON signal is asserted to the ATX power supply. The core power rails that are distributed *directly* from the ATX power supply are: ±5V, ±12V and +3.3V.
Corner	Describes how a component performs when all parameters that could impact performance are adjusted to have the same impact on performance. Examples of these parameters include variations in manufacturing process, operating temperature, and operating voltage. The results in performance of an electronic component that may change as a result of corners include (but are not limited to): clock to output time, output driver edge rate, output drive current, and input drive current. Discussion of the “slow” corner would mean having a component operating at its slowest, weakest drive strength performance. Similar discussion of the “fast” corner would mean having a component operating at its fastest, strongest drive strength performance. Operation or simulation of a component at its slow corner and fast corner is expected to bound the extremes between slowest, weakest performance and fastest, strongest performance.
Crosstalk	The reception on a victim network of a signal imposed by aggressor network(s) through inductive and capacitive coupling between the networks. • Backward Crosstalk–coupling that creates a signal in a victim network that travels in the opposite direction as the aggressor’s signal. • Forward Crosstalk–coupling that creates a signal in a victim network that travels in the same direction as the aggressor’s signal. • Even Mode Crosstalk–coupling from single or multiple aggressors when all the aggressors switch in the same direction that the victim is switching. • Odd Mode Crosstalk–coupling from single or multiple aggressors when all the aggressors switch in the opposite direction that the victim is switching.
Derived power rail	A *derived* power rail is any power rail that is generated from another power rail using an on-board voltage regulator. For example, 3.3VSB is usually derived (on the motherboard) from 5VSB using a voltage regulator.
Dual power rail	A dual power rail is derived from different rails at different times (depending on the power state of the system). Usually, a dual power rail is derived from a *standby supply* during *suspend* operation and derived from a *core supply* during *full-power* operation.

Term	Definition
Flight Time	Flight Time is a term in the timing equation that includes the signal propagation delay, any effects the system has on the T_{CO} of the driver, plus any adjustments to the signal at the receiver needed to guarantee the setup time of the receiver. More precisely, *flight time* is defined to be: The time difference between a signal at the input pin of a receiving agent crossing VREF (adjusted to meet the receiver manufacturer's conditions required for AC timing specifications; i.e., ringback, etc.), and the output pin of the driving agent crossing VREF if the driver was driving the Test Load used to specify the driver's AC timings. The VREF Guardband takes into account sources of noise that may affect the way an AGTL+ signal becomes valid at the receiver. See the definition of the VREF Guardband. • **Maximum and Minimum Flight Time** - Flight time variations can be caused by many different parameters. The more obvious causes include variation of the board dielectric constant, changes in load condition, crosstalk, VTT noise, VREF noise, variation in termination resistance and differences in I/O buffer performance as a function of temperature, voltage and manufacturing process. Some less obvious causes include effects of *Simultaneous Switching Output (SSO)* and packaging effects. — The Maximum Flight Time is the largest flight time a network will experience under all variations of conditions. Maximum flight time is measured at the appropriate VREF Guardband boundary. — The Minimum Flight Time is the smallest flight time a network will experience under all variations of conditions. Minimum flight time is measured at the appropriate VREF Guardband boundary. For more information on flight time and the VREF Guardband, see the *Intel® Pentium® II Processor Developer's Manual*.
Full-power operation	During *full-power* operation, all components on the motherboard remain powered. Note that *full-power* operation includes both the *full-on* operating state (S0) and the processor Stop Grant state (S1).
GMCH	Graphics and Memory Controller Hub. A component of the Intel® 810E chipset platform for use with the Universal Socket 370
GTL+	GTL+ is the bus technology used by the Pentium Pro processor. This is an incident wave switching, open-drain bus with pull-up resistors that provide both the high logic level and termination. It is an enhancement to the GTL (Gunning Transceiver Logic) technology. See the *Intel® Pentium® II Processor Developer's Manual* for more details of GTL+.
ICH	82801AA I/O Controller Hub component.
ISI	Inter-symbol interference is the effect of a previous signal (or transition) on the interconnect delay. For example, when a signal is transmitted down a line and the reflections due to the transition have not completely dissipated, the following data transition launched onto the bus is affected. ISI is dependent upon frequency, time delay of the line, and the reflection coefficient at the driver and receiver. ISI can impact both timing and signal integrity.
Network	The trace of a Printed Circuit Board (PCB) that completes an electrical connection between two or more components.
Network Length	The distance between agent 0 pins and the agent pins at the far end of the bus.
Overdrive Region	Is the voltage range, at a receiver, located above and below VREF for signal integrity analysis. See the *Intel® Pentium® II Processor Developer's Manual* for more details.

Term	Definition
Overshoot	Maximum voltage allowed for a signal at the processor core pad. See each processor's datasheet for overshoot specification.
Pad	The electrical contact point of a semiconductor die to the package substrate. A pad is only observable in simulation.
Pin	The contact point of a component package to the traces on a substrate such as the motherboard. Signal quality and timings can be measured at the pin.
Power rails	An ATX power supply has 6 power rails: +5V, -5V, +12V, -12V, +3.3V, +5VSB. In addition to these power rails, several other power rails can be created with voltage regulators.
Ringback	The voltage that a signal rings back to after achieving its maximum absolute value. Ringback may be due to reflections, driver oscillations, or other transmission line phenomena.
Settling Limit	Defines the maximum amount of ringing at the receiving pin that a signal must reach before its next transition. See the respective processor's datasheet for settling limit specification.
Setup Window	The time between the beginning of Setup to Clock (T_{SU_MIN}) and the arrival of a valid clock edge. This window may be different for each type of bus agent in the system.
Simultaneous Switching Output (SSO)	Simultaneous Switching Output (SSO) Effects refers to the difference in electrical timing parameters and degradation in signal quality caused by multiple signal outputs simultaneously switching voltage levels (e.g., high-to-low) in the opposite direction from a single signal (e.g., low-to-high) or in the same direction (e.g., high-to-low). These are respectively called odd-mode switching and even-mode switching. This simultaneous switching of multiple outputs creates higher current swings that may cause additional propagation delay (or "push-out"), or a decrease in propagation delay (or "pull-in"). These SSO effects may impact the setup and/or hold times and are not always taken into account by simulations. System timing budgets should include margin for SSO effects.
Standby power rail	A power rail that in on during *suspend* operation (these rails are also on during *full-power* operation). These rails are on at all times (when the power supply is plugged into AC power). The only standby power rail that is distributed *directly* from the ATX power supply is 5VSB (5V Standby). There can be other standby rails that are created with voltage regulators.
Stub	The branch from the bus trunk terminating at the pad of an agent.
Suspend operation	During suspend operation, power is removed from some components on the motherboard. The customer reference board supports three suspend states: processor Stop Grant (S1), Suspend-to-RAM (S3) and Soft-off (S5).
Suspend-to-RAM (STR	In the STR state, the system state is stored in main memory and all unnecessary system logic is turned off. Only main memory and logic required to *wake* the system remain powered.
System Bus	The system bus is the processor bus.
Test Load	Intel uses a 50 Ω test load for specifying its components.
Trunk	The main connection, excluding interconnect branches, from one end agent pad to the other end agent pad.
Undershoot	Minimum voltage observed for a signal to extend below VSS at the device pad.

Term	Definition
Universal Socket 370	Refers to the Intel 810E chipset using the “universal” PGA370 socket. In general, these designs support 66/100/133 MHz system bus operation, Intel VRM guidelines for future 0.13 micron processors, and Celeron® processors (CPUID=068xh), Pentium® III processor (CPUID=068xh), and future Pentium III processors in single-microprocessor based designs.
Victim	A network that receives a coupled crosstalk signal from another network is called the victim network.
VREF Guardband	A guardband (DVREF) defined above and below VREF to provide a more realistic model accounting for noise such as crosstalk, VTT noise, and VREF noise.

1.2 Related Document

Document and Location	Document Number
Intel® 810E Chipset: 82810E Graphics and Memory Controller Hub (GMCH) Datasheet http://developer.intel.com/design/chipsets/datashts/290676.htm	290676
Intel® 82801BA I/O Controller Hub 2 (ICH2) and Intel® 82801 BAM I/O Controller Hub 2 Mobile (ICH2-M) Datasheet http://developer.intel.com/design/chipsets/datashts/290687.htm	290687
Intel® 82802AB/AC FirmWare Hub (FWH) Datasheet http://developer.intel.com/design/chipsets/datashts/290658.htm	290658
Intel® Celeron® Processor Datasheet http://developer.intel.com/design/celeron/datashts/243658.htm	243658
Intel® Celeron® Processor Specification Update http://developer.intel.com/design/celeron/specupdt/243748.htm	243748
CK 810E Clock Synthesizer Driver Specification, r 0.9	FM-1654
PPGA 370 Power Delivery Guidelines	
Pentium® III Processor for the SC242 at 450 MHz to 1.13 GHz Datasheet http://developer.intel.com/design/pentiumiii/datashts/244452.htm	244452
Intel® Pentium® III Processor Specification Update http://developer.intel.com/design/pentiumiii/specupdt/244453.htm	244453
Intel® Pentium® III Power Distribution Guidelines (AP-907) Application Note http://developer.intel.com/design/pentiumiii/applnots/245085.htm	245085
PCI Local Bus Specification, Revision 2.2	
Universal Serial Bus Specification, Revision 1.0	
Intel® 82562ET Platform LAN Connect (PLC) Datasheet	
PCB Design for the Intel® 82562 ET/EM Platform LAN Connect	
Intel® 82562EH HomePNA 1 Mb/s Physical Layer Interface Datasheet http://www.intel.com/design/network/home/82562EH_datasheet.pdf	278313
Intel® 82562EH HomePNA 1 Mb/s Physical Layer Interface Brief Datasheet http://www.intel.com/design/network/prodbrf/82562eh.htm	278314

1.3 System Overview

The 810E chipset platform for use with the universal socket 370 contains a Graphics and Memory Controller Hub (GMCH) component and I/O Controller Hub (ICH) component for desktop platforms.

The GMCH provides the processor interface optimized for future 0.13 micron 370 socket processors, DRAM interface, hub interface, and internal graphics. This product provides flexibility and scalability in graphics and memory subsystem performance.

The Accelerated Hub Architecture interface (i.e., the chipset component interconnect) is designed into the chipset to provide an efficient, high-bandwidth communication channel between the GMCH and the I/O controller hub. The chipset architecture also enables a security and manageability infrastructure through the firmware hub component.

An ACPI-compliant 810E chipset universal platform can support the *Full-on (S0), Stop Grant (S1), Suspend to RAM (S3), Suspend to Disk (S4),* and *Soft-off (S5)* power management states. The chipset also supports *wake-on-LAN** for remote administration and troubleshooting. The chipset architecture removes the requirement for the ISA expansion bus that was traditionally integrated into the I/O subsystem of PCIsets/AGPsets. This removes many of the conflicts experienced when installing hardware and drivers into legacy ISA systems. The elimination of ISA provides true *plug-and-play* for the platform. Traditionally, the ISA interface was used for audio and modem devices. The addition of AC'97 allows the OEM to use *software-configurable* AC'97 audio and modem coder/decoders (codecs), instead of the traditional ISA devices.

The 810E chipset platform for use with the universal socket 370 contains two core components:

- Intel 82810E Graphics and Memory Controller Hub (GMCH)
- Intel 82801AA I/O Controller Hub (ICH)

The GMCH integrates a 66/100/133 MHz, P6 family system bus controller, integrated 2D/3D graphics accelerator, 100 MHz SDRAM controller and a high-speed hub interface for communication with the I/O Controller Hub (ICH). The ICH integrates an Ultra ATA/66 controller, USB host controller, LPC interface controller, FWH interface controller, PCI interface controller, AC'97 digital controller, and a hub interface for communication with the GMCH. System Features.

1.3.1 Component Features

1.3.1.1 Intel® 82810E GMCH Features

- Processor/System Bus Support
  - Optimized for future Intel Pentium III processors that use 0.13 micron technology at 133 MHz system bus frequency
  - Supports 32-bit AGTL or AGTL+ bus addressing
  - Supports uni-processor systems
  - Utilizes AGTL and AGTL+ bus driver technology (gated AGTL/AGTL+ receivers for reduced power)
- Integrated DRAM controller
  - 32 MB to 512 MB using 16Mb/64Mb/128 Mb technology
  - 100 MHz interface
  - 64-bit data interface
  - Standard Synchronous DRAM (SDRAM) support
  - Supports only 3.3V DIMM DRAM configurations
  - No registered DIMM support
  - Support for asymmetrical DRAM addressing only
  - Support for x8, x16, and X32 DRAM device widths
- Integrated Graphics Controller
  - Full 2D hardware acceleration
  - Texture-mapped 3D with point sampled, bilinear, trilinear, and anisotropic filtering
  - Hardware motion compensation assist for software MPEG/DVD decode
  - Digital Video Out interface for support of digital displays
  - Integrated 230 MHz DAC
- Optional Local Graphics Memory Controller (Display Cache)
  - 32-bit data interface
  - 133 MHz memory clock
  - Support for 1MX16 (4MB ONLY)
- Packaging/Power
  - 421 BGA
  - 1.8V core and 3.3V CMOS I/O

1.3.1.2 Intel® 82801AA I/O Controller Hub (ICH)

The ICH allows the I/O subsystem to access the rest of the system, as follows:

- Upstream accelerated hub architecture interface for access to the GMCH
- PCI 2.2 interface (6 PCI Request/Grant pairs)
- Bus master IDE controller; supports Ultra ATA/66
- USB controller
- I/O APIC
- SMBus controller
- FWH interface
- LPC interface
- AC'97 2.1 interface
- Integrated system management controller
- Alert on LAN*
- IRQ controller
- Packaging/Power
  - 241 Mini BGA
  - 3.3V core and 1.8V and 3.3V Standby

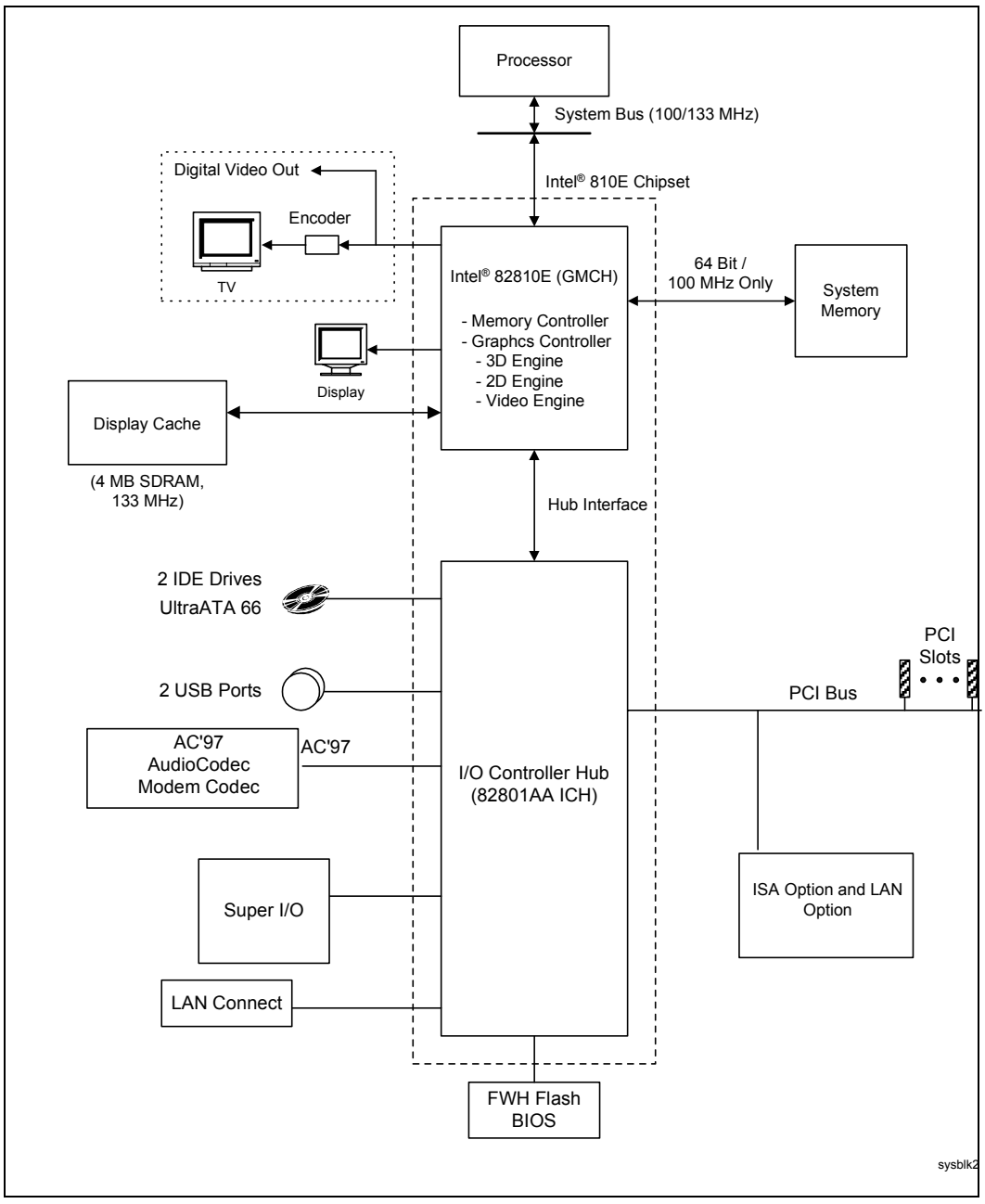
1.3.1.3 Firmware Hub (FWH)

The hardware features of the firmware hub include:

- An integrated hardware Random Number Generator (RNG)
- Register-based locking
- Hardware-based locking
- 5 General Purpose Interrupts (GPI)
- Packaging/Power
  - 40L TSOP and 32L PLCC
  - 3.3V core and 3.3V / 12V for fast programming

1.3.2 System Configurations

Figure 1. Intel® 810E Chipset System



1.4 Platform Initiatives

1.4.1 Universal Socket 370 Design

The 810E chipset platform for use with the Universal Socket 370 allows systems designers to build one system that is compatible with the Pentium III processor (CPUID=068xh), Celeron processor (CPUID=068xh), and future 0.13 micron socket 370 processors. When implemented, the 810E chipset platform for use with the Universal Socket 370 can detect which processor is present in the socket and function accordingly.

1.4.2 Hub Architecture Interface

As I/O speeds increase, the demand placed on the PCI bus by the I/O bridge becomes significant. With the addition of AC'97 and Ultra ATA/66, coupled with the existing USB, I/O requirements could affect PCI bus performance. The chipset platform's *accelerated hub architecture* ensures that the I/O subsystem, both PCI and integrated I/O features (IDE, AC'97, USB), receives adequate bandwidth. By placing the I/O bridge on the accelerated hub architecture interface instead of PCI, I/O functions integrated into the ICH and the PCI peripherals are ensured the bandwidth necessary for peak performance.

1.4.3 Manageability

The 810E chipset platform integrates several functions designed to manage the system and lower the system's total cost of ownership (TCO) of the system. These system management functions are designed to report errors, diagnose the system, and recover from system lock-ups, without the aid of an external micro controller.

1.4.3.1 TCO Timer

The ICH integrates a programmable TCO Timer. This timer is used to detect system locks. The first expiration of the timer generates an SMI# that the system can use to recover from a software lock. The second expiration of the timer causes a system reset to recover from a hardware lock.

1.4.3.2 Processor Present Indicator

The ICH looks for the processor to fetch the first instruction after reset. If the processor does not fetch the first instruction, the ICH will reboot the system.

1.4.3.3 Function Disable

The ICH provides the ability to disable the following functions: AC'97 Modem, AC'97 Audio, IDE, USB, and SMBus. Once disabled, these functions no longer decode I/O, memory or PCI configuration space. Also, no interrupts or power management events are generated by the disabled functions.

1.4.3.4 Intruder Detect

The ICH provides an input signal (INTRUDER#) that can be attached to a switch that is activated when the system case is opened. The ICH can be programmed to generate an SMI# or TCO event as the result of an active INTRUDER# signal.

1.4.3.5 Alert on LAN*

The ICH supports Alert on LAN. In response to a TCO event (intruder detect, thermal event, processor boot failure), the ICH sends a hard-coded message over the SMBus. A LAN controller supporting the Alert on LAN protocol can decode this SMBus message and send a message over the network to alert the network manager.

1.4.4 AC ’97

The *Audio Codec ’97* (AC’97) specification defines a digital interface that can be used to attach an *audio codec* (AC), a *modem codec* (MC), an *audio/modem codec* (AMC) or both an AC and an MC. The AC’97 specification defines the interface between the system logic and the audio or modem codec, known as the *AC’97 Digital Link*.

The chipset platform’s AC’97 (with the appropriate codecs) not only replaces ISA audio and modem functionality, but also improves overall platform integration by incorporating the AC’97 digital link. Using the chipset’s integrated AC’97 digital link reduces cost and eases migration from ISA.

The ICH is an AC’97-compliant controller that supports up to two codecs, with independent PCI functions for audio and modem. The ICH communicates with the codec(s) via a digital serial link called the AC-link. All digital audio/modem streams and command/status information are communicated over the AC-link. Microphone input and left and right audio channels are supported for a high-quality, two-speaker audio solution. Wake-on-ring-from-suspend also is supported with an appropriate modem codec.

By using an audio codec, the AC’97 digital link allows for cost-effective, high-quality, integrated audio. In addition, an AC’97 soft modem can be implemented with the use of a modem codec. Several system options exist when implementing AC’97. The chipset platform’s integrated digital link allows two external codecs to be connected to the ICH. The system designer can provide audio with an audio codec or a modem with a modem codec. For systems requiring both audio and a modem, there are two solutions: the audio codec and the modem codec can be integrated into an AMC, or separate audio and modem codecs can be connected to the ICH.

Modem implementation for different countries must be taken into consideration, as telephone systems may vary. By implementing a split design, the audio codec can be on board and the modem codec can be placed on a riser. Intel is developing an AC ’97 digital link connector. With a single integrated codec, or AMC, both audio and modem can be routed to a connector near the rear panel where the external ports can be located.

1.4.5 Low-Pin-Count (LPC) Interface

In the 810E chipset platform, the Super I/O (SIO) component has migrated to the Low-Pin-Count (LPC) interface. Migration to the LPC interface allows for lower-cost Super I/O designs. The LPC Super I/O component requires the same feature set as traditional Super I/O components. It should include a keyboard and mouse controller, floppy disk controller, and serial and parallel ports. In addition to the Super I/O features, an integrated game port is recommended, because the AC'97 interface does not provide support for a game port. In systems with ISA audio, the game port typically existed on the audio card. The fifteen-pin game port connector provides for two joysticks and a two-wire MPU-401 MIDI interface. Consult your preferred Super I/O vendor for a comprehensive list of the devices offered and the features supported.

In addition, depending on system requirements, specific system I/O requirements may be integrated into the LPC Super I/O. For example, a USB hub may be integrated to connect to the ICH USB output and extend it to multiple USB connectors. Other SIO integration targets include a device bay controller or an ISA-IRQ-to-serial-IRQ converter to support a PCI-to-ISA bridge. Contact your Super I/O vendor to ensure the availability of the desired LPC Super I/O features.

2 General Design Considerations

This design guide documents motherboard layout and routing guidelines for 810E universal socket 370 platform-based systems. This design guide does not discuss the functional aspects of any bus or the layout guidelines for an add-in device.

If the guidelines listed in this document are not followed, it is very important that thorough signal integrity and timing simulations be completed for each design. Even when the guidelines are followed, critical signals should be simulated to ensure the proper signal integrity and flight time. As bus speeds increase, it is imperative that the guidelines documented are followed precisely. Any deviation from these guidelines should be simulated.

The trace impedance typically noted (i.e., 60 Ω ± 15%) is the "nominal" trace impedance for a 5-mil-wide trace. That is, it is the impedance of the trace when not subjected to the fields created by changing current in neighboring traces. When calculating flight times, it is important to consider the minimum and maximum impedance of a trace, based on the switching of neighboring traces. The use of wider spaces between the traces can minimize this trace-to-trace coupling. In addition, these wider spaces reduce crosstalk and settling time.

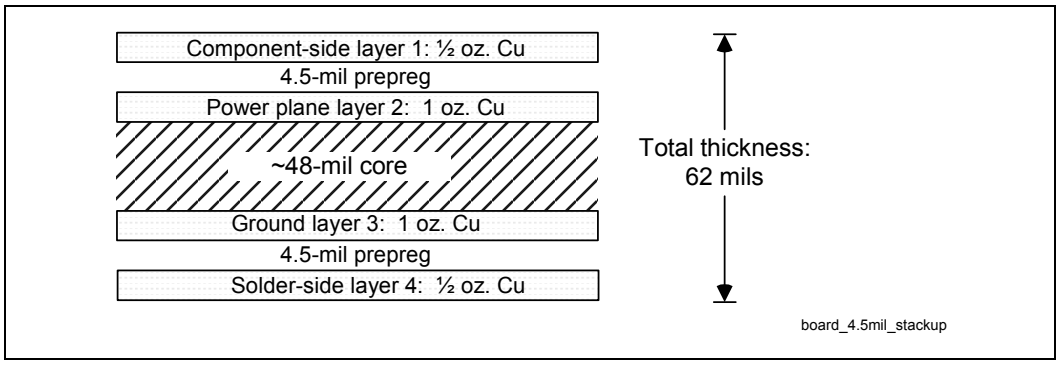
Coupling between two traces is a function of the coupled length, the distance separating the traces, the signal edge rate, and the degree of mutual capacitance and inductance. To minimize the effects of trace-to-trace coupling, follow the routing guidelines documented in this section.

Additionally, these routing guidelines are created using a PCB *stack-up* similar to that illustrated in Figure 2.

2.1 Nominal Board Stack-Up

The 810E chipset universal platform requires a board stack-up yielding a target impedance of 60 Ω ± 10% with a 5 mil nominal trace width. Figure 2 presents an example stack-up that achieves this. It is a 4-layer printed circuit board (PCB) construction using 53%-resin FR4 material.

Figure 2. Board Construction Example for 60 Ω Nominal Stack-up



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3 Component Layouts

Figure 3 illustrates the relative signal quadrant locations on the GMCH ballout. It does not represent the actual ballout. Refer to the *Intel® 810E Chipset: 82810E Graphics and Memory Controller Hub (GMCH)* Datasheet for the actual ballout.

Figure 3. Intel® 82810E GMCH 421-BGA Quadrant Layout (Top View)

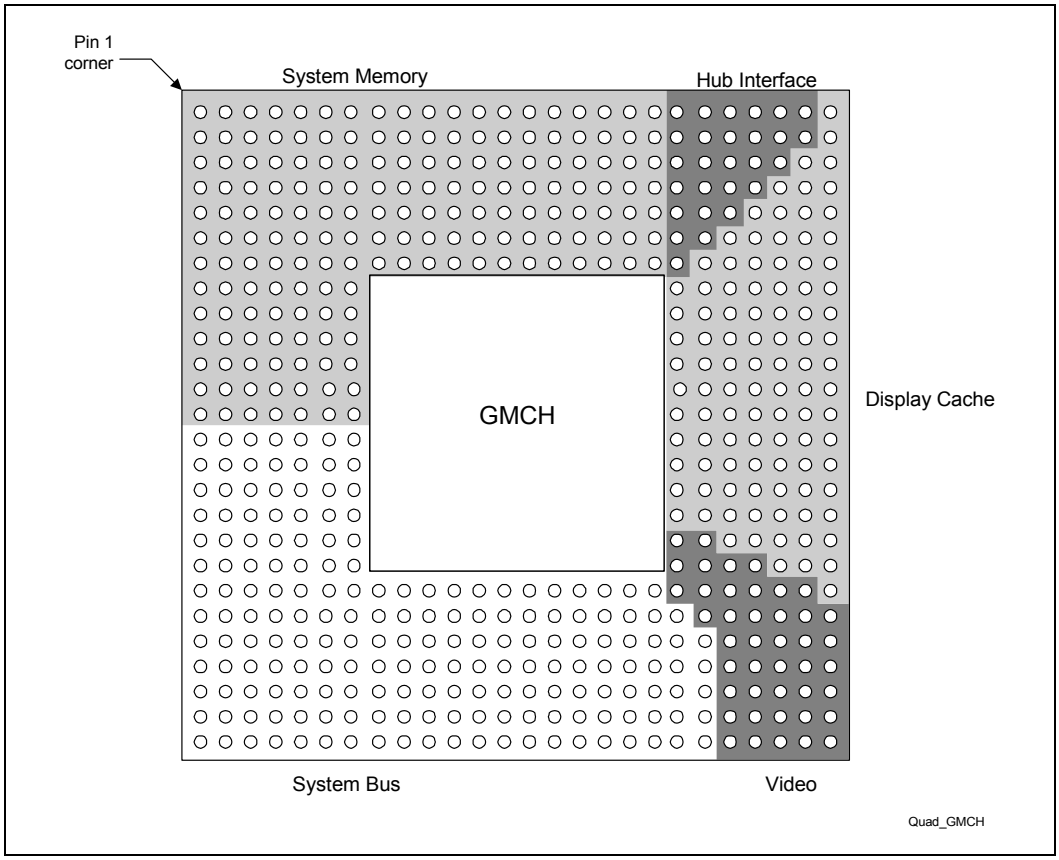


Figure 4 illustrates the relative signal quadrant locations on the ICH ballout. It does not represent the actual ballout. Refer to the *Intel® 82801AA I/O Controller Hub (ICH) and Intel® 82801BAM I/O Controller Hub (ICH-M)* Datasheet for the actual ballout.

Figure 4. ICH 241-Ball µBGA* CSP Quadrant Layout (Top View)

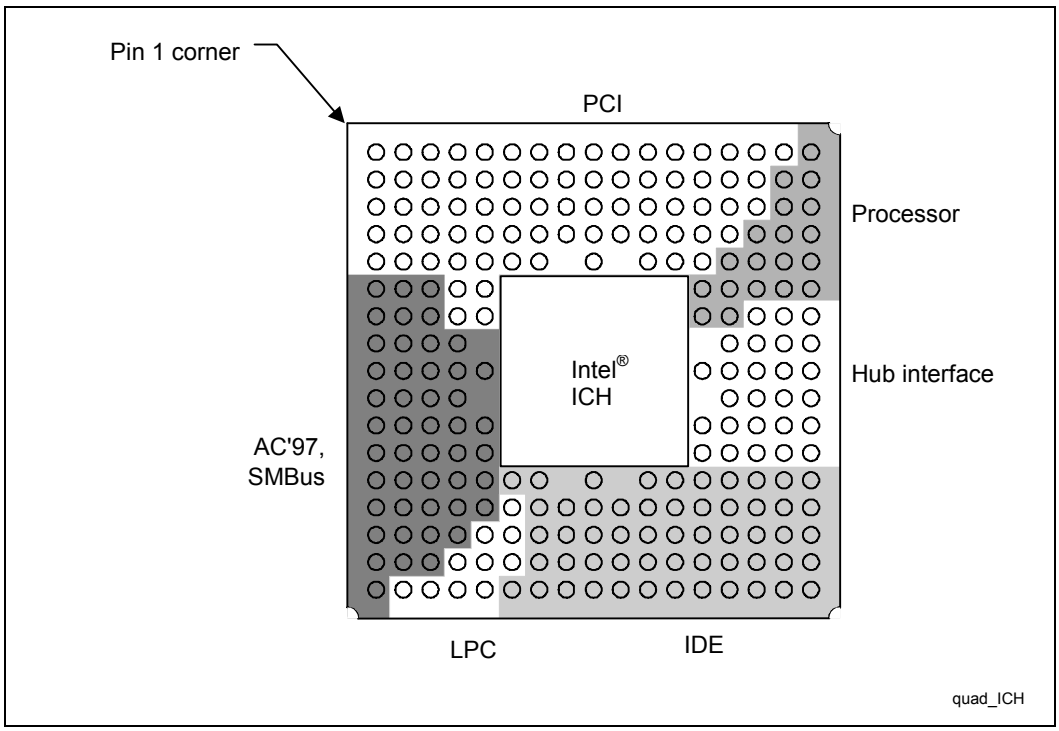
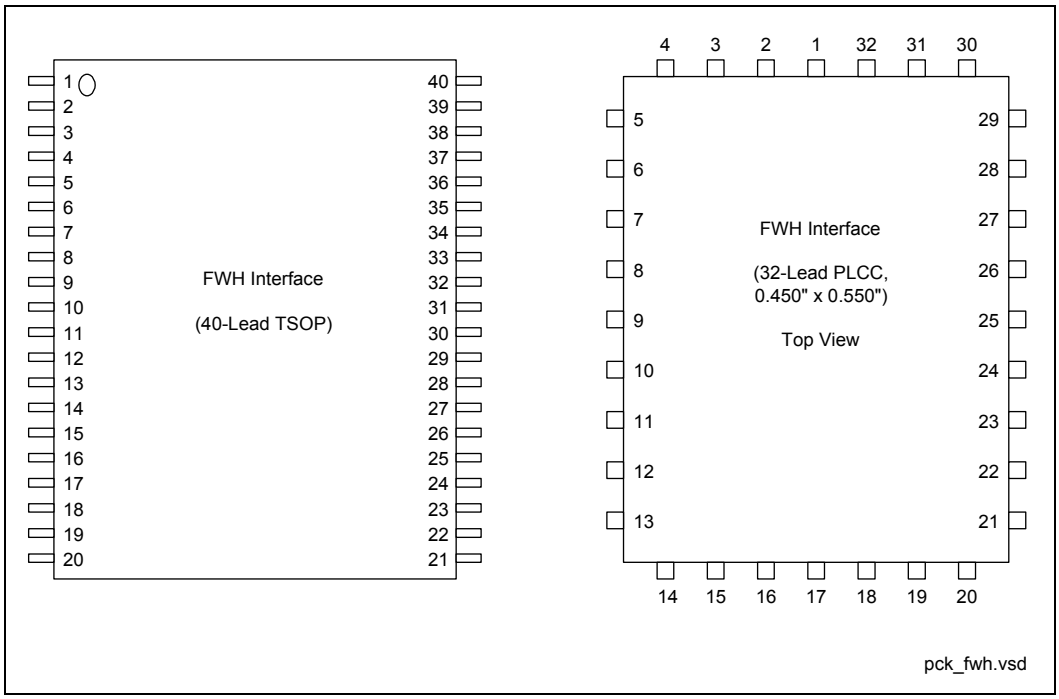


Figure 5. Firmware Hub (FWH) Packages



4 Universal Motherboard Design

4.1 Universal Motherboard Definition Details

The universal socket 370 platform supports Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh) as well as future 0.13 micron socket 370 processors. The Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh) have different requirements for functioning properly in a platform than the future 0.13 micron socket 370 processors. It is necessary to understand these differences and how they affect the design of the platform. Refer to Table 1 through Table 3 for a high-level description of the differences that require additional circuitry on the motherboard. Specific details on implementing this circuitry are discussed further in this chapter. For a detailed description of the pin differences between the Pentium III processor (CPUID=068xh) / Celeron processor (CPUID=068xh), and future 0.13 micron socket 370 processor pins, refer to Section 5.4.

Table 1. Processor Considerations for Universal Motherboard Design

Signal Name or Pin Number	Function In Intel® Pentium® III Processor (CPUID=068xh) and Intel® Celeron® Processor (CPUID=068xh)	Function In Future 0.13 Micron Socket 370 Processors	Implementation for Universal Socket 370 Design
AF36	VSS	No connect	Addition of circuitry that generates a processor identification signal used to configure board-level operation.
AG1	VSS	VTT	Addition of FET switch to ground or VTT, controlled by processor identification signal. **Note:** FET must have no more than 100 milliohms resistance between source and drain.
AJ3	**NC**	**NC**	**PGA 370 socket pin AJ3 is a "NC" (no connect) for either processor.**
AK22	GTL_REF	VCMOS_REF	Addition of resistor-divider network to provide 1.0V, which will satisfy voltage tolerance requirements of the Pentium® III processor (CPUID=068xh) and Celeron® processor (CPUID=068xh) as well as future 0.13 micron socket 370 processors.
PICCLK	Requires 2.5V	Requires 2.0V	Addition of FET switch to provide proper voltage, controlled by processor identification signal.

Signal Name or Pin Number	Function In Intel® Pentium® III Processor (CPUID=068xh) and Intel® Celeron® Processor (CPUID=068xh)	Function In Future 0.13 Micron Socket 370 Processors	Implementation for Universal Socket 370 Design
PWRGOOD	Requires 2.5V	Requires 1.8V	Addition of resistor-divider network to provide 2.1V, which will satisfy voltage tolerance requirements of the Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh) as well as future 0.13 micron socket 370 processors.
VTT	Requires 1.5V	Requires 1.25V	Modification to VTT generation circuit to switch between 1.5V or 1.25V, controlled by processor identification signal.
VTTPWRGD	Not used	Input signal to future 0.13 micron socket 370 processors to indicate that VID signals are stable	Addition of VTTPWRGD generation circuit.

Table 2. ICH Considerations for Universal Motherboard Design

Signal	Issue	Implementation For Universal Motherboard Design
PWROK	GMCH and CK810E must not sample BSEL[1:0] until VTTPWRGD asserted. ICH must not initialize before CK810E clocks stabilize	Addition of circuitry to have VTTPWRGD gate PWROK from power supply to ICH. The ICH will hold GMCH in reset until VTTPWRGD asserted plus 20 ms time delay to allow CK810E clocks to stabilize

Table 3. Clock Synthesizer Considerations for Universal Motherboard Design

Signal	Issue	Implementation For Universal Motherboard Design
VDD	CK810E does not support VTTPWRGD	Addition of a FET switch, which supplies power to VDD only when VTTPWRGD is asserted. Note: FET must have no more than 100 milliohms resistance between source and drain.

4.2 Processor Design Requirements

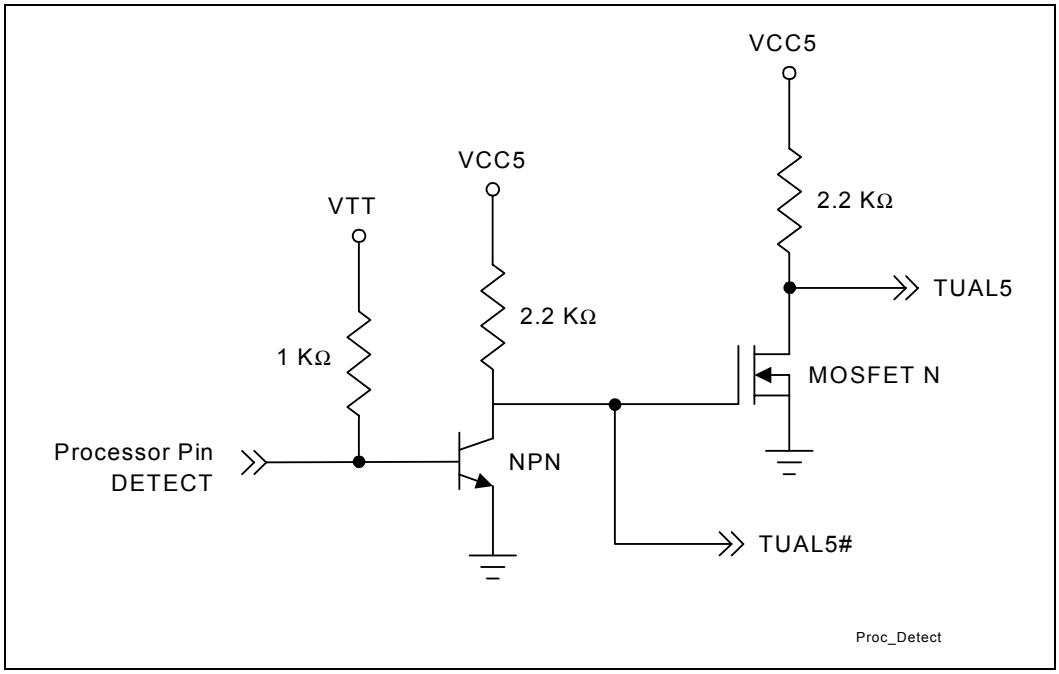
4.2.1 Use of Universal Motherboard Design With the 82810E GMCH

The universal socket 370 design is intended for use with the 810E chipset platform for use with the universal socket 370. A universal socket 370 design populated with an A0 stepping of the GMCH is compatible with future 0.13 micron socket 370 processors.

4.2.2 Identifying the Processor at the Socket

For the platform to configure for the requirements of the processor in the socket, it must first identify whether the processor is a Pentium III processor (CPUID=068xh) / Celeron processor (CPUID=068xh), or a future 0.13 micron socket 370 processors. Pin AF36 is a ground pin on a Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh); pin AF36 is an unconnected pin on future 0.13 micron Socket 370 processors. Referring to Figure 6, the platform uses a detect circuit connected to this processor pin. If a future 0.13 micron Socket 370 processor is present in the socket, the TUAL5 reference schematic signal will be pulled to the 5V rail and the TUAL5# reference schematic signal will be pulled to ground. Otherwise, for a Pentium III processor (CPUID=068xh) or Celeron processor (CPUID=068xh), the TUAL5 reference schematic signal will be pulled to ground and the TUAL5# will be pulled to the 5V rail.

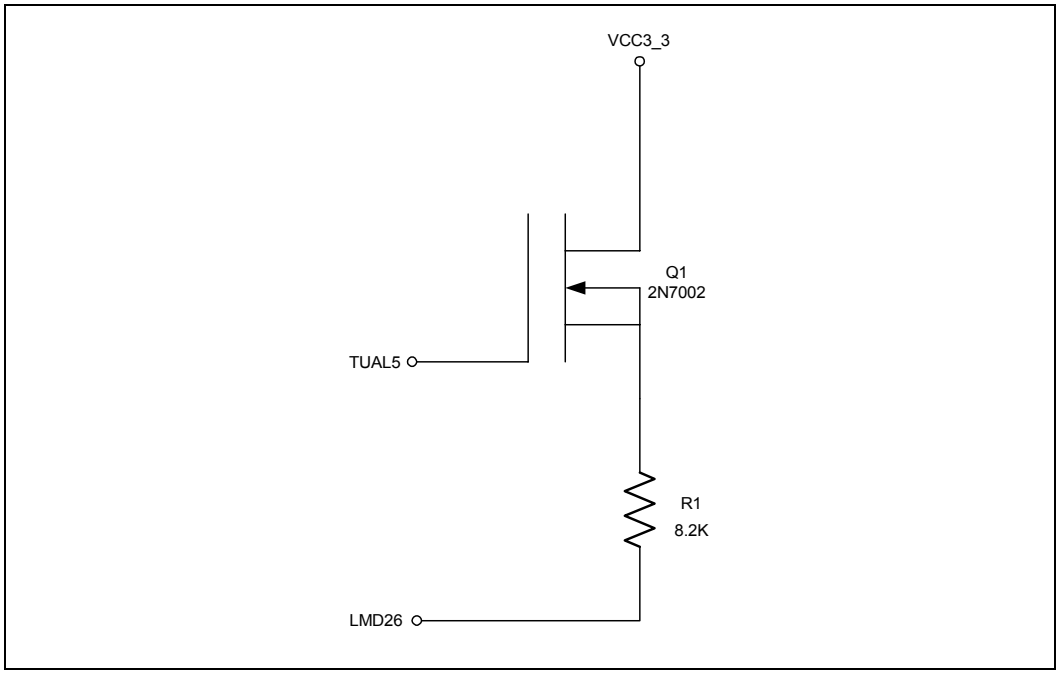
Figure 6. Processor Detect Mechanism at Socket/TUAL5 Generation Circuit



4.2.3 Setting Processor Auto-Detect

A processor auto-detect circuit for the functionality is shown as Figure 6, Section 4.2.2. A circuit that can use the processor auto-detect information to set LMD26 appropriately is shown as Figure 7, below.

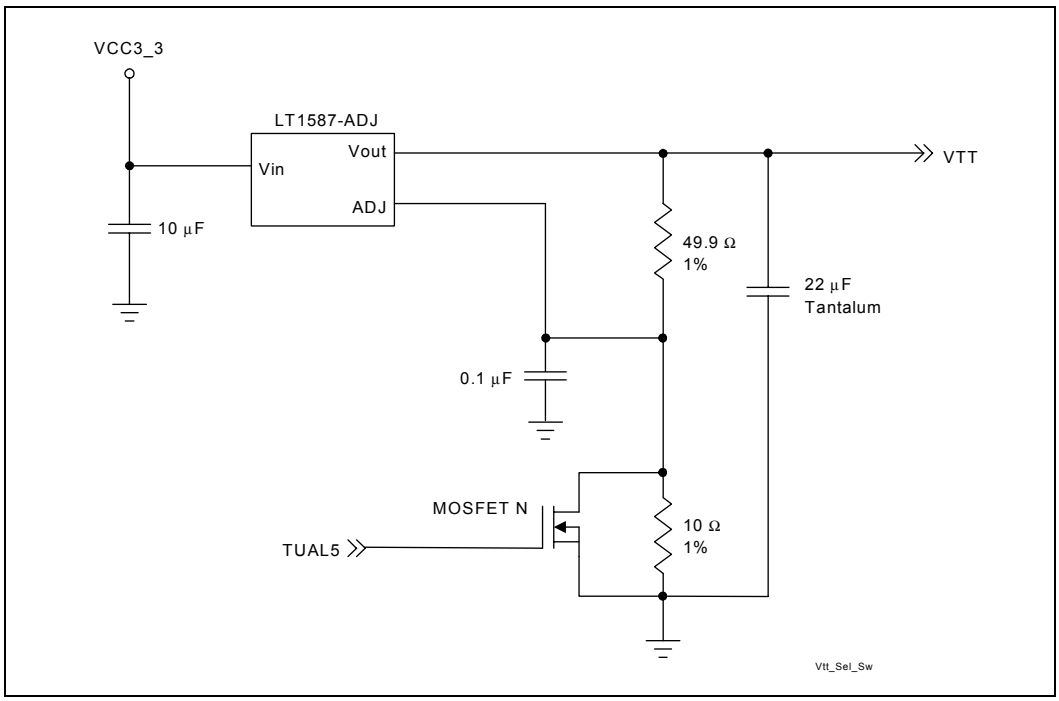
Figure 7 Processor Auto-Detect Circuit for LMD 26



4.2.4 Setting the Appropriate Processor VTT Level

Because the Pentium III processor (CPUID=068xh) / Celeron processor (CPUID=068xh), and future 0.13 micron socket 370 processors require different VTT levels, the platform must be able to provide the appropriate voltage level after determining which processor is in the socket. Referring to Figure 8, the TUAL5 reference schematic signal serves to control the FET, and by doing so determines whether the voltage regulator supplies 1.25V or 1.5V to VTT for AGTL or AGTL+, respectively.

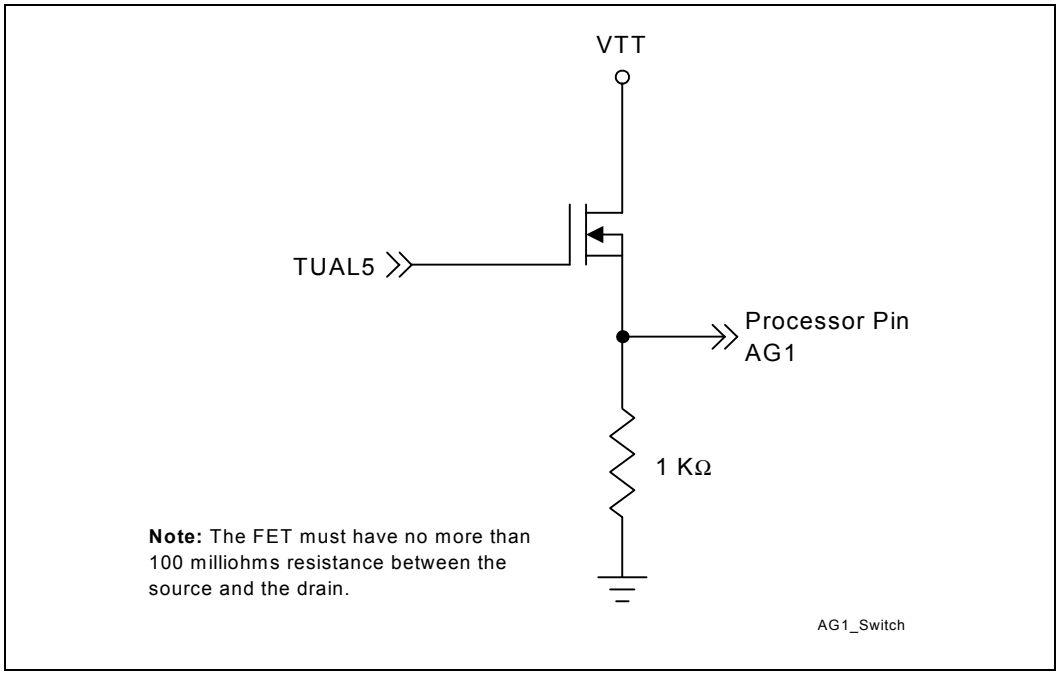
Figure 8. VTT Selection Switch



4.2.5 VTT Processor Pin AG1

Processor pin AG1 requires additional attention since it is a ground pin on a Pentium III processor (CPUID=068xh) / Celeron processor (CPUID=068xh) and a VTT pin on a future 0.13 micron socket 370 processor. A separate switch controlled by the TUAL5 reference schematic signal determines whether pin AG1 is pulled to ground or VTT. Refer to Figure 9 for an example implementation.

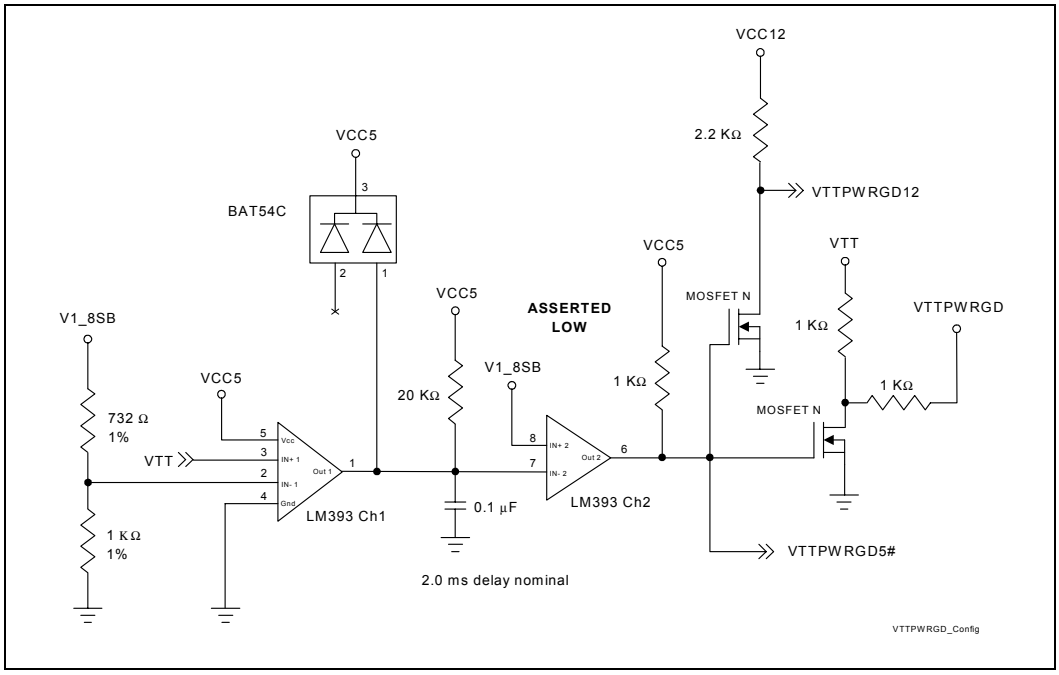
Figure 9. Switching Pin AG1



4.2.6 Configuring Non-VTT Processor Pins

When asserted, the VTTPWGRD signal must be level-shifted to 12 V to properly drive the gating circuitry of the CK810E. Furthermore, while the VTTPWRGD signal is connected to the VTTPWRGD pin on a future 0.13 micron socket 370 processor, on a Pentium III processor (CPUID=068xh) or Celeron processor (CPUID=068xh) that same pin is a ground. To provide proper functionality, a 1.0 kΩ resistor must be placed in series between the circuitry that generates the signal VTTPWRGD and the processor pin VTTPWRGD. Refer to Figure 10 for an example implementation. Voltage regulators that generate the standard VTTPWRGD signal are available.

Figure 10. VTTPWRGD Configuration Circuit

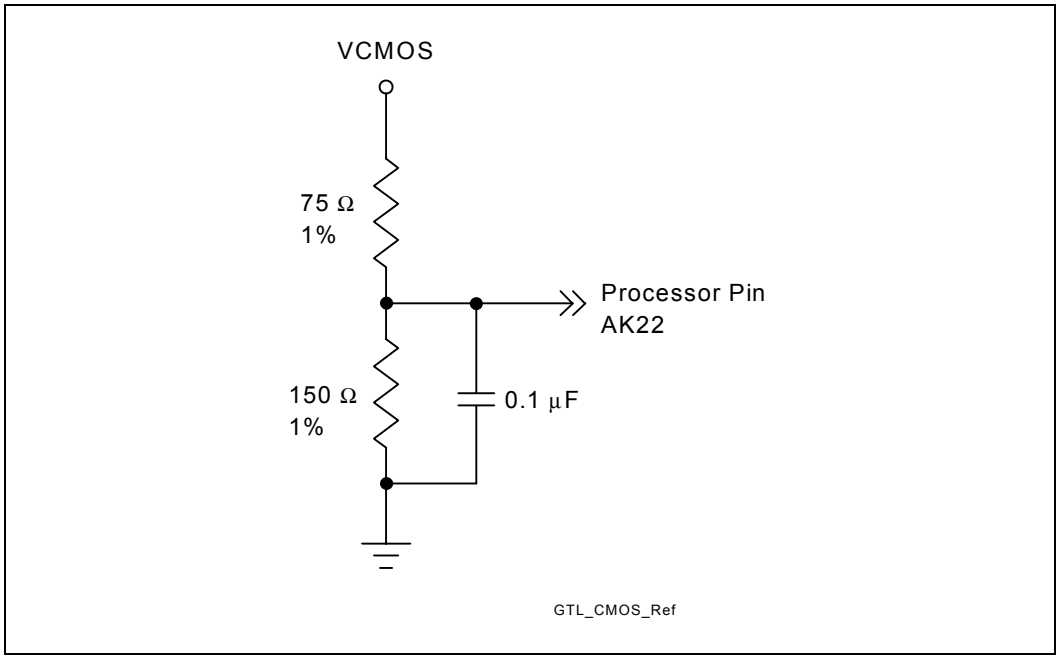


NOTE: The diode is included so that repeated pressing of the reset or power button does not cause the capacitor to build up enough charge to circumvent the 20 ms delay.

4.2.7 VCMOS Reference

In previous platforms supporting the Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh), VCMOS was generated by the same power plane as VTT. The future 0.13 micron socket 370 processors do not generate VCMOS, and the universal platform is required to generate this separately on the motherboard. Processor pin AK22, which is a GTL_REF pin on a Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh), has been changed to a VCMOS_REF pin on future 0.13 micron socket 370 processors. Referring to Figure 11, a network of resistors and a capacitor must be added so that this pin operates appropriately for whichever processor is in the socket).

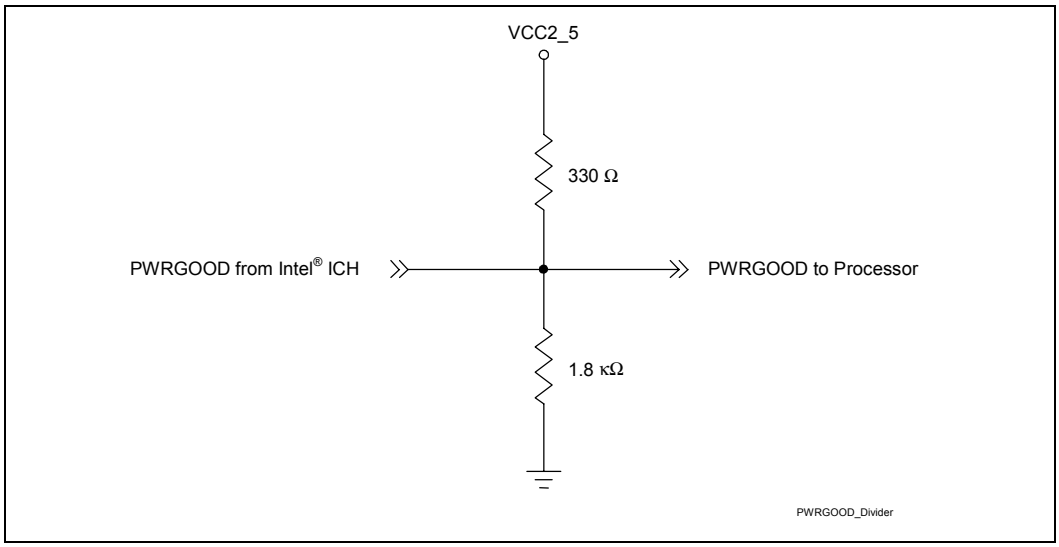
Figure 11. GTL_REF/VCMOS_REF Voltage Divider Network



4.2.8 Processor Signal PWRGOOD

The processor signal PWRGOOD is specified at different voltage levels depending on whether it is a Pentium III processor (CPUID=068xh) / Celeron processor (CPUID=068xh), or whether it is a future 0.13 micron socket 370 processor. As there is an overlap between the ranges of accepted voltage levels for these two processor groups, a resistor divider network that provides 2.1V will satisfy the requirements of all supported processors. See Figure 12 for an example implementation.

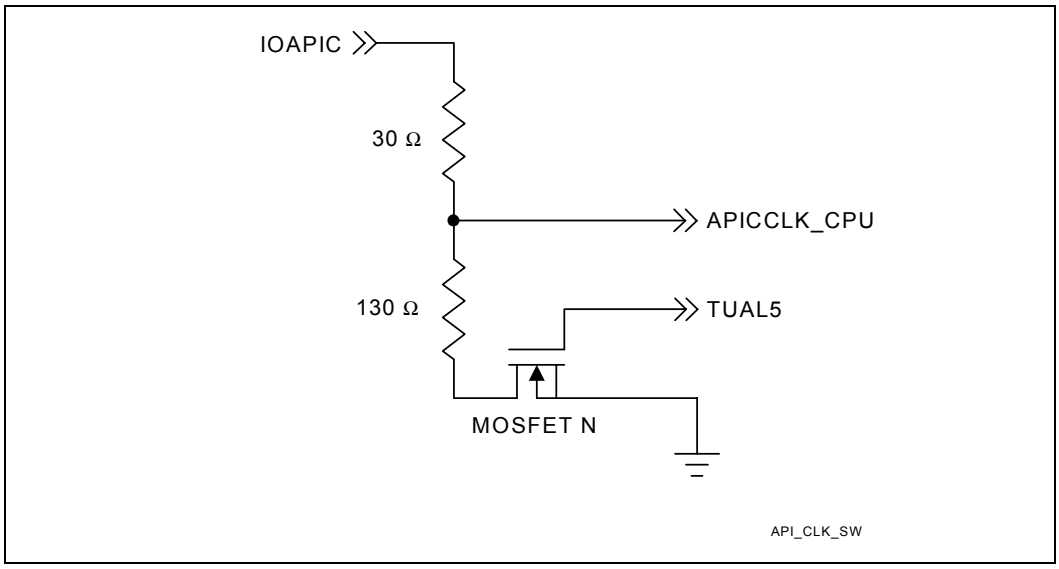
Figure 12. Resistor Divider Network for Processor PWRGOOD



4.2.9 APIC Clock Voltage Switching Requirements

The processor's APIC clock is also specified at different voltage levels depending on whether it is for the Pentium III processor (CPUID=068xh) / Celeron processor (CPUID=068xh) or whether it is for a future 0.13 micron socket 370 processor. There is no overlap in the range of accepted voltage levels for the two processor groups, so a voltage switch is required to ensure proper operation. Figure 13 shows an example implementation.

Figure 13 Voltage Switch For Processor APIC Clock

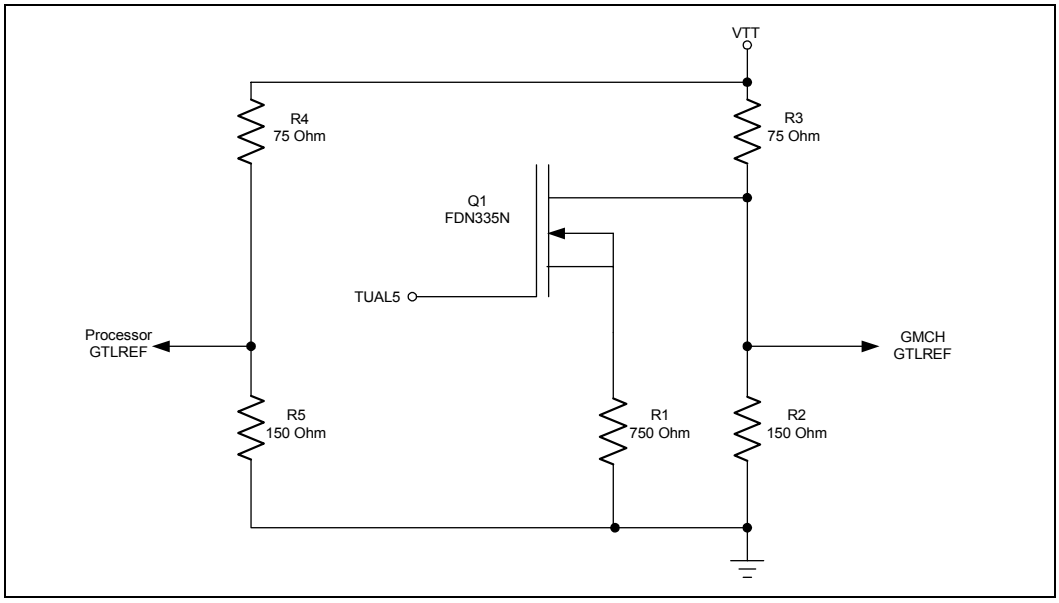


NOTE: the 30 Ω resistor represents the series resistor typically used in connecting the APIC clock to the processor.

4.2.10 GTLREF Topology and Layout

In a platform supporting the future 0.13 micron socket 370 processors, the voltage requirements for GTLREF are different for the processor and the chipset. This difference requires that separate resistor sites be added to the layout to split the GTLREF sources. In a universal motherboard design, a Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh) will be unaffected by the difference in GTLREF. The recommended GTLREF circuit topology is shown in Figure 14. To auto-set the appropriate GTLREF voltage depending on which processor is used in the platform.

Figure 14. GTLREF Circuit Topology



GTLREF Layout and Routing Guidelines

- Place all resistor sites for GTLREF generation close to the GMCH.
- Route GTLREF with as wide a trace as possible.
- Use one 0.1 µF decoupling capacitor for every two GTLREF pins at the processor (four capacitors total). Place as close as possible (within 500 mils) to the Socket 370 GTLREF pins.
- Use one 0.1 µF decoupling capacitor for each of the two GTLREF pins at the GMCH (two capacitors total). Place as close as possible to the GMCH GTLREF balls.

4.3 Power Sequencing on Wake Events

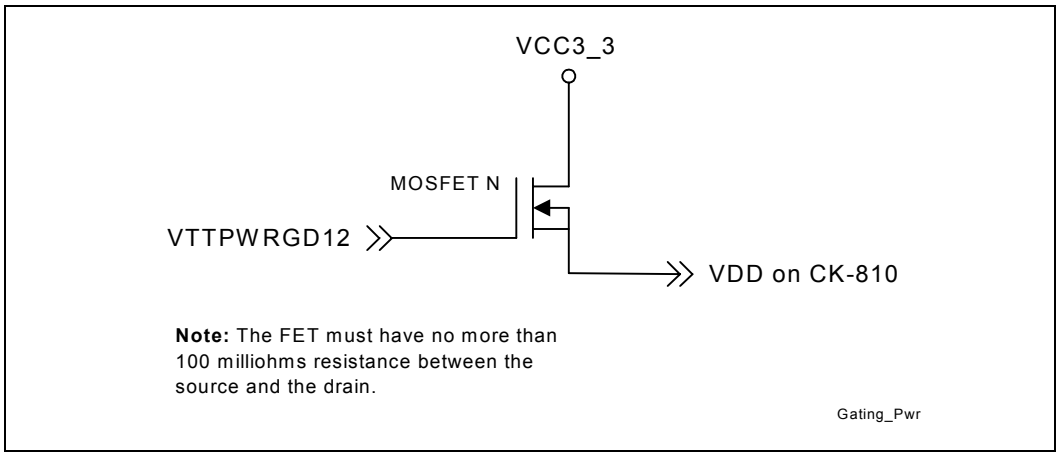
In addition to the mechanism for identifying the processor in the socket, special handling of wake events is required for 810E chipset universal platforms that support functionality of future 0.13 micron socket 370 processors. When a wake event is triggered, the GMCH and the CK810E must not sample BSEL[1:0] until the signal VTTPWRGD is asserted. This is handled by setting up the following sequence of events:

1. Power is not connected to the CK810E-compliant clock driver until VTTPWRGD12 is asserted.
2. Clocks to the ICH stabilize before the power supply asserts PWROK to the ICH. There is no guarantee this will occur as the implementation for the previous step relies on the 12 V supply. Thus it is necessary to gate PWROK to the ICH from the power supply while the CK810E is given sufficient time for the clocks to become stable. The amount of time required is a minimum 20 ms.
3. ICH takes the GMCH out of reset.
4. GMCH samples BSEL[1:0]. (CK-810E will have sampled BSEL[1:0] much earlier.)

4.3.1 Gating of CK810E to VTTPWRGD

System designers must ensure that the VTTPWRGD signal is asserted before the CK810E-compliant clock driver receives power. This is handled by having the 3.3 V rail of the clock driver gated by the VTTPWRGD12 reference schematic signal. Unlike previous 810E chipset designs, the 3.3 V standby rail is not used to power the clock as the VTTPWRGD12 reference schematic signal will cut power to the clock when going into any sleep state. Refer to Figure 15 for an example implementation.

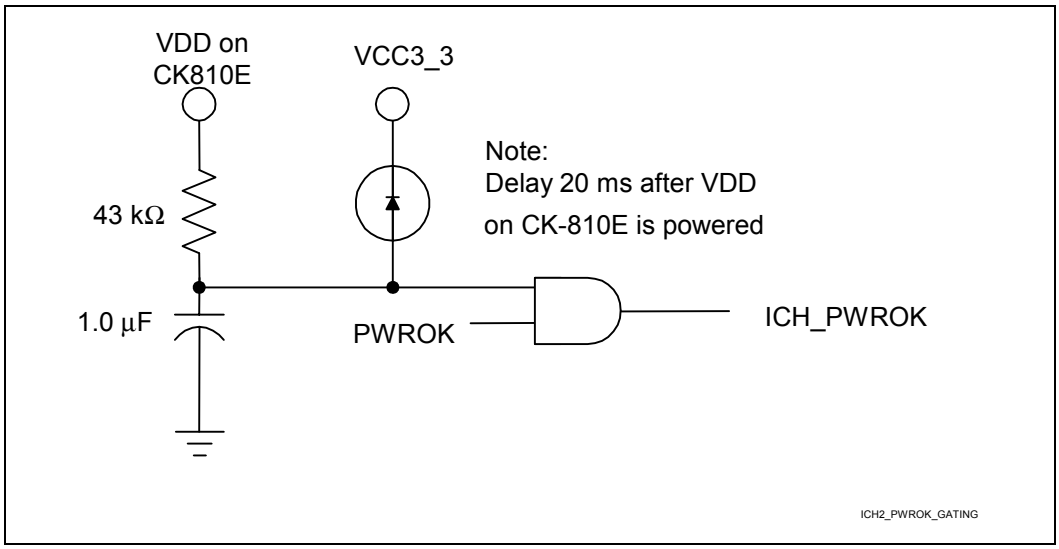
Figure 15. Gating Power to CK810E



4.3.2 Gating of PWROK to ICH

With power being gated to the CK810E by the signal VTTPWRGD12, it is important that the clocks to the ICH are stable before the power supply asserts PWROK to the ICH. As the clocking power gating circuitry relies on the 12 V supply, there is no guarantee that these conditions will be met. This is why an estimated minimum time delay of 20ms must be added after power is connected to the CK810E to give the clock driver sufficient time to stabilize. This time delay will gate the power supply's assertion of PWROK to the ICH. After the time delay, the power supply can safely assert PWROK to the ICH, with the ICH subsequently taking the GMCH out of reset. Refer to Figure 16 for an example implementation.

Figure 16 PWROK Gating Circuit For ICH



NOTE: The diode is included so that repeated pressing of the reset or power button does not cause the capacitor to build up enough charge to circumvent the 20ms delay.

5 System Bus Design Guidelines

The Pentium III processor delivers higher performance by integrating the Level 2 cache into the processor and running it at the processor's core speed. The Pentium III processor runs at higher core and system bus speeds than previous-generation IA-32 processors while maintaining hardware and software compatibility with earlier Pentium III processors. The new Flip Chip-Pin Grid Array 2 (FC-PGA2) package technology enables compatibility with previous Flip Chip-Pin Grid Array (FC-PGA) packages using the PGA370 socket.

This section presents the considerations for designs capable of using the 810E chipset universal platform with the full range of Pentium III processors using the PGA370 socket.

5.1 System Bus Routing Guidelines

The following layout guide supports designs using Pentium III processor (CPUID=068xh) / Celeron processor (CPUID=068xh), and future 0.13 micron socket 370 processors with the 810E chipset platform. The solution covers system bus speeds of 66/100/133 MHz for the Pentium III processor (CPUID=068xh) / Celeron processor (CPUID=068xh), and future 0.13 micron socket 370 processors. All processors must also be configured to 56 Ω on-die termination.

5.1.1 Initial Timing Analysis

Table 4 lists the AGTL/AGTL+ component timings of the processors and 810E chipset universal platform's GMCH defined at the pins. **These timings are for reference only. Obtain each processor's specifications from its respective processor datasheet and the chipset values from the appropriate 810E chipset datasheet.**

Table 4. Intel® Pentium® III Processor AGTL/AGTL+ Parameters for Example Calculations

IC Parameters	Intel® Pentium® III Processor at 133 MHz System Bus	82810E GMCH	Notes
Clock to Output maximum (T_{CO_MAX})	3.25 ns (for 66/100/133 MHz system bus speeds)	4.1 ns	1, 2
Clock to Output minimum (T_{CO_MIN})	0.40 ns (for 66/100/133 MHz system bus)	1.05 ns	1, 2
Setup time (T_{SU_MIN})	1.20 ns for BREQ Lines 0.95 ns for all other AGTL/AGTL+ Lines @ 133 MHz 1.20 ns for all other AGTL/AGTL+ Lines @ 66/100 MHz	2.65 ns	1, 2,3
Hold time (T_{HOLD})	1.0 ns (for 66/100/133 MHz system bus speeds)	0.10 ns	1

NOTES:
1. All times in nanoseconds.
2. **Numbers in table are for reference only**. These timing parameters are subject to change. Check the appropriate component documentation for the valid timing parameter values.
3. T_{SU_MIN} = 2.65 ns assumes that the GMCH sees a minimum edge rate equal to 0.3 V/ns.

Table 5 contains an example AGTL+ initial maximum flight time, and Table 6 contains an example minimum flight time calculation for a 133 MHz, uniprocessor system using the Pentium III processor and the 810E chipset universal platform's system bus. Note that assumed values were used for the clock skew and clock jitter. **The clock skew and clock jitter values depend on the clock components and the distribution method chosen for a particular design and must be budgeted into the initial timing equations, as appropriate for each design.**

Table 5 and Table 6 were derived assuming the following:

- CLK_{SKEW} = 0.20 ns (Note: This assumes that the clock driver pin-to-pin skew is reduced to 50 ps by tying the two host clock outputs together (i.e., "ganging") at the clock driver output pins, and that the PCB clock routing skew is 150 ps. The system timing budget must assume 0.175 ns of clock driver skew if outputs are not tied together as well as the use of a clock driver that meets the CK810E Clock Synthesizer/Driver Specification.)
- CLKJITTER = 0.250 ns

See the respective processor's datasheet, the appropriate 810E chipset universal documentation, and the *CK810E Clock Synthesizer/Driver Specification* for details on clock skew and jitter specifications. Exact details regarding the host clock routing topology are provided with the platform design guideline.

Table 5. Example T_{FLT_MAX} Calculations for 133 MHz Bus

Driver	Receiver	Clk Period[2]	T_{CO_MAX}	T_{SU_MIN}	Clk_{SKEW}	Clk_{JITTER}	M_{ADJ}	Recommended T_{FLT_MAX}
Processor	GMCH	7.50	3.25	2.65	0.20	0.25	0.40	1.1
GMCH	Processor	7.50	4.1	1.20	0.20	0.25	0.40	1.35

NOTES:
1. All times in nanoseconds
2. BCLK period = 7.50 ns @ 133.33 MHz

Table 6. Example T_{FLT_MIN} Calculations (Frequency Independent)

Driver	Receiver	T_{HOLD}	Clk_{SKEW}	T_{CO_MIN}	Recommended T_{FLT_MIN}
Processor	GMCH	0.10	0.20	0.40	0.10
GMCH	Processor	1.00	0.20	1.05	0.15

NOTE: All times in nanoseconds

The flight times in Table 5 include margin to account for the following phenomena that Intel observed when multiple bits are switching simultaneously. These multi-bit effects can adversely affect the flight time and signal quality and sometimes are not accounted for during simulation. Accordingly, the maximum flight times depend on the baseboard design, and additional adjustment factors or margins are recommended.

- SSO push-out or pull-in
- Rising or falling edge rate degradation at the receiver caused by inductance in the current return path, requiring extrapolation that causes additional delay
- Crosstalk on the PCB and inside the package which can cause variation in the signals

Additional effects exist that **may not necessarily** be covered by the multi-bit adjustment factor and should be budgeted as appropriate to the baseboard design. These effects are included as M_{ADJ} in the example calculations in Table 5. Examples include:

- The effective board propagation constant (SEFF), which is a function of:
  - Dielectric constant (εr) of the PCB material
  - Type of trace connecting the components (stripline or microstrip)
  - Length of the trace and the load of the components on the trace. Note that the board propagation constant multiplied by the trace length is a **component** of the flight time, **but not necessarily equal to** the flight time.

5.2 General Topology and Layout Guidelines

Figure 17. Topology for 370-Pin Socket Designs with Single-Ended Termination (SET)

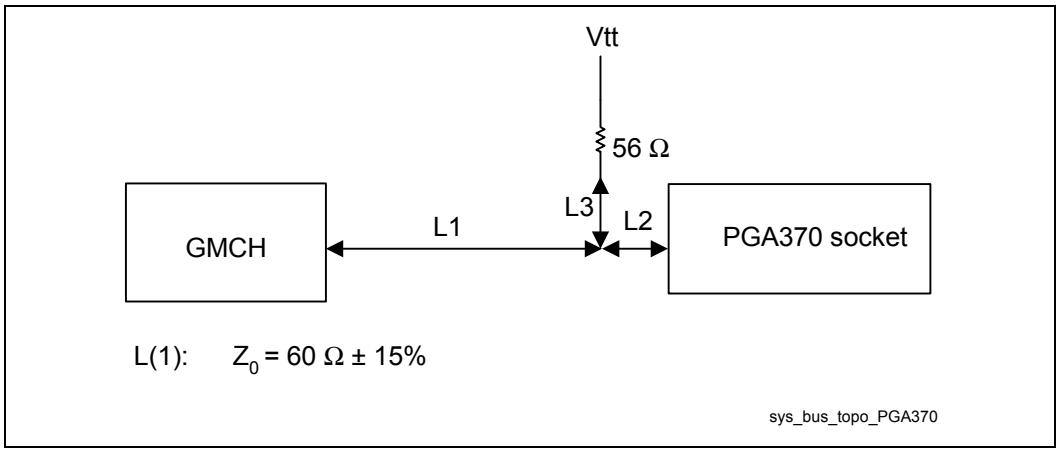


Table 7. Trace Guidelines for Figure 17

Description	Min. Length (inches)	Max. Length (inches)
GMCH to PGA370 socket trace	1.90	4.50

NOTE: All AGTL/AGTL+ bus signals should be referenced to the ground plane for the entire route.

- Use an intragroup AGTL/AGTL+ spacing : line width : dielectric thickness ratio of at least 2:1:1 for microstrip geometry. If εr = 4.5, this should limit coupling to 3.4%. For example, intragroup AGTL+ routing could use 10-mil spacing, 5-mil traces, and a 5-mil prepreg between the signal layer and the plane it references (assuming a 4-layer motherboard design).
- The recommended trace width is 5 mils, but not greater than 6 mils.

Table 8 contains the trace width : space ratios assumed for this topology. Three types of crosstalk are considered in this guideline: Intragroup AGTL/AGTL+, Intergroup AGTL/AGTL+, and AGTL/AGTL+ to non-AGTL/AGTL+. Intragroup AGTL/AGTL+ crosstalk involves interference between AGTL/AGTL+ signals within the same group. Intergroup AGTL/AGTL+ crosstalk involves interference from AGTL/AGTL+ signals in a particular group to AGTL/AGTL+ signals in a different group. An example of AGTL/AGTL+ to non-AGTL/AGTL+ crosstalk is when CMOS and AGTL/AGTL+ signals interfere with each other. The AGTL/AGTL+ signals consist of the following groups: data signals, control signals, clock signals, and address signals.

Table 8. Trace Width: Space Guidelines

Crosstalk Type	Trace Width:Space Ratios[1, 2]
Intragroup AGTL/AGTL+ signals (same group AGTL/AGTL+)	5:10 or 6:12
Intergroup AGTL/AGTL+ signals (different group AGTL/AGTL+)	5:15 or 6:18
AGTL/AGTL+ to System Memory Signals	5:30 or 6:36
AGTL/AGTL+ to non-AGTL/AGTL+	5:25 or 6:24

NOTES:
1. Edge to edge spacing.
2. Units are in mils.

5.2.1 Motherboard Layout Rules for AGTL/AGTL+ Signals

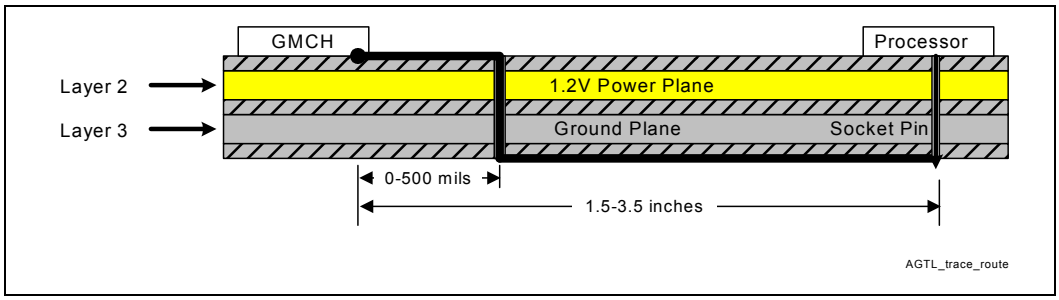
5.2.1.1 Ground Reference

It is strongly recommended that AGTL/AGTL+ signals be routed on the signal layer next to the ground layer (referenced to ground). It is important to provide an effective signal return path with low inductance. The best signal routing is directly adjacent to a solid GND plane with no splits or cuts. Eliminate parallel traces between layers not separated by a power or ground plane. If a signal has to go through routing layers, the recommendations are:

Note: Following these layout rules is critical for AGTL/AGTL+ signal integrity, particularly for 0.18 micron and smaller process technology.

For signals going from a ground reference to a power reference, add capacitors between ground and power near the vias to provide an AC return path. One capacitor should be used for every three signal lines that change reference layers. Capacitor requirements are as follows: C=100 nF, ESR=80 mΩ, ESL=0.6 nH. Refer to Figure 18 for an example of switching reference layers.

Figure 18. AGTL/AGTL+ Trace Routing



NOTE: For signals going from one ground reference to another, separate ground reference, add vias between the two ground planes to provide a better return path.

5.2.1.2 Reference Plane Splits

Splits in reference planes disrupt signal return paths and increase overshoot/undershoot due to significantly increased inductance.

5.2.1.3 Processor Connector Breakout

It is strongly recommended that AGTL/AGTL+ signals do not traverse multiple signal layers. Intel recommends breaking out all signals from the connector on the same layer. If routing is tight, break out from the connector on the opposite routing layer over a ground reference and cross over to main signal layer near the processor connector.

5.2.1.4 Minimizing Crosstalk

The following general rules minimize the impact of crosstalk in a high-speed AGTL/AGTL+ bus design:

- Maximize the space between traces. Wherever possible, maintain a minimum of 10 mils (assuming a 5-mil trace) between trace edges. It may be necessary to use tighter spacing when routing between component pins. When traces must be close and parallel to each other, minimize the distance that they are close together and maximize the distance between the sections when the spacing restrictions are relaxed.
- Avoid parallelism between signals on adjacent layers, if there is no AC reference plane between them. As a rule of thumb, route adjacent layers orthogonally.
- Since AGTL/AGTL+ is a low-signal-swing technology, it is important to isolate AGTL/AGTL+ signals from other signals by at least 25 mils. This will avoid coupling from signals that have larger voltage swings, such as 5 V PCI.
- AGTL/AGTL+ signals must be well isolated from system memory signals. AGTL/AGTL+ signal trace edges must be at least 30 mils from system memory trace edges within 100 mils of the ball of the Intel 82810E GMCH.
- Select a board stack-up that minimizes the coupling between adjacent signals. Minimize the nominal characteristic impedance within the AGTL/AGTL+ specification. Minimizing the height of the trace from its reference plane, which minimizes crosstalk, can do this.
- Route AGTL/AGTL+ address, data, and control signals in separate groups to minimize crosstalk between groups. Keep at least 15 mils between each group of signals.
- Minimize the dielectric used in the system. This makes the traces closer to their reference plane and thus reduces the crosstalk magnitude.
- Minimize the dielectric process variation used in the PCB fabrication.
- Minimize the cross-sectional area of the traces. This can be done by means of narrower traces and/or by using thinner copper, but the trade-off for this smaller cross-sectional area is higher trace resistivity, which can reduce the falling-edge noise margin because of the I*R loss along the trace.

5.2.1.5 Motherboard Layout Rules for Non-AGTL/AGTL+ (CMOS) Signals

Table 9. Routing Guidelines for Non-AGTL/AGTL+ Signals

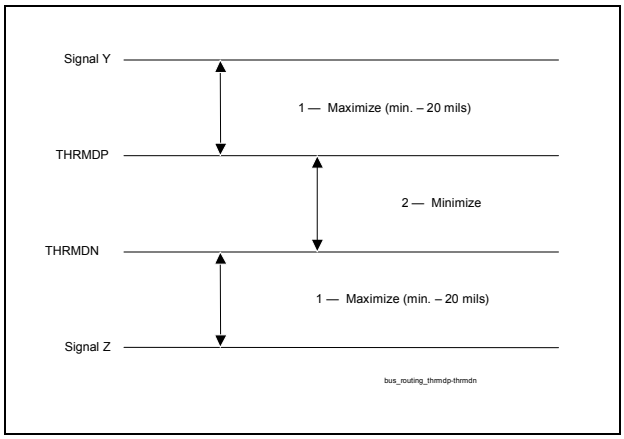
Signal	Trace Width	Spacing to Other Traces	Trace Length
A20M#	5 mils	10 mils	1” to 9”
FERR#	5 mils	10 mils	1” to 9”
FLUSH#	5 mils	10 mils	1” to 9”
IERR#	5 mils	10 mils	1” to 9”
IGNNE#	5 mils	10 mils	1” to 9”
INIT#	5 mils	10 mils	1” to 9”
LINT[0] (INTR)	5 mils	10 mils	1” to 9”
LINT[1] (NMI)	5 mils	10 mils	1” to 9”
PICD[1:0]	5 mils	10 mils	1” to 9”
PREQ#	5 mils	10 mils	1” to 9”
PWRGOOD	5 mils	10 mils	1” to 9”
SLP#	5 mils	10 mils	1” to 9”
SMI#	5 mils	10 mils	1” to 9”
STPCLK	5 mils	10 mils	1” to 9”
THERMTRIP#	5 mils	10 mils	1” to 9”

NOTES:
1. Route these signals on any layer or combination of layers.

5.2.1.6 THRMDP and THRMDN

These traces (THRMDP and THRMDN) route the processor’s thermal diode connections. The thermal diode operates at very low currents and may be susceptible to crosstalk. The traces should be routed close together to reduce loop area and inductance.

Figure 19. Routing for THRMDP and THRMD



NOTES:
1. Route these traces parallel and equalize lengths within ± 0.5 inches.
2. Route THRMDP and THRMDN on the same layer.

5.2.1.7 Additional Routing and Placement Considerations

- Distribute VTT with a wide trace. A 0.050 inches minimum trace is recommended to minimize DC losses. Route the VTT trace to all components on the host bus. Be sure to include decoupling capacitors.
- The VTT voltage should be 1.5 V ± 3% for static conditions, and 1.5 V ± 9% for worst-case transient conditions when a Pentium III processor (CPUID=068xh) or Celeron processor (CPUID=068xh) processor are present in the socket. If a future 0.13 micron socket 370 processor is being used, the VTT voltage should then be 1.25 V ± 3% for static conditions, and 1.25 V ± 9% for worst-case transient conditions.
- Place resistor divider pairs for VREF generation at the GMCH component. VREF also is delivered to the processor.

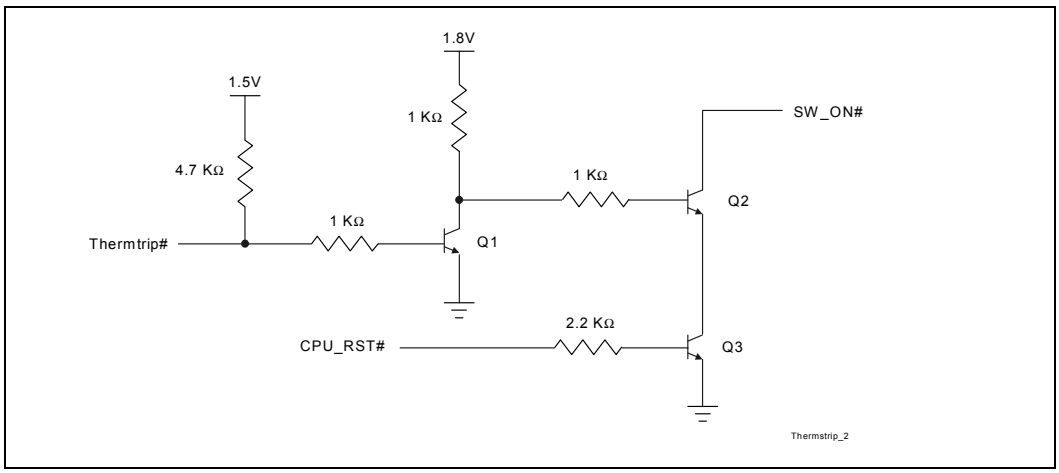
5.3 Electrical Differences for Universal PGA370 Designs

There are several electrical changes between previous PGA370 designs and the *universal PGA370* design, as follows:

- Changes to the PGA370 socket pin definitions.
- Addition of VTTPWRGD signal to ensure stable VID selection for future 0.13 micron socket 370 processors.
- Addition of THERMTRIP circuit to allow processor to detect catastrophic overheat.
- Addition of VID[25mV] signal to support future 0.13 micron socket 370 processors.
- Processor VTT level is switchable to 1.25V or 1.5V, depending on which processor is present in the socket.
- In designs using future 0.13 micron socket 370 processors, the processor does not generate VCMOS_REF.

5.3.1 THERMTRIP Circuit

Figure 20. Example Implementation of THERMTRIP Circuit



NOTES:

1. The pull-up voltage on the collector of Q1 is required to be 1.8V derived from a 3.3V source.
2. THERMTRIP is not valid until after CPU_RST# is deasserted. This is handled by gating the assertion of THERMTRIP with CPU_RST#. Using the CPU_RST# in this manner has minimal impact to the signal quality.
3. THERMTRIP must not go higher than VCC_{CMOS} levels. The pull-up on THERMTRIP is now connected to 1.5V.
4. CPU_RST# must gate SW_ON# from ground. This prevents glitching on SW_ON# during power-up and powerdown.
5. The resistance to the base of the transistor gating CPU_RST# must be at least 2.2 kΩ for proper Vih levels on CPU_RST#.

5.3.1.1 THERMTRIP Timing

When the THERMTRIP signal is asserted, both the VCC and VTT supplies to the processor must be turned off to prevent thermal runaway of the processor. The time required from THERMTRIP asserted to VCC rail at ½ nominal is 500ms and THERMTRIP asserted to VTT rail at ½ nominal is 500ms. System designers must ensure that the decoupling scheme used on these rails does not violate the THERMTRIP timing specifications.

5.3.1.2 Workaround for THERMTRIP on 0.13 Micron Processors with CPUID=6B1h

A platform supporting the future 0.13 micron socket 370 processors must implement a workaround required for the future 0.13 micron socket 370 processor with a CPUID = 06B1h. The internal control register bit responsible for operation of the THERMTRIP circuit functionality may power up in an uninitialized state. As a result, THERMTRIP# may be incorrectly asserted during deassertion of RESET# at nominal operating temperatures. When THERMTRIP# is asserted as a result of this situation, the processor may shut down internally and stop execution. In addition, when the THERMTRIP# pin is asserted, the processor may incorrectly continue to execute, leading to intermittent system power-on boot failures. The occurrence and repeatability of failures is system dependent; however, all systems and processors are susceptible to failure.

To prevent the risk of power-on boot failures, a platform workaround is required. The system must provide a rising edge on the TCK signal during the power-on sequence that meets all of the following requirements:

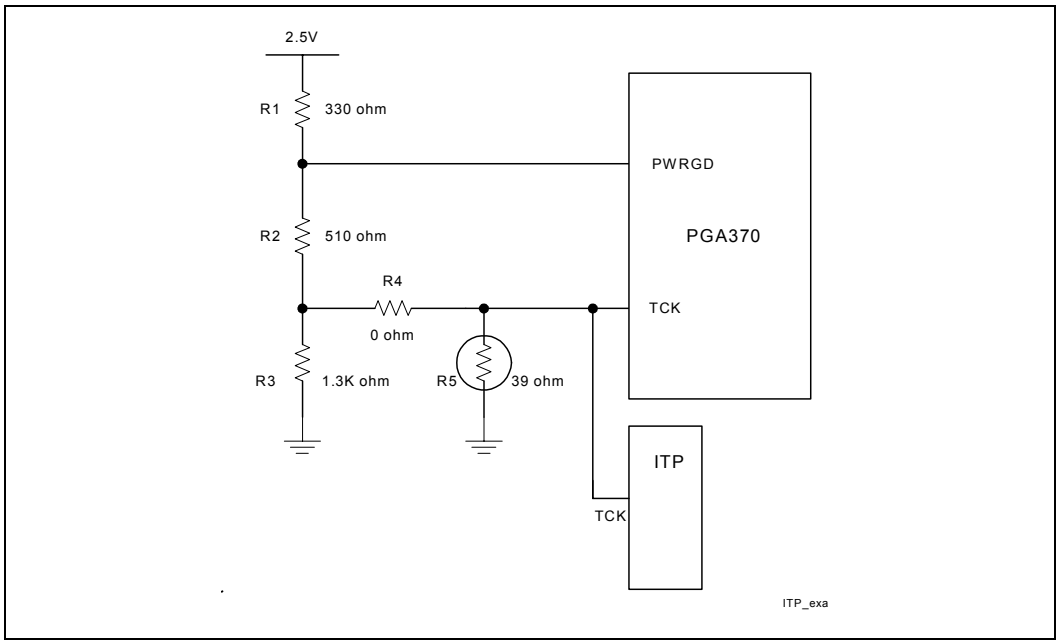
- •Rising edge occurs after VCC_{CORE} is valid and stable
- •Rising edge occurs before or at the deassertion of RESET#
- •Rising edge occurs after all VREF input signals are at valid voltage levels
- •TCK input meets the Vih min (1.3V) and max (1.65V) specification requirements

Specific workaround implementations may be platform specific. The following examples have been tested as acceptable workaround implementations.

The example workaround circuits (see Figure 21) attached require circuit modification for ITP tools to function correctly. These modifications must remove the workaround circuitry from the platform and may cause systems to fail to boot. Review the accompanying notes with each workaround for ITP modification details. If the system fails to boot when using ITP, issuing the ITP 'Reset Target' command on failing systems will reset the system and provide a sufficient rising edge on the TCK pin to ensure proper system boot.

In addition, the example workaround circuits shown do not support production motherboard test methodologies that require the use of the processor JTAG/TAP port. Alternative workaround solutions must be found if such test capability is required.

Figure 21. Example Circuit Showing ITP Workaround



NOTES:
1. For Production Boards:
   Depopulate R5
2. To use ITP:
   Install R5, Depopulate R4

5.4 PGA370 Socket Definition Details

Table 10 compares the pin names and functions of the Intel processors supported in the 810E chipset universal platform.

Table 10. Processor Pin Definition Comparison

Pin #	Intel® Celeron® Processor (CPUID = 068xh) Pin Name	Intel® Pentium® III Processor (CPUID=068xh) Pin Name	Intel® Pentium® III Processor that uses 0.13 Micron Technology Pin Name	Function
AA33	Reserved	V_{TT}	V_{TT}	• AGTL/AGTL+ termination voltage
AA35	Reserved	V_{TT}	V_{TT}	• AGTL/AGTL+ termination voltage
AB36	VCC_{CMOS}	VCC_{CMOS}	V_{TT}	• CMOS voltage level for Pentium III processor (CPUID=068xh) and Intel® Celeron® processor (CPUID=068xh) • AGTL termination voltage for future 0.13 micron socket 370 processors
AD36	VCC1.5	VCC1.5	V_{TT}	• VCC1.5 for Intel® Pentium® III processor (CPUID=068xh) and Celeron processor (CPUID=068xh) • V_{TT} for future 0.13 micron socket 370 processors
AF36	VSS	VSS	DETECT	• Ground for Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh) • No connect for future 0.13 micron socket 370 processors
AG1[1]	VSS	VSS	V_{TT}	• Ground for Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh) • V_{TT} for future 0.13 micron socket 370 processors
AH4	Reserved	RESET#	RESET#	• Processor reset for the Pentium III processor (068xh) and future 0.13 micron socket 370 processors
AH20	Reserved	V_{TT}	V_{TT}	• AGTL/AGTL+ termination voltage

Pin #	Intel® Celeron® Processor (CPUID = 068xh) Pin Name	Intel® Pentium® III Processor (CPUID=068xh) Pin Name	Intel® Pentium® III Processor that uses 0.13 Micron Technology Pin Name	Function
AJ3[1]	VSS	VSS	RESET2#	• Ground for Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh) • RESET for future 0.13 micron socket 370 processors
AK4	VSS	VSS	VTTPWRGD	• Ground for Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh) • VID control signal on future 0.13 micron socket 370 processors
AK16	Reserved	VTT	VTT	• AGTL/AGTL+ termination voltage
AK22	GTL_REF	GTL_REF	VCMOS_REF	• GTL reference voltage for Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh) • CMOS reference voltage future 0.13 micron socket 370 processors
AK36	VSS	VSS	VID[25mV]	• Ground for Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh) • 25mV step VID select bit for future 0.13 micron socket 370 processors
AL13	Reserved	VTT	VTT	• AGTL/AGTL+ termination voltage
AL21	Reserved	VTT	VTT	• AGTL/AGTL+ termination voltage
AN3	GND	GND	DYN_OE	• Ground for Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh) • Dynamic output enable for future 0.13 micron socket 370 processors
AN11	Reserved	VTT	VTT	• AGTL/AGTL+ termination voltage
AN15	Reserved	VTT	VTT	• AGTL/AGTL+ termination voltage
AN21	Reserved	VTT	VTT	• AGTL/AGTL+ termination voltage

Pin #	Intel® Celeron® Processor (CPUID = 068xh) Pin Name	Intel® Pentium® III Processor (CPUID=068xh) Pin Name	Intel® Pentium® III Processor that uses 0.13 Micron Technology Pin Name	Function
E23	Reserved	VTT	VTT	• AGTL/AGTL+ termination voltage
G35	Reserved	VTT	VTT	• AGTL/AGTL+ termination voltage
G37	Reserved	Reserved	VTT	• Reserved for Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh) • AGTL termination voltage for future 0.13 micron socket 370 processors
N37	NC	NC	NCHCTRL	• No connect for Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh) • NCHCTRL for future 0.13 micron socket 370 processors
S33	Reserved	VTT	VTT	• AGTL/AGTL+ termination voltage
S37	Reserved	VTT	VTT	• AGTL/AGTL+ termination voltage
U35	Reserved	VTT	VTT	• AGTL/AGTL+ termination voltage
U37	Reserved	VTT	VTT	• AGTL/AGTL+ termination voltage
W3	Reserved	A34#	A34#	• Additional AGTL/AGTL+ address
X4[1]	RESET#	RESET2#	VSS	• Processor reset Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh) • Ground for future 0.13 micron socket 370 processors
X6	Reserved	A32#	A32#	• Additional AGTL/AGTL+ address
X34	VCC_{CORE}	VCC_{CORE}	VTT	• Reserved for Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh) • AGTL termination voltage for future 0.13 micron socket 370 processors

Pin #	Intel® Celeron® Processor (CPUID = 068xh) Pin Name	Intel® Pentium® III Processor (CPUID=068xh) Pin Name	Intel® Pentium® III Processor that uses 0.13 Micron Technology Pin Name	Function
Y1	Reserved	Reserved	Reserved	• Reserved for Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh) • No connect for future 0.13 micron socket 370 processors
Y33	Reserved	CLKREF	CLKREF	• 1.25 V PLL reference
Z36	VCC2.5	VCC2.5	Reserved	• VCC2.5 for Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh) • No connect for future 0.13 micron socket 370 processors

NOTES:
1. Refer to Chapter 4.

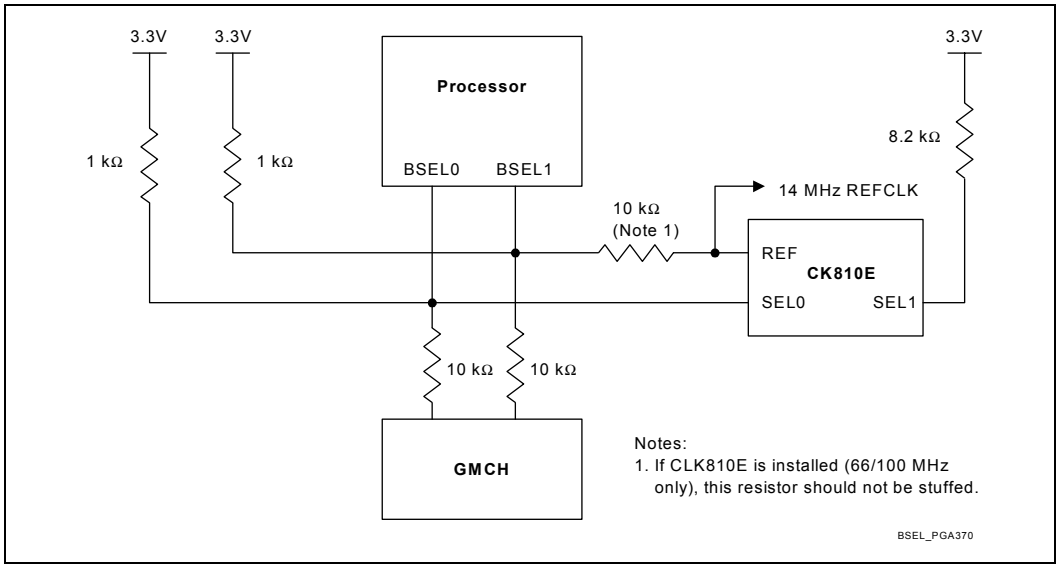
5.5 BSEL[1:0] Implementation Differences

Future 0.13 micron socket 370 processors will select the 133 MHz system bus frequency setting from the clock synthesizer. A Pentium III processor (CPUID=068xh) utilizes the BSEL1 pin to select either the 100 MHz or 133 MHz system bus frequency setting from the clock synthesizer. A Celeron processor (CPUID=068xh) uses both BSEL pins to select 66 MHz system bus frequency from the clock synthesizer. Processors in a FC-PGA or a FC-PGA2 are 3.3 V tolerant for these signals, as are the clock and chipset.

CK810E has been designed to support selections of 66 MHz, 100 MHz, and 133 MHz. The REF input pin has been redefined to be a frequency selection strap (BSEL1) during power-on and then becomes a 14 MHz reference clock output. Figure 22 shows the new BSEL[1:0] circuit design for *universal PGA370* designs. Note that BSEL[1:0] now are pulled up using 1 kΩ resistors. Also refer to Figure 23 for more details.

Note: In a design supporting future 0.13 micron socket 370 processors, the BSEL[1:0] lines are not valid until VTTPWRGD is asserted. Refer to Section 4.2.10 for full details.

Figure 22. BSEL[1:0] Circuit Implementation for PGA370 Designs



5.6 CLKREF Circuit Implementation

The CLKREF input, utilized by the Pentium III processor (CPUID=068xh) / Celeron processor (CPUID=068xh) and future 0.13 micron socket 370 processors, require a 1.25V source. It can be generated from a voltage divider on the VCC2.5 or VCC3.3 sources utilizing 1% tolerant resistors. A 4.7 µF decoupling capacitor should be included on this input. See Figure 23 and Table 11 for example CLKREF circuits.

Note: Do not use VTT as the source for this reference!

Figure 23. Examples for CLKREF Divider Circuit

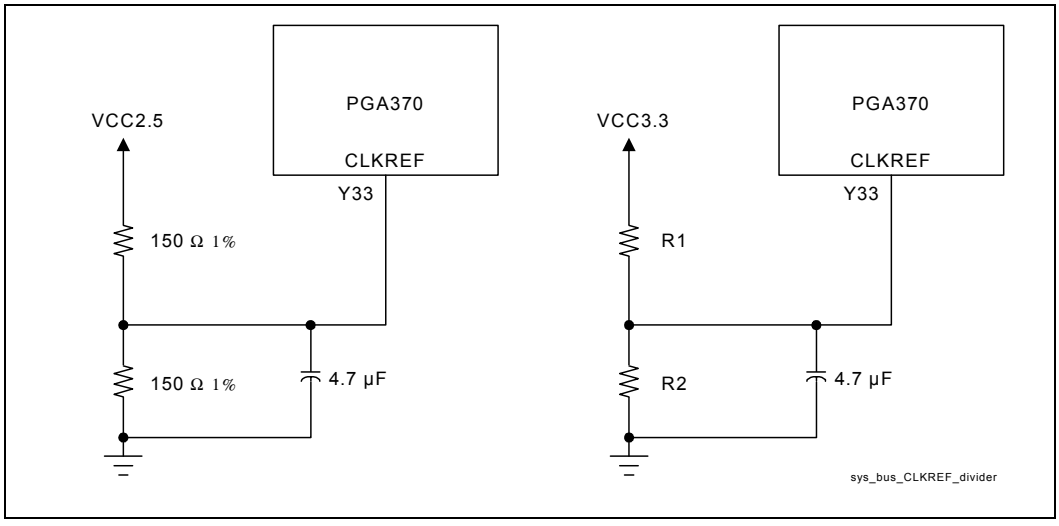


Table 11. Resistor Values for CLKREF Divider (3.3 V Source)

R1 (Ω), 1%	R2 (Ω), 1%	CLKREF Voltage (V)
182	110	1.243
301	182	1.243
374	221	1.226
499	301	1.242

5.7 Undershoot/Overshoot Requirements

Undershoot and overshoot specifications become more critical as the process technology for microprocessors shrinks due to thinner gate oxide. Violating these undershoot and overshoot limits will degrade the life expectancy of the processor.

The Pentium III processor (CPUID=068xh) / Celeron processor (CPUID=068xh) and future 0.13 micron socket 370 processors have more restrictive overshoot and undershoot requirements for system bus signals than previous processors. These requirements stipulate that a signal at the output of the driver buffer and at the input of the receiver buffer must not exceed the maximum absolute overshoot voltage limit or the minimum absolute undershoot voltage limit. Exceeding either of these limits will damage the processor. There is also a time-dependent, non-linear overshoot and undershoot requirement that depends on the amplitude and duration of the overshoot/undershoot. See the appropriate processor's electrical, mechanical and thermal specification for more details on the processor overshoot/undershoot specifications.

5.8 Processor Reset Requirements

Universal PGA370 designs must route the AGTL/AGTL+ reset signal from the chipset to two pins on the processor as well as to the debug port connector. This reset signal is connected to the following pins at the PGA370 socket:

- **AH4 (RESET#).** The reset signal is connected to this pin for the Pentium III processor (CPUID=068xh), Celeron processor (CPUID=068xh), and future 0.13 micron socket 370 processors
- **X4 (Reset2# or GND, depending on processor).** The X4 pin is RESET2# for Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh). X4 is GND for future 0.13 micron socket 370 processors. An additional 1kΩ resistor is connected in series with pin X4 to the reset circuitry since pin X4 is a ground pin in future 0.13 micron socket 370 processors.

Note: The AGTL/AGTL+ reset signal must always terminate to VTT on the motherboard.

Designs that do not support the debug port will not utilize the 240 Ω series resistor or the connection of RESET# to the debug port connector. RESET2# is not required for platforms that do not support the Celeron processor (CPUID=068xh). Pin X4 should then be connected to ground.

The routing rules for the AGTL/AGTL+ reset signal are shown in Figure 24.

Figure 24. RESET#/RESET2# Routing Guidelines

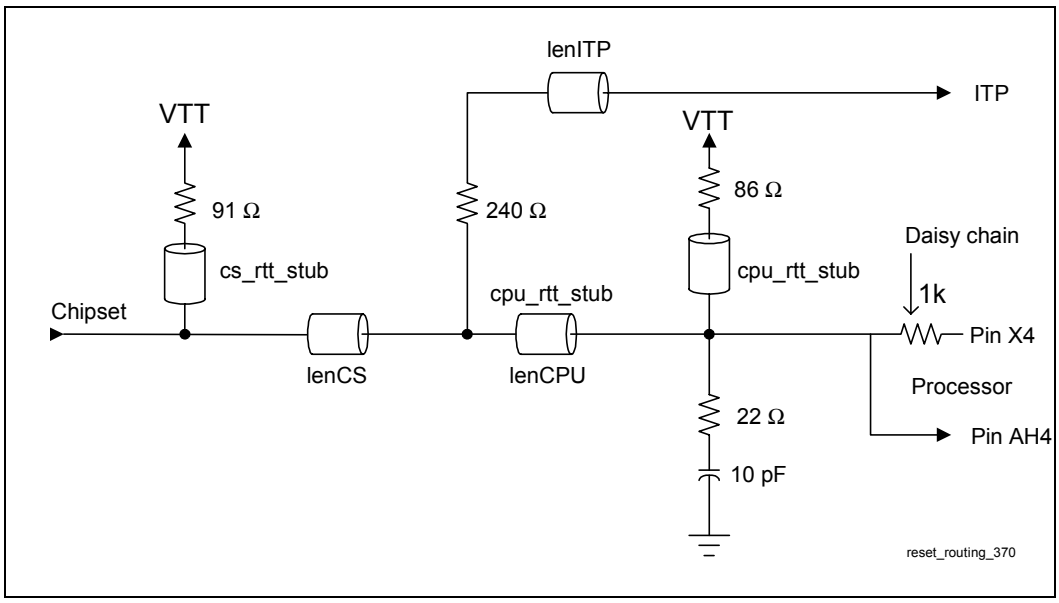


Table 12. RESET#/RESET2# Routing Guidelines (see Figure 24)

Parameter	Minimum (in)	Maximum (in)
LenCS	0.5	1.5
LenITP	1	3
LenCPU	0.5	1.5
cs_rtt_stub	0.5	1.5
cpu_rtt_stub	0.5	1.5

5.9 Processor PLL Filter Recommendations

Intel PGA370 processors have internal phase lock loop (PLL) clock generators that are analog and require quiet power supplies to minimize jitter.

5.9.1 Topology

The general desired topology for these PLLs is shown in Figure 26. Not shown are the parasitic routing and local decoupling capacitors. Excluded from the external circuitry are parasitics associated with each component.

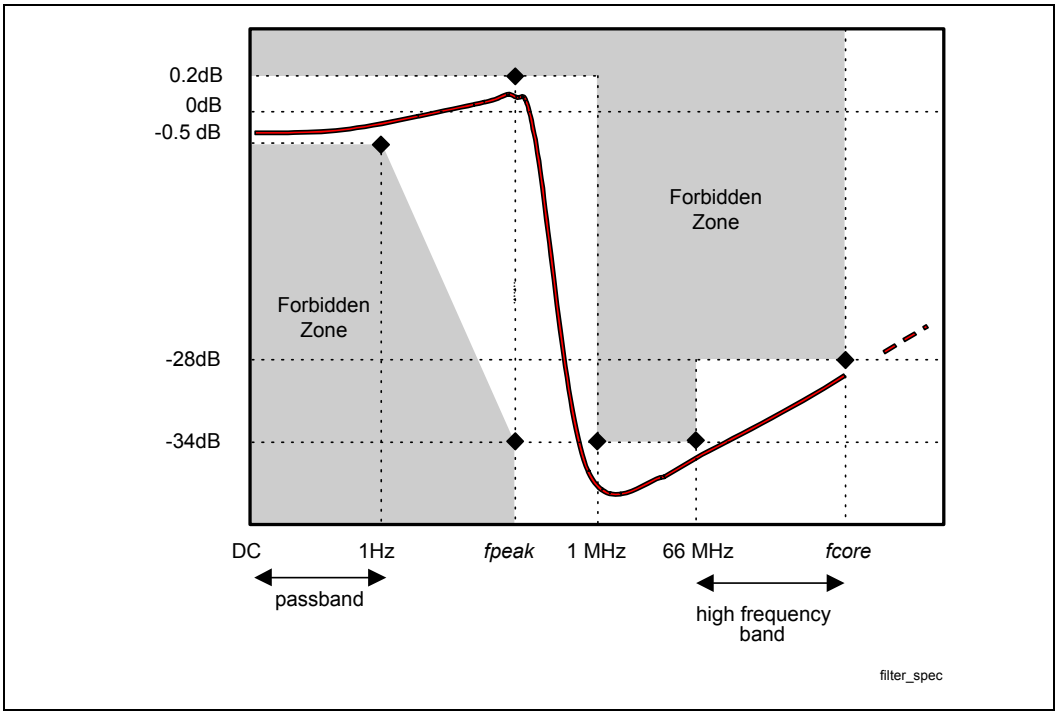
5.9.2 Filter Specification

The function of the filter is to protect the PLL from external noise through low-pass attenuation. The low-pass specification, with input at VCC_{CORE} and output measured across the capacitor, is as follows:

- < 0.2 dB gain in pass band
- < 0.5 dB attenuation in pass band (see DC drop in next set of requirements)
- > 34 dB attenuation from 1 MHz to 66 MHz
- > 28 dB attenuation from 66 MHz to core frequency

The filter specification is graphically shown in Figure 25.

Figure 25. Filter Specification



NOTES:
1. Diagram not to scale.
2. No specification for frequencies beyond *fcore*.
3. *fpeak* should be less than 0.05 MHz.

Other requirements:

- Use shielded-type inductor to minimize magnetic pickup.
- Filter should support DC current > 30 mA.
- DC voltage drop from VCC to PLL1 should be < 60 mV, which in practice implies series R < 2 Ω. This also means pass-band (from DC to 1 Hz) attenuation < 0.5 dB for VCC = 1.1 V, and < 0.35 dB for VCC = 1.5 V.

5.9.3 Recommendation for Intel® Platforms

The following tables contain examples of components that meet Intel's recommendations, when configured in the topology of Figure 26.

Table 13. Component Recommendations – Inductor

Part Number	Value	Tol.	SRF	Rated I	DCR (Typical)
TDK MLF2012A4R7KT	4.7 µH	10%	35 MHz	30 mA	0.56 Ω (1 Ω max.)
Murata LQG21N4R7K00T1	4.7 µH	10%	47 MHz	30 mA	0.7 Ω (± 50%)
Murata LQG21C4R7N00	4.7 µH	30%	35 MHz	30 mA	0.3 Ω max.

Table 14. Component Recommendations – Capacitor

Part Number	Value	Tolerance	ESL	ESR
Kemet T495D336M016AS	33 µF	20%	2.5 nH	0.225 Ω
AVX TPSD336M020S0200	33 µF	20%	2.5 nH	0.2 Ω

Table 15. Component Recommendation – Resistor

Value	Tolerance	Power	Note
1 Ω	10%	1/16 W	Resistor may be implemented with trace resistance, in which case a discrete R is not needed. See Figure 27.

To satisfy damping requirements, total series resistance in the filter (from VCC_{CORE} to the top plate of the capacitor) must be at least 0.35 Ω. This resistor can be in the form of a discrete component or routing or both. For example, if the chosen inductor has minimum DCR of 0.25 Ω, then a routing resistance of at least 0.10 Ω is required. Be careful not to exceed the maximum resistance rule (2 Ω). For example, if using discrete R1 (1 Ω ± 1%), the maximum DCR of the L (trace plus inductor) should be less than 2.0 - 1.1 = 0.9 Ω, which precludes the use of some inductors and sets a max. trace length.

Other routing requirements:

- The capacitor (C) should be close to the PLL1 and PLL2 pins, < 0.1 Ω per route. These routes do not count towards the minimum damping R requirement.
- The PLL2 route should be parallel and next to the PLL1 route (i.e., minimize loop area).
- The inductor (L) should be close to C. Any routing resistance should be inserted between VCC_{CORE} and L.
- Any discrete resistor (R) should be inserted between VCC_{CORE} and L.

Figure 26. Example PLL Filter Using a Discrete Resistor

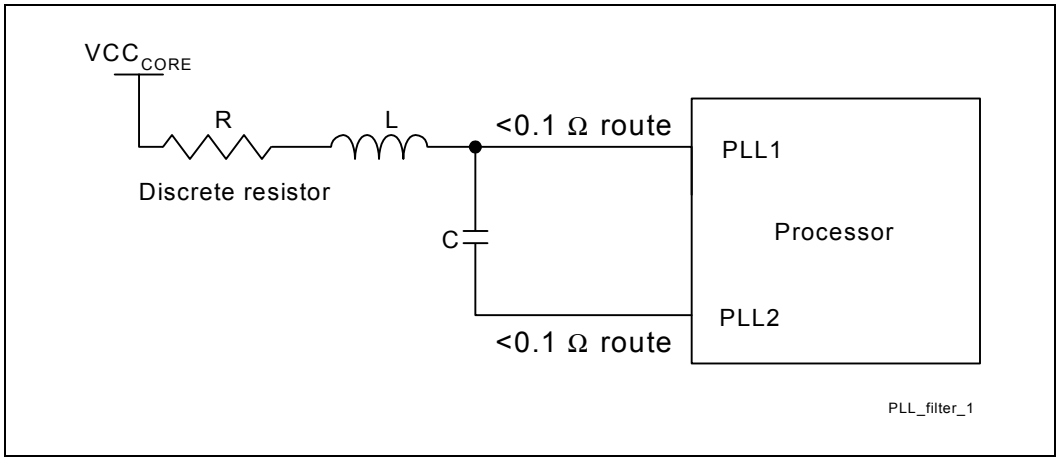
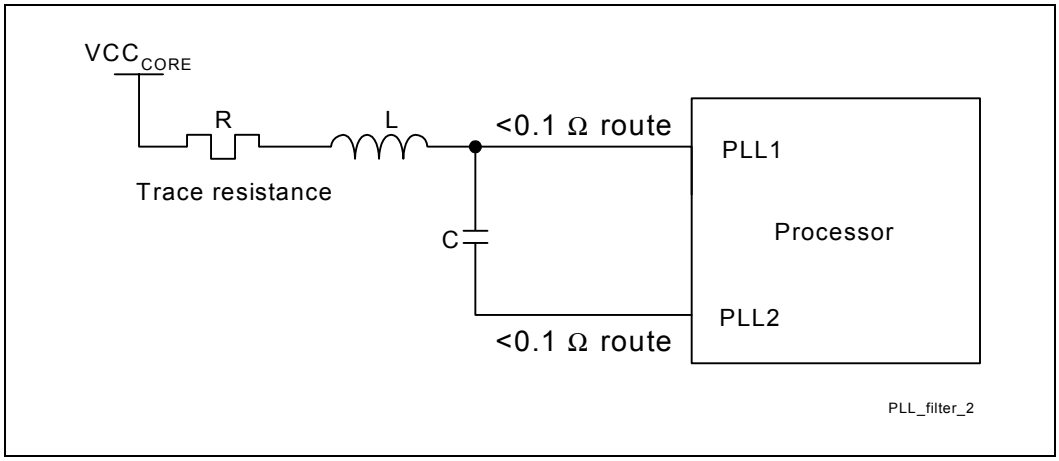


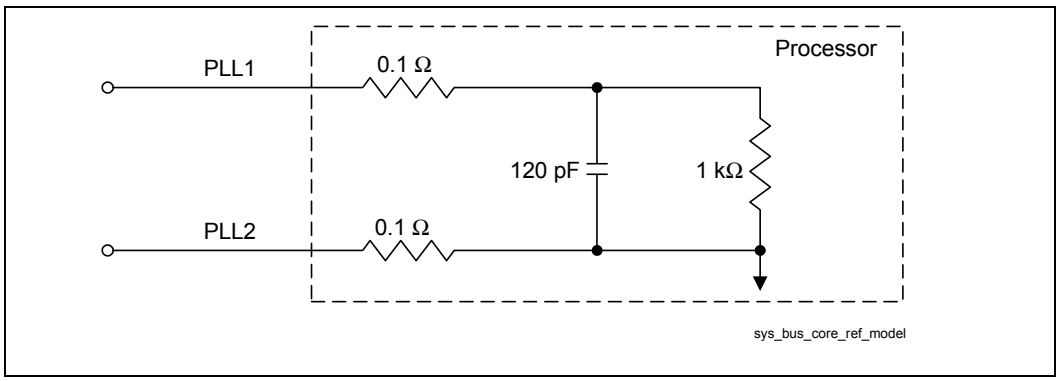
Figure 27. Example PLL Filter Using a Buried Resistor



5.9.4 Custom Solutions

As long as designers satisfy filter performance and requirements as specified and outlined in Section 5.9.2, other solutions are acceptable. Custom solutions should be simulated against a standard reference core model, which is shown in Figure 28.

Figure 28. Core Reference Model



NOTES:
1. 0.1 Ω resistors represent package routing.
2. 120 pF capacitor represents internal decoupling capacitor.
3. 1 kΩ resistor represents small signal PLL resistance.
4. Be sure to include all component and routing parasitics.
5. Sweep across component/parasitic tolerances.
6. To observe IR drop, use DC current of 30 mA and minimum VCC_{CORE} level.
7. For other modules (interposer, DMM, etc.), adjust routing resistor if desired, but use minimum numbers.

5.10 Voltage Regulation Guidelines

A *universal PGA370* design will need the voltage regulation module (VRM) or on-board voltage regulator (VR) to be compliant with Intel *VRM 8.5 DC-DC Converter Design Guidelines*.

5.11 Decoupling Guidelines for Universal PGA370 Designs

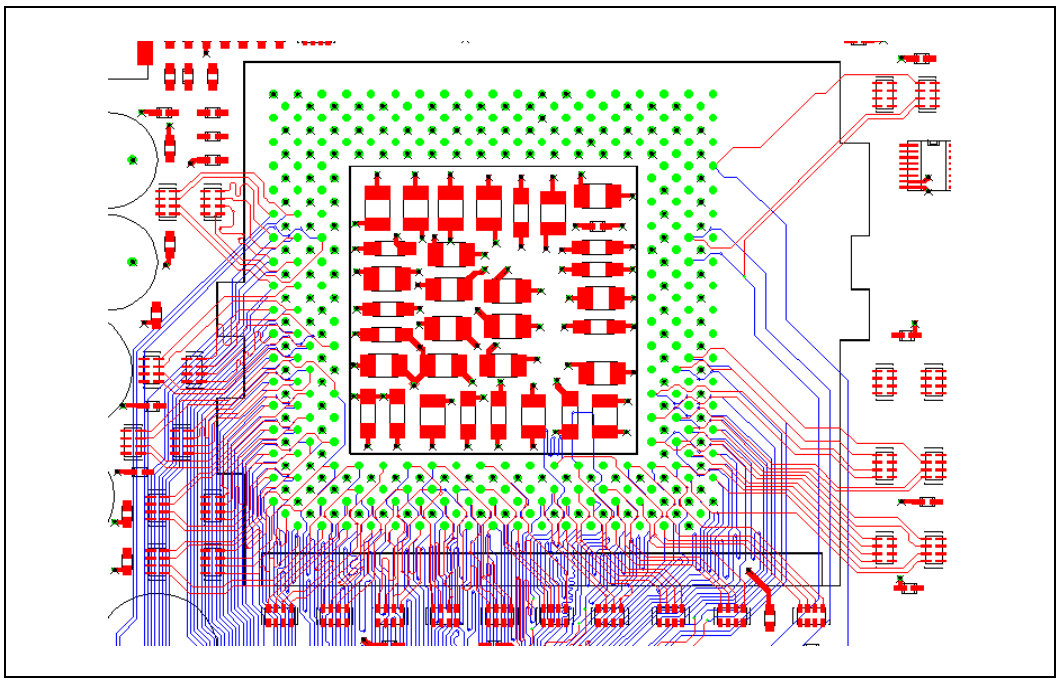
These preliminary decoupling guidelines for *universal PGA370* designs are estimated to meet the specifications of *VRM 8.5 DC-DC Converter Design Guidelines*.

5.11.1 VCC_{CORE} Decoupling Design

- Sixteen or more 4.7 µF capacitors in 1206 packages.

All capacitors should be placed within the PGA370 socket cavity and mounted on the primary side of the motherboard. The capacitors are arranged to minimize the overall inductance between the VCC_{CORE}/VSS power pins, as shown in Figure 29.

Figure 29. Capacitor Placement on the Motherboard



5.11.2 VTT Decoupling Design

For Itt = 2.3 A (max.)

- 20 0.1 µF capacitors in 0603 packages placed as closed as possible to the processor VTT pins. The capacitors are shown on the exterior of Figure 29.

5.11.3 V_{REF} Decoupling Design

- Four 0.1 µF capacitors in 0603 package placed near V_{REF} pins (within 500 mils).

5.12 Thermal Considerations

5.12.1 Heat Sink Volumetric Keep-Out Regions

Current heat sink recommendations are only valid for supported Celeron and Pentium III processor frequencies.

Figure 30 shows the system component keep-out volume above the socket connector required for the reference design thermal solution for high frequency processors. This keep-out envelope provides adequate room for the heat sink, fan and attach hardware under static conditions as well as room for installation of these components on the socket. The heatsink must be compatible with the Integrated Heat Spreader (IHS) used by higher frequency Pentium III processors.

Figure 31 shows component keep-outs on the motherboard required to prevent interference with the reference design thermal solution. Note portions of the heat sink and attach hardware hang over the motherboard.

Adhering to these keep-out areas will ensure compatibility with Intel boxed processor products and Intel-enabled third-party vendor thermal solutions for high frequency processors. While the keep-out requirements should provide adequate space for the reference design thermal solution, systems integrators should check with their vendors to ensure their specific thermal solutions fit within their specific system designs. Ensure that the thermal solutions under analysis comprehend the specific thermal design requirements for higher frequency Pentium III processors.

While thermal solutions for lower frequency processors may not require the full keep-out area, larger thermal solutions will be required for higher frequency processors, and failure to adhere to the guidelines will result in mechanical interference.

Figure 30. Heatsink Volumetric Keep-Out Regions

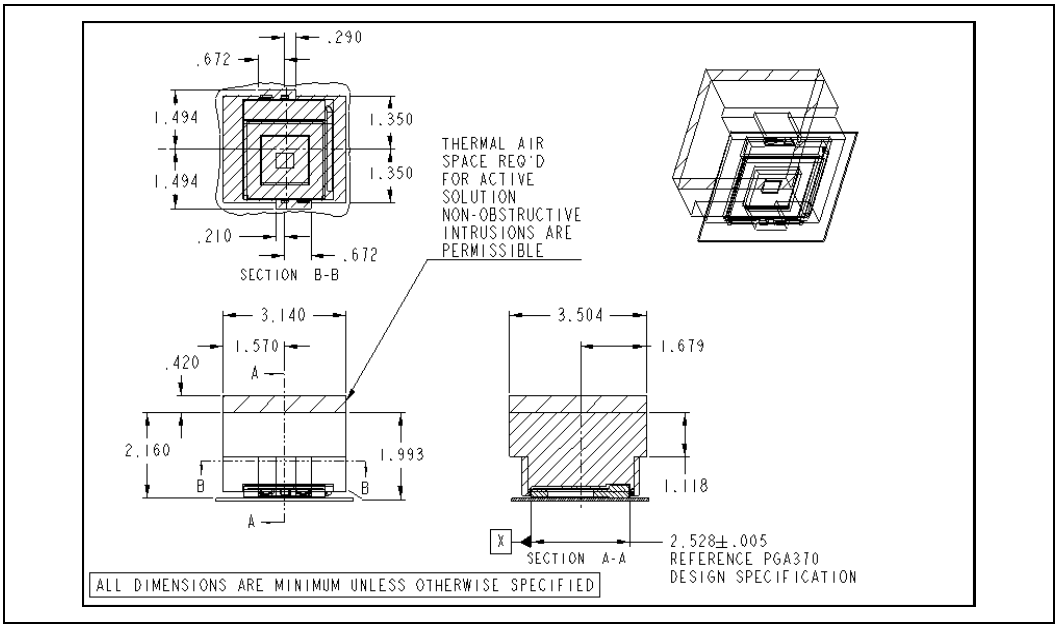
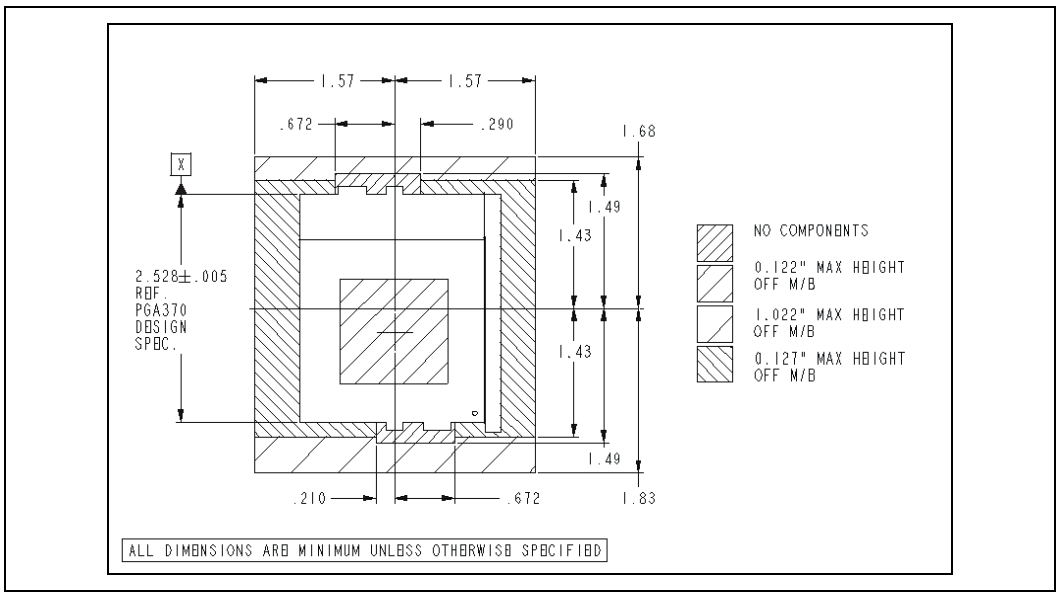


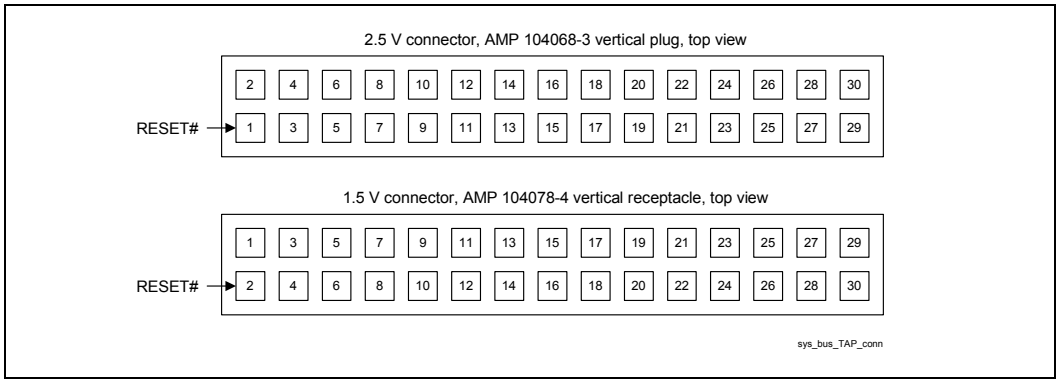
Figure 31. Motherboard Component Keep-Out Regions



5.13 Debug Port Changes

Due to the lower voltage technology employed with newer processors, changes are required to support the debug port. Previously, test access port (TAP) signals used 2.5 V logic, as is the case with the Celeron processor in the PPGA package. Pentium III processor (CPUID=068xh) / Celeron processor (CPUID=068xh) and future 0.13 micron socket 370 processors utilize 1.5 V logic levels on the TAP. As a result, the type of debug port connecter used in *universal PGA370* designs is dependent on the processor that is currently in the socket. The 1.5 V connector is a mirror image of the older 2.5 V connector. Either connector will fit into the same printed circuit board layout. Only the pin numbers would change (see Figure 32). Also required, along with the new connector, is an In-Target Probe* (ITP) that is capable of communicating with the TAP at the appropriate logic levels.

Figure 32. TAP Connector Comparison



Caution: Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh) require an in-target probe (ITP) compatible with 1.5 V signal levels on the TAP. Previous ITPs were designed to work with higher voltages and may damage the processor if connected to any of these specified processors.

See the processor datasheet for more information regarding the debug port.

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6 Layout and Routing Guidelines

This chapter describes motherboard layout and routing guidelines for 810E chipset systems, except for the processor layout guidelines. For the PGA370 processor specific layout guidelines, refer to Chapter 2. This chapter does not discuss the functional aspects of any bus or the layout guidelines for an add-in device.

Note: If the guidelines listed in this document are not followed, it is very important that thorough signal integrity and timing simulations are completed for each design. Even when the guidelines are followed, critical signals are recommended to be simulated to ensure proper signal integrity and flight time. Any deviation from these guidelines Should be simulated.

6.1 General Recommendations

The trace impedance typically noted (i.e., 60 Ω ±15%) is the "nominal" trace impedance for a 5 mil wide trace (i.e., the impedance of the trace when not subjected to the fields created by changing current in neighboring traces). When calculating flight times, it is important to consider the minimum and maximum impedance of a trace based on the switching of neighboring traces. Using wider spaces between the traces can minimize this trace-to-trace coupling. In addition, these wider spaces reduce settling time.

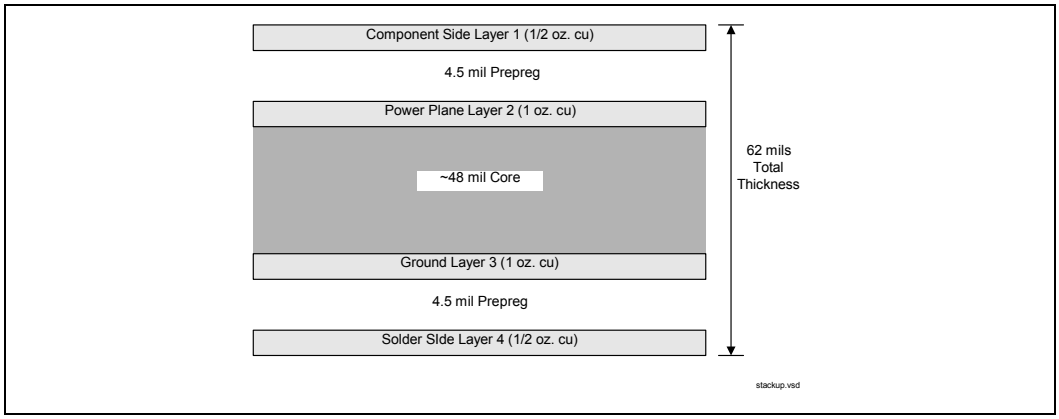
Coupling between two traces is a function of the coupled length, the distance separating the traces, the signal edge rate, and the degree of mutual capacitance and inductance. To minimize the effects of trace-to-trace coupling, the routing guidelines documented in this section should be followed.

Additionally, these routing guidelines are created using the *stack-up* (refer to the following Figure 33). If this stack-up is not used, simulations should be completed.

6.2 Nominal Board Stack-Up

The 810E chipset platform requires a board stack-up yielding a target impedance of 60 Ω ±15% with a 5 mil nominal trace width. The following Figure 33 presents an example stack-up to achieve this. It is a 4-layer fabrication construction using 53% resin, FR4 material.

Figure 33. Nominal Board Stack-Up



6.3 Component Quadrant Layouts

Figure 34. GMCH Quadrant Layout (topview)

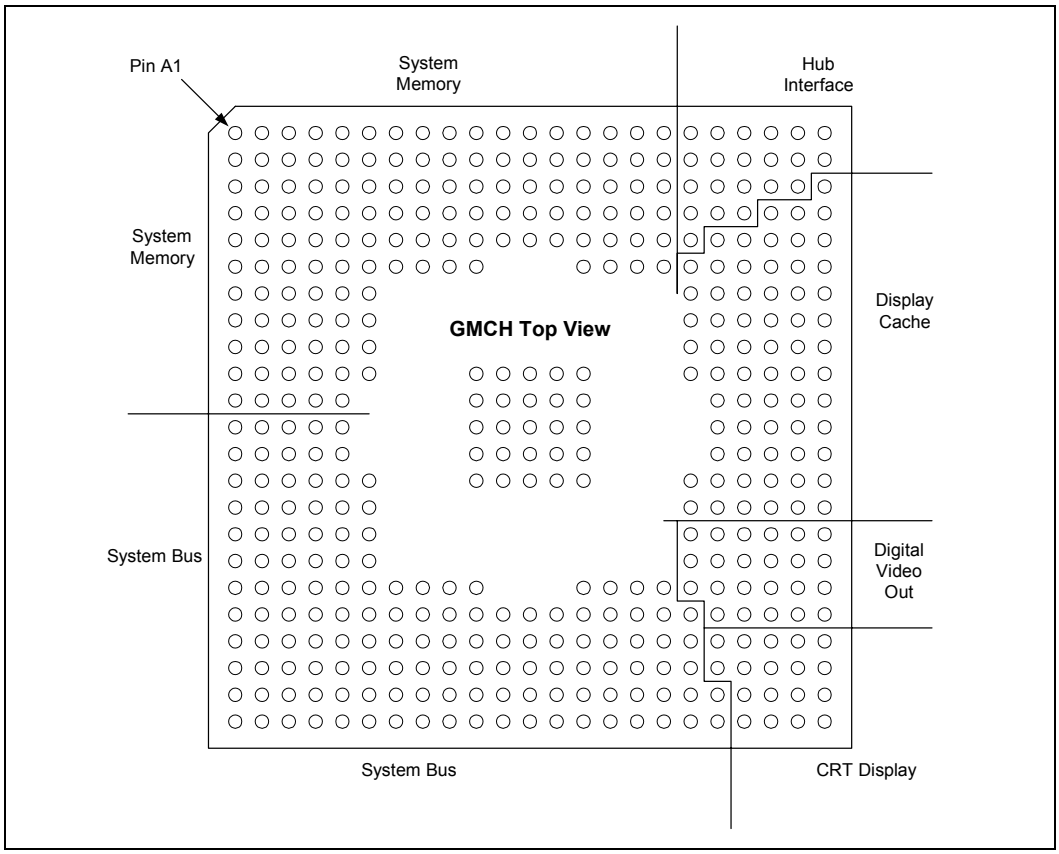
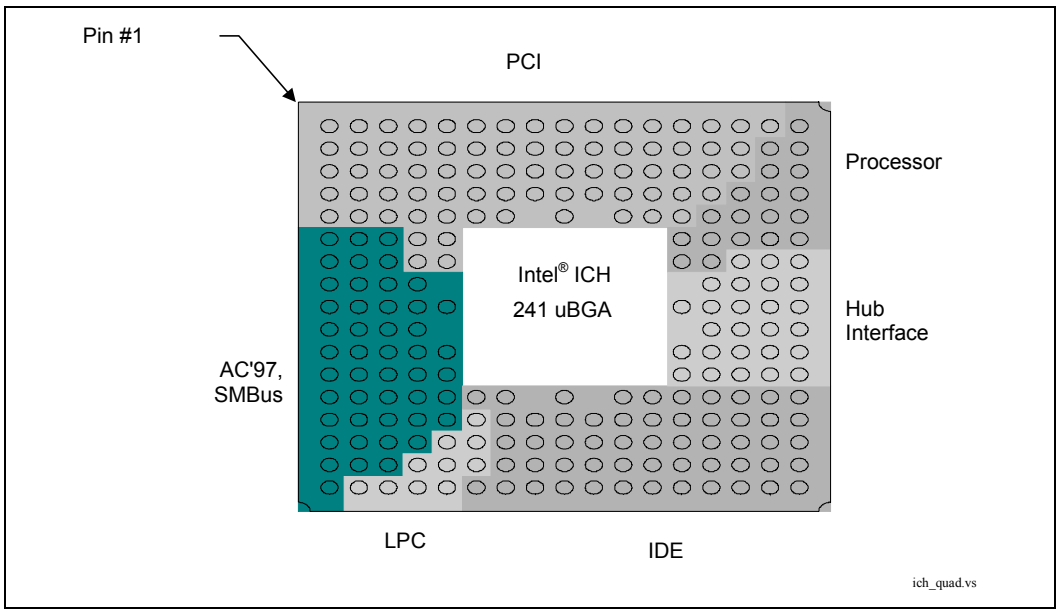


Figure 35. ICH 241-uBGA Quadrant Layout (top view)

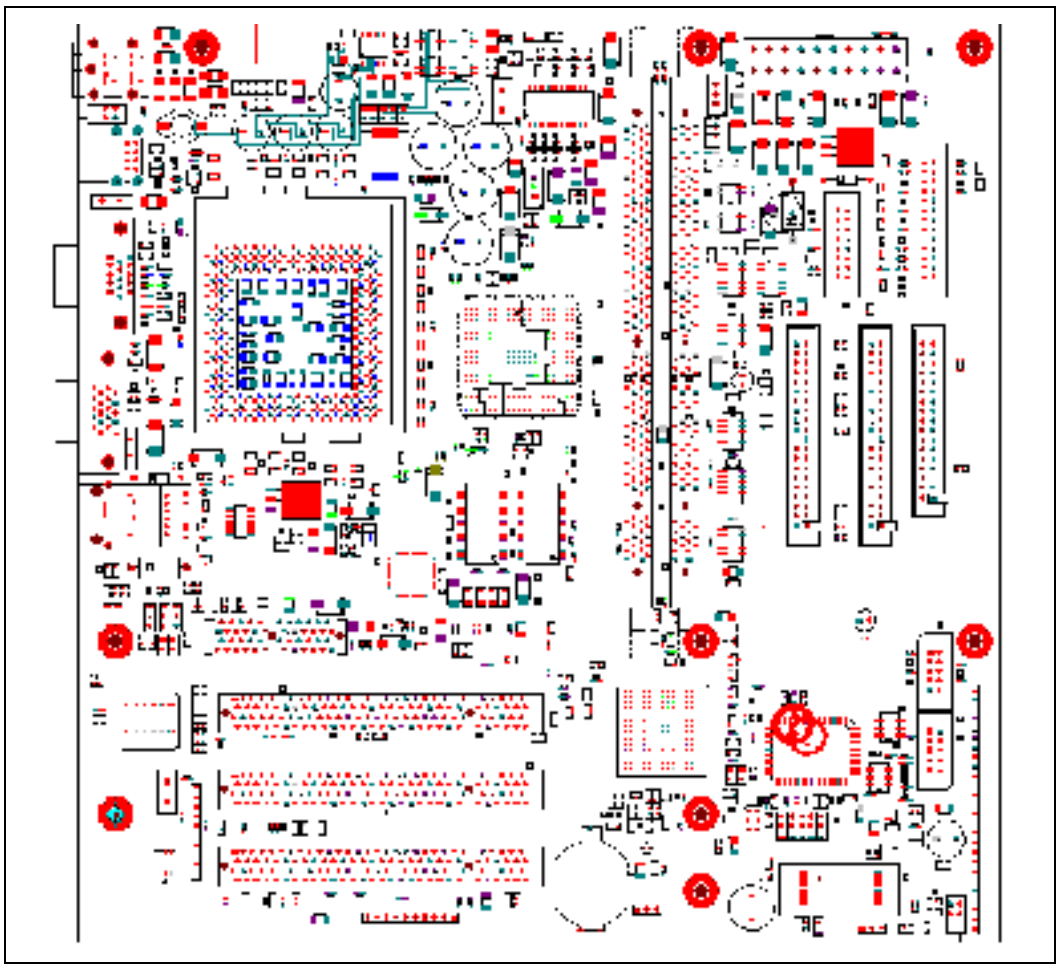


6.4 Intel® 810E Chipset Component Placement

The assumptions for component placement are:

- µATX Form Factor
- 4-Layer Motherboard
- Single Sided Assembly

Figure 36. µATX Placement Example for PGA370 Processors



6.5 System Memory Layout Guidelines

6.5.1 System Memory Solution Space

Figure 37. System Memory Topologies

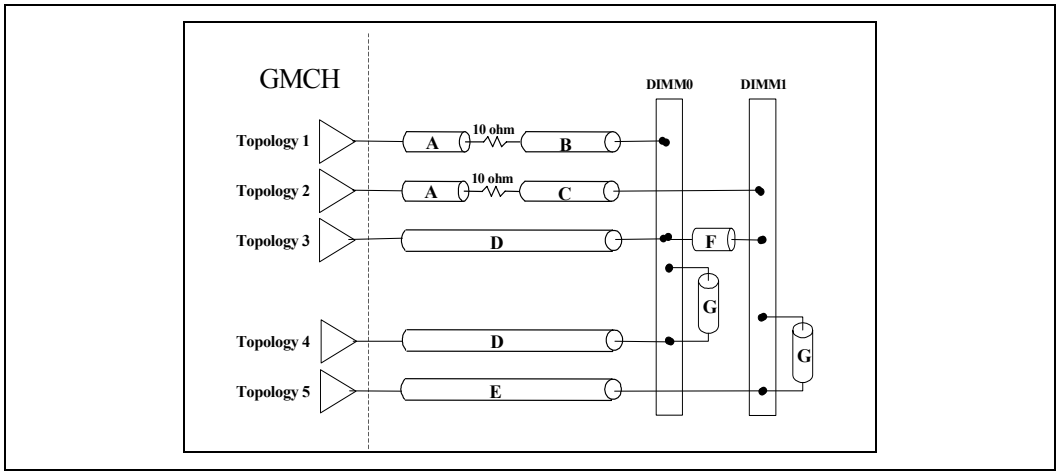


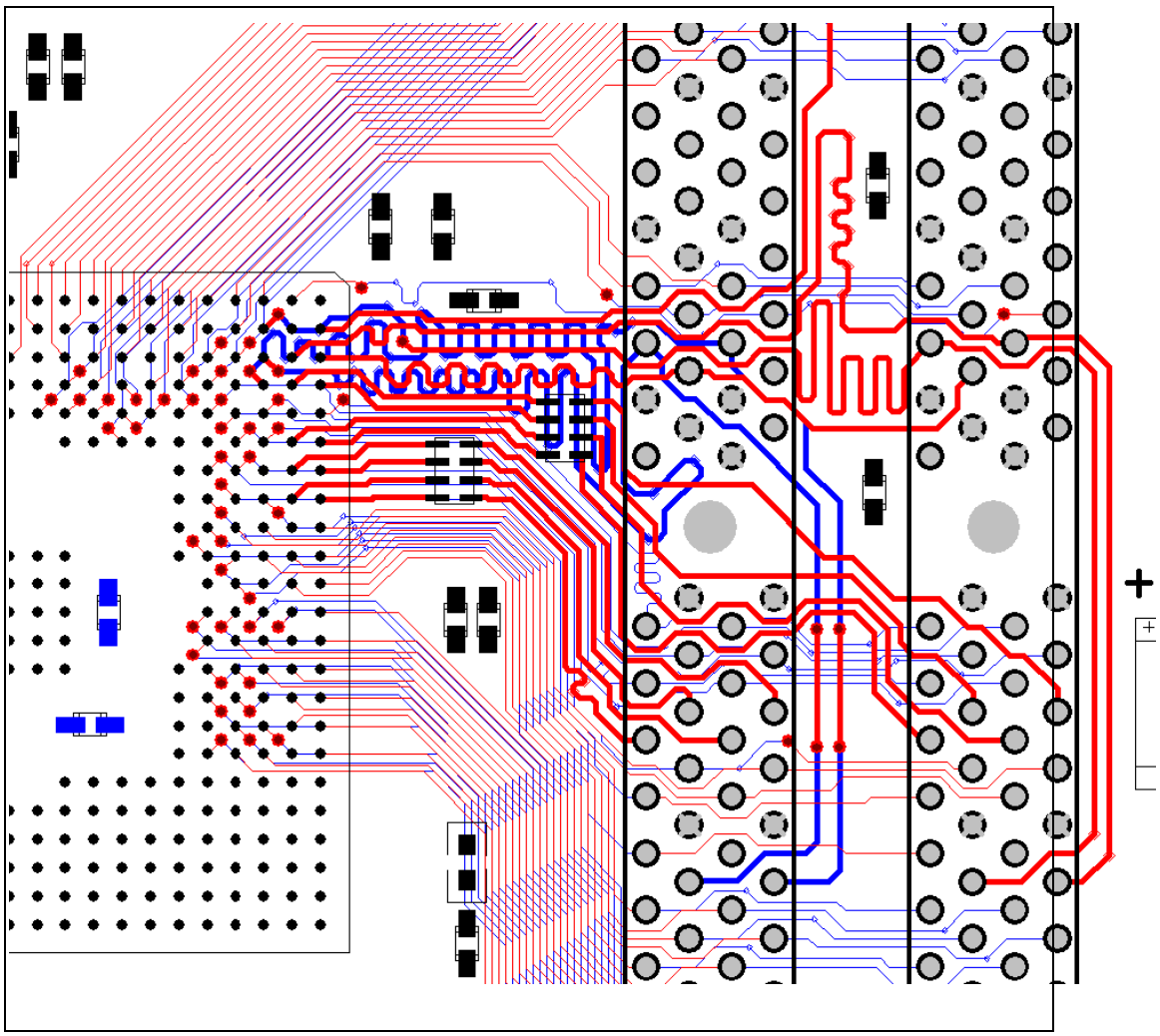
Table 16. System Memory Routing

Signal		Top.	Trace (mils)		Trace Lengths (inches)													
					A	B		C		D		E		F		G	
			Width	Space	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
SCS[3:2]#	Opt.1	5	10	8								3	5			1.5	2
	Opt.2	5	10	8								2.2	5			1.5	1.8
	Opt.3	5	10	8								1.6	5			1.15	1.5
SCS[1:0]#	Opt.1	4	10	8						3	5					1.5	2
	Opt.2	4	10	8						2.2	5					1.5	1.8
	Opt.3	4	10	8						1.6	5					1.15	1.5
SMAA[7:4]		1	10	8	0.5	0.5	2										
SMAB[7:4]#		2	10	8	0.5			0.5	2								
SCKE[1:0]		3	10	8						1	2.5			0.4	1		
SMD[63:0], SDQM[7:0]		3	5	7						1	3			0.4	1		
SCAS#, SRAS#, SWE#		3	5	7						1	3.5			0.4	1		
SBS[1:0], SMAA[11:8, 3:0]		3	5	7						1	2.5			0.4	1		

NOTES: It is recommended to add 10 Ω series resistors to the MAA[7:4] and the MAB[7:4] lines as close as possible to GMCH for signal integrity.

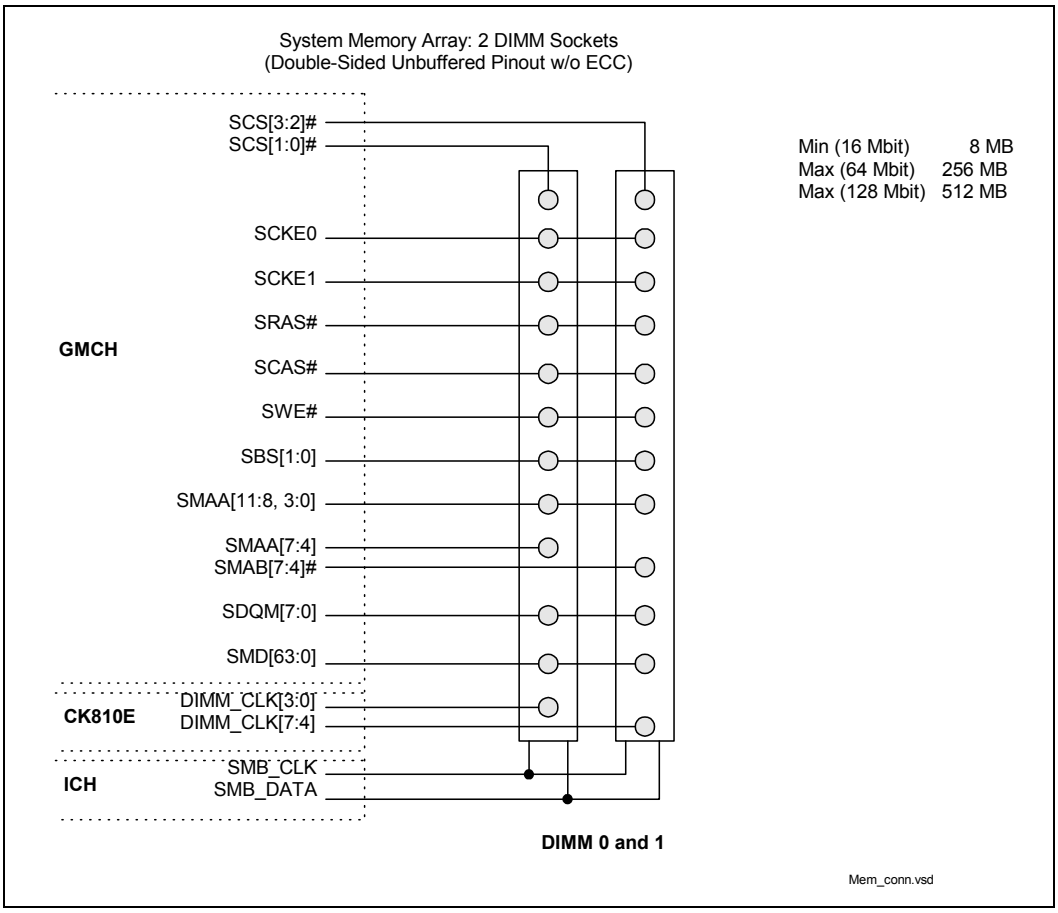
6.5.2 System Memory Routing Example

Figure 38. System Memory Routing Example



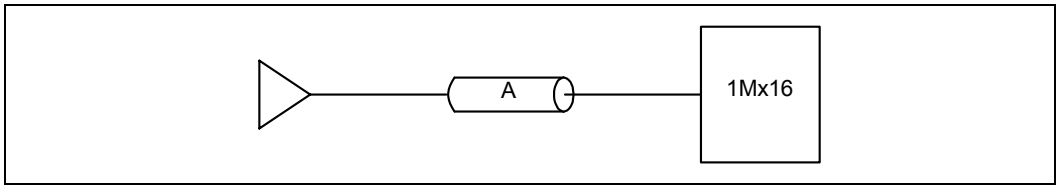
6.5.3 System Memory Connectivity

Figure 39. System Memory Connectivity



6.6 Display Cache Interface

Figure 40. Display Cache (Topology 1)



6.6.1 Display Cache Solution Space

Table 17. Display Cache Routing (Topology 1)

Signal	Topology	Trace (mils)		A (inches)	
		Width	Spacing	Min	Max
LMD[31:0], LDQM[3:0]	1	5	7	1	5

NOTES:
1. Trace Length (inches)

Figure 41. Display Cache (Topology 2)

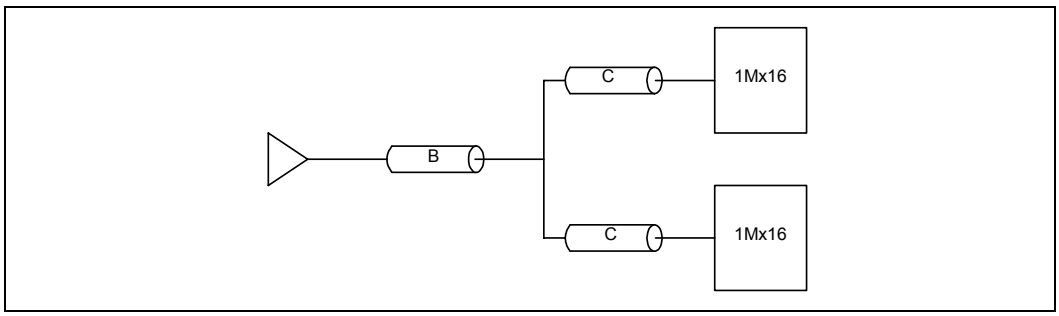


Table 18. Display Cache Routing (Topology 2)

Signal	Topology	Trace (units=mils)		B (inches)		C (inches)	
		Width	Spacing	Min	Max	Min	Max
LMA[11:0], LWE#, LCS#, LRAS#, LCAS#	2	5	7	1	3.75	0.75	1.25

Figure 42. Display Cache (Topology 3)

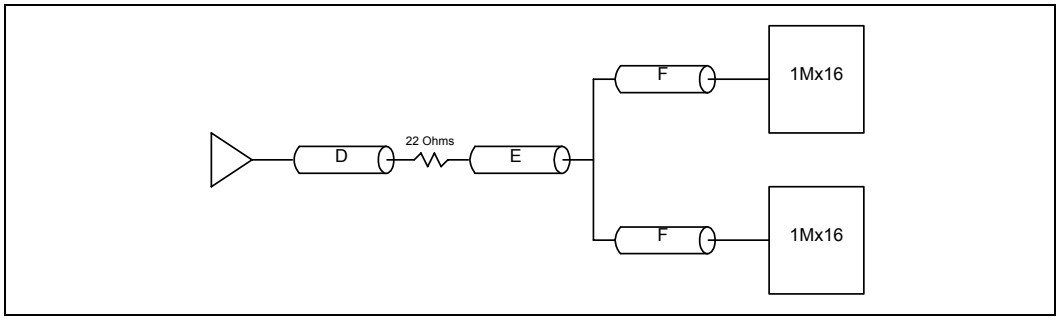


Table 19. Display Cache Routing (Topology 3)

Signal	Topology	Trace (units=mils)		D (inches)	E (inches)		F (inches)	
		Width	Spacing	Length	Min	Max	Min	Max
TCLK	3	5	7	0.5	1.5	2.5	0.75	1.25

Figure 43. Display Cache (Topology 4)

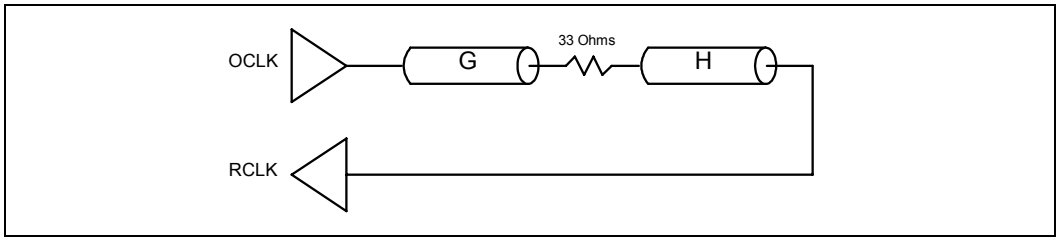


Table 20. Display Cache Routing (Topology 4)

Signal	Topology	Trace (units=mils)		G (inches)	H (inches)	
		Width	Spacing	Length	Min	Max
OCLK	4	5	6	0.5	3.25	3.75

6.7 Hub Interface

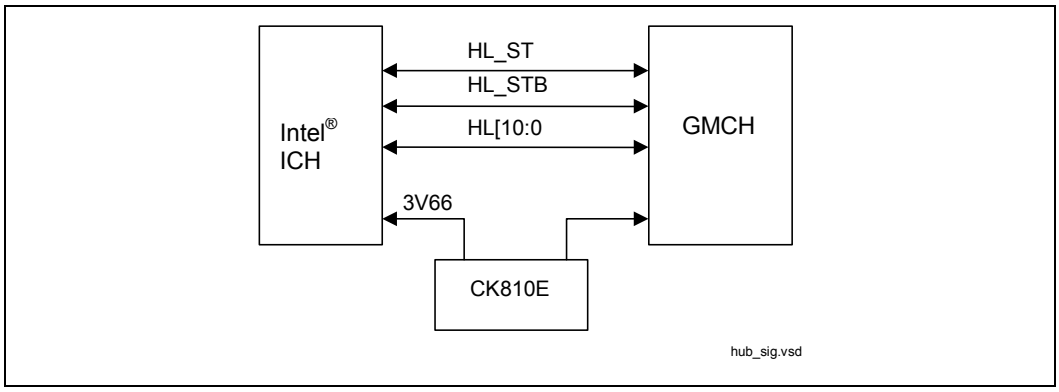
The GMCH ball assignment and ICH ball assignment have been optimized to simplify hub interface routing. It is recommended that the hub interface signals are routed directly from the GMCH to the ICH on the top signal layer (refer to the following Figure 44). The hub interface has two signal groups:

- Data Signals: HL[10:0]
- Strobe Signals: HL_STB, HL_STB# (differential strobe pair).

There are no pull-ups or pull-downs required on the hub interface. HL11 can be brought out to a test point for NAND Tree testing.

Each signal should be routed such that the signal meets the guidelines documented for its signal group.

Figure 44. Hub Interface Signal Routing Example



6.7.1 Data Signals

Hub interface data signals should be routed with a trace width of *5* mils and a trace spacing of *20* mils. These signals can be routed with a trace width of *5* mils and a trace spacing of *15* mils for navigation around components or mounting holes. To break-out of the GMCH and the ICH, the hub interface data signals can be routed with a trace width of *5* mils and a trace spacing of *5* mils. The signals should be separated to a trace width of *5* mils and a trace spacing of 20 mils within 0.3” of the GMCH/ICH components.

The maximum trace length for the hub interface data signals is 7”. These signals should each be matched within ±0.1” of the HL_STB and HL_STB# signals.

6.7.2 Strobe Signals

Due to their differential nature, the hub interface strobe signals should be 5 mils wide and routed 20 mils apart. This strobe pair should be a minimum of 20 mils from any adjacent signals. The maximum length for the strobe signals is 7” and the two strobes should be the same length. Additionally, the trace length for each data signal should be matched to the trace length of the strobes with ±0.1”.

6.7.3 HREF Generation/Distribution

There are two types of HREF generation. For a single hub interface circuit, the top 500 pF capacitor and 56 Ω resistor are not stuffed. The lower 56 Ω resistor is replaced with 0 Ω (short). The lower 500 pF capacitor is replaced by a 0.1 µF capacitor.

HREF is the hub interface reference voltage. It is 0.5 * 1.8V = 0.9V +/-2%. It can be generated locally, or a single HREF divider can be used (as shown in the following two Figure 45, Figure 46). The resistors in the DC element should be equal in value and rated at 1% tolerance. The value of these resistors must be chosen to ensure that the reference voltage tolerance is maintained over the entire input leakage specification. The recommended range for the resistor value is from minimum 100 Ω to maximum 1 kΩ (300 Ω is shown in the example.)

The single HREF divider should not be located more than 4" away from either the GMCH or the ICH.

The reference voltage generated by a single HREF divider should be bypassed to ground at each component with a 0.01 µF capacitor located close to the component HREF pin. If the reference voltage is generated locally, the bypass capacitor needs to be close to the component HREF pin.

Figure 45. Single Hub Interface Reference Divider Circuit

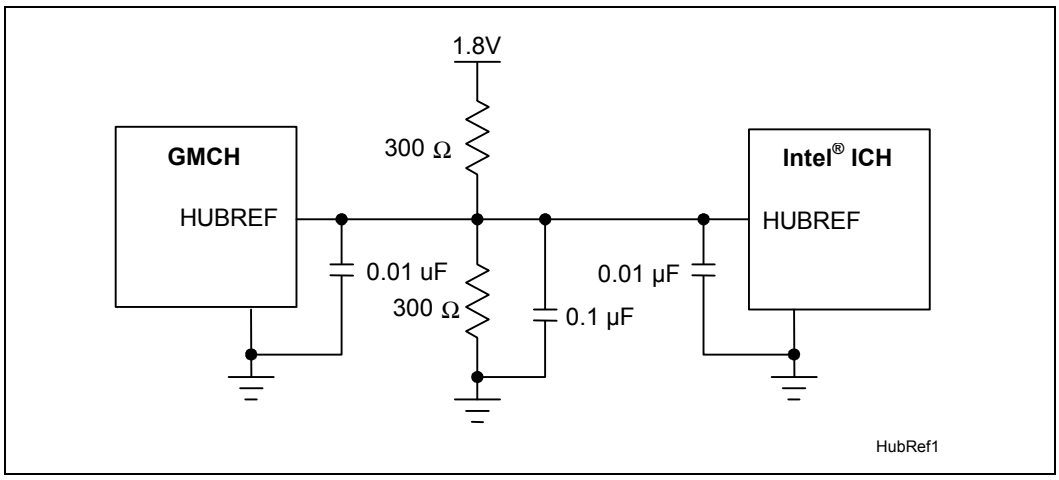
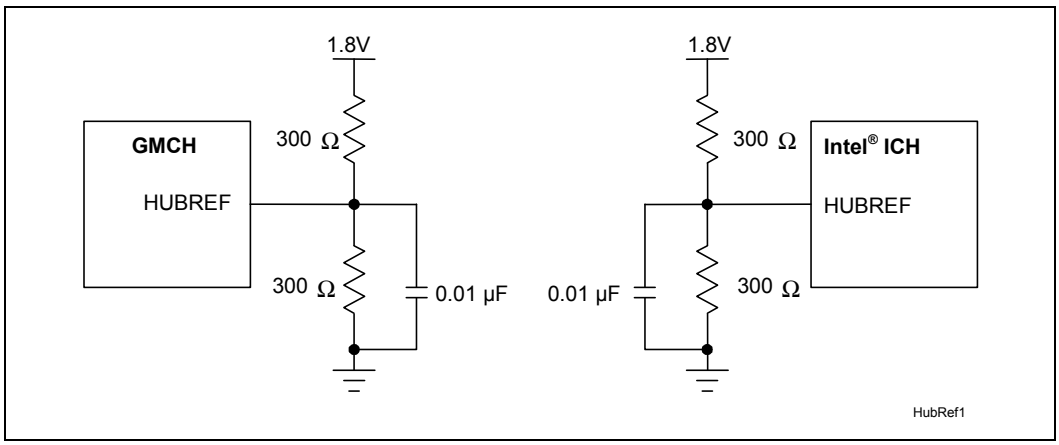


Figure 46. Locally Generated Hub Interface Reference Dividers



6.7.4 Compensation

There are two options for the ICH hub interface compensation (HLCOMP). HLCOMP is used by the ICH to adjust buffer characteristics to specific board characteristics. Refer to the *Intel® 82801AA (ICH) and Intel® 82801AB (ICH0) I/O Controller Hub* Datasheet for details on compensation. It can be used as either Impedance Compensation (ZCOMP) or Resistive Compensation (RCOMP). The guidelines are below:

- **RCOMP:** Tie the HLCOMP pin to a 40 Ω 1% or 2% pull-up resistor (to 1.8V) via a 10 mil wide, 0.5” trace (targeted for a nominal trace impedance of 40 Ω).
- **ZCOMP:** The HLCOMP pin should be tied to a 10 mil trace that is AT LEAST 18” long. This trace should be unterminated and care should be taken when routing the signal to avoid crosstalk (15-20 mil separation between this signal and any adjacent signals is recommended). This signal may not cross power plane splits.

The GMCH also has a hub interface compensation pin. This signal (HLCOMP) can be routed using either the RCOMP method or ZCOMP method described for the ICH.

6.8 Ultra ATA/66

6.8.1 IDE Routing Guidelines

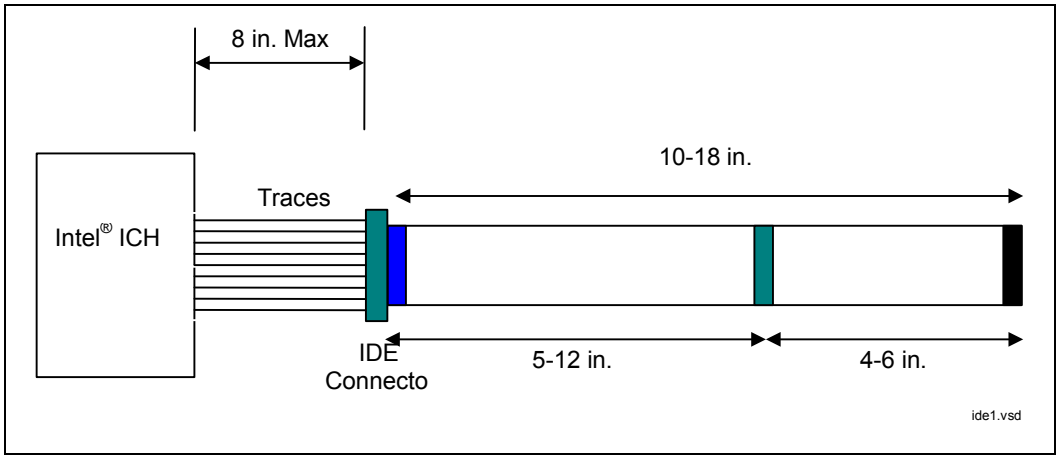
This section contains guidelines for connecting and routing the ICH IDE interface. The ICH has two independent IDE channels. This section provides guidelines for IDE connector cabling and motherboard design, including component and resistor placement, and signal termination for both IDE channels. The ICH0 and the ICH has integrated the series terminating resistors that have been typically required on the IDE data and control signals running to the two ATA connectors.

The IDE interface can be routed with 5 mil traces on 5 mil spaces and should be less than 8 inches long (from ICH to IDE connector). Additionally, the shortest IDE signal (on a given IDE channel) must be less than 1” shorter than the longest IDE signal (on the channel).

Cabling

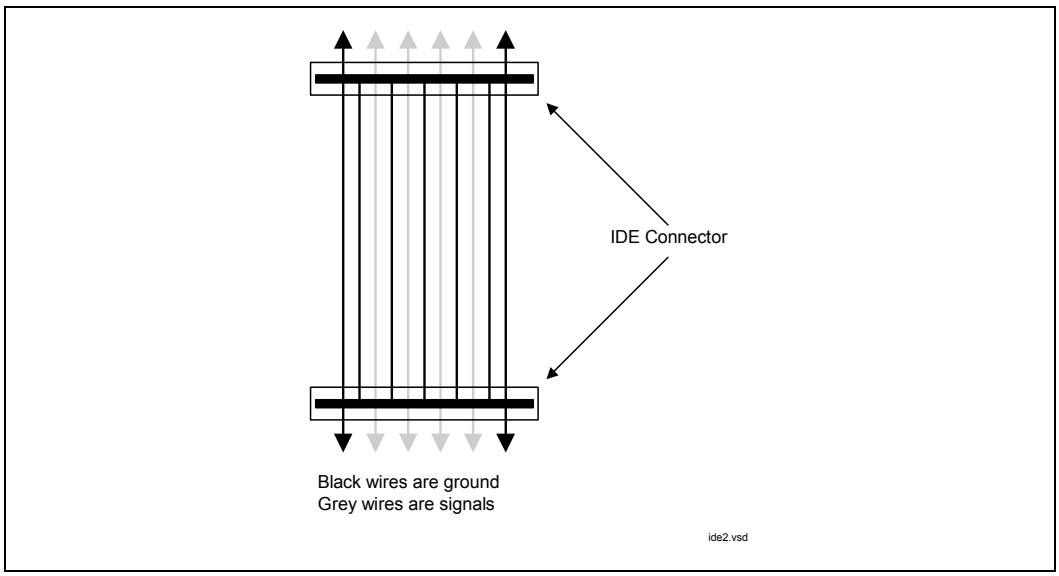
- **Length of Cable:** Each IDE cable should be equal to or less than 18 inches.
- **Capacitance:** Less than 30 pF.
- **Placement:** A maximum of 6 inches between drive connectors on the cable. If a single drive is placed on the cable it should be placed at the end of the cable. If a second drive is placed on the same cable it should be placed on the next closest connector to the end of the cable (6" away from the end of the cable).
- **Grounding:** Provide a direct low impedance chassis path between the motherboard ground and hard disk drives.
- **UltraATA/66:** Ultra ATA/66 requires the use of an 80 conductor cable
- **ICH Placement:** The ICH should be placed within 8" of the ATA connector.
- **PC99 Requirement:** Support Cable Select for master-slave configuration is a system design requirement for Microsoft* PC99. The CSEL signal needs to be pulled down at the host side by using a 470 Ω pull-down resistor for each ATA connector.

Figure 47. IDE Min/Max Routing and Cable Lengths



A new IDE cable is required for Ultra ATA/66. This cable is an 80 conductor cable; however, the 40 pin connectors do not change. The wires in the cable alternate: ground, signal, ground, signal, ground, signal, ground, etc. All the ground wires are tied together on the cable (and they are tied to the ground on the motherboard through the ground pins in the 40 pin connector). This cable conforms to the Small Form Factor Specification SFF-8049. This specification can be obtained from the Small Form Factor Committee.

Figure 48. Ultra ATA/66 Cable



Motherboard

- **ICH Placement:** The ICH should be placed within 8” of the ATA connector(s). There are no minimum length requirements for this spacing.
- **Capacitance:** The capacitance of each pin of the IDE connector on the host should be below 25 pF when the cables are disconnected from the host.
- **Series Termination:** There is no need for series termination resistors on the data and control signals since there is series termination integrated into these signal lines on the ICH.
  - A 1 kΩ pull-up to 5V is required on PIORDY and SIORDY.
  - A 470 Ω pull-down is required on pin 28 of each connector.
  - A 5.6 kΩ pull-down is required on PDREQ and SDREQ.
  - Support Cable Select (CSEL) is a PC99 requirement. The state of the cable select pin determines the master/slave configuration of the hard drive at the end of the cable.
  - Primary IDE connector uses IRQ14 and the secondary IDE connector uses IRQ15.
  - IRQ14 and IRQ15 each need an 8.2 kΩ pull-up resistor to VCC.
  - Due to the elimination of the ISA bus from the ICH, PCI_RST# should be connected to pin 1 of the IDE connectors as the IDE reset signal. Due to high loading, the PCI_RST# signal should be buffered.
  - There is no internal pull-up or down on PDD7 or SDD7 of the ICH. Devices shall not have a pull-up resistor on DD7. It is recommended that a host have a 10 kΩ pull-down resistor on PDD7 and SDD7 to allow the host to recognize the absence of a device at power-up (as required by the ATA-4 specification).
  - If no IDE is implemented with the ICH, the input signals (xDREQ and xIORDY) can be grounded and the output signals left as no connects.

Figure 49. Resistor Schematic for Primary IDE Connectors

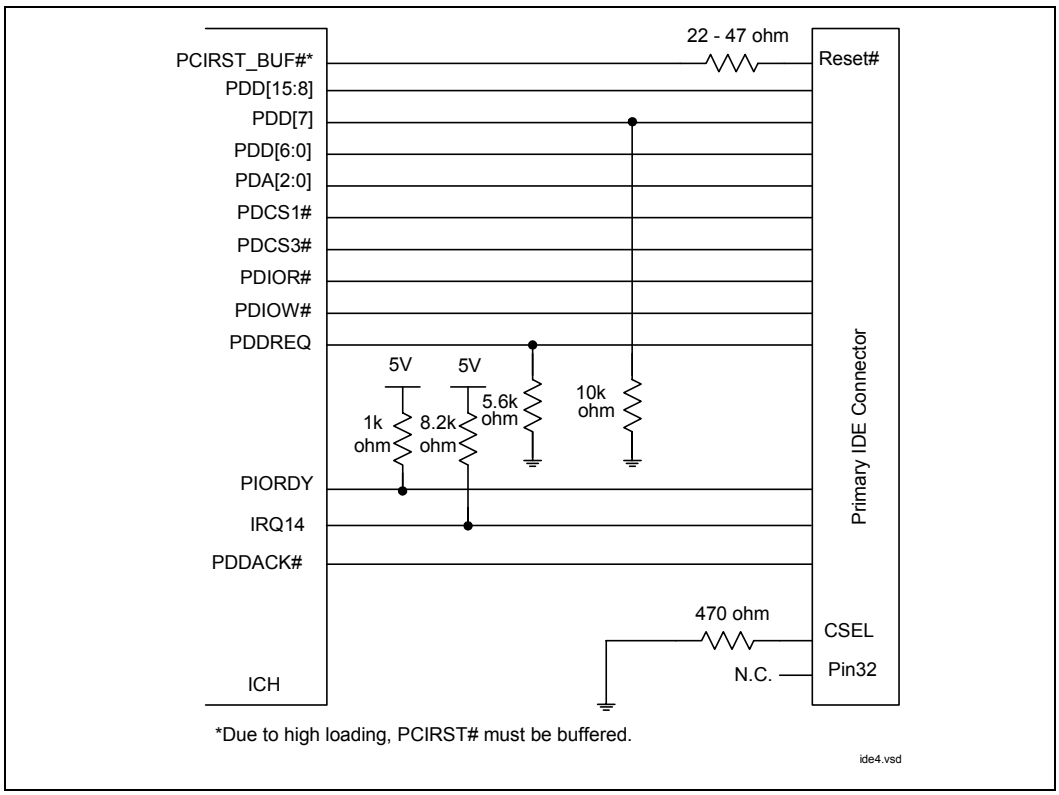
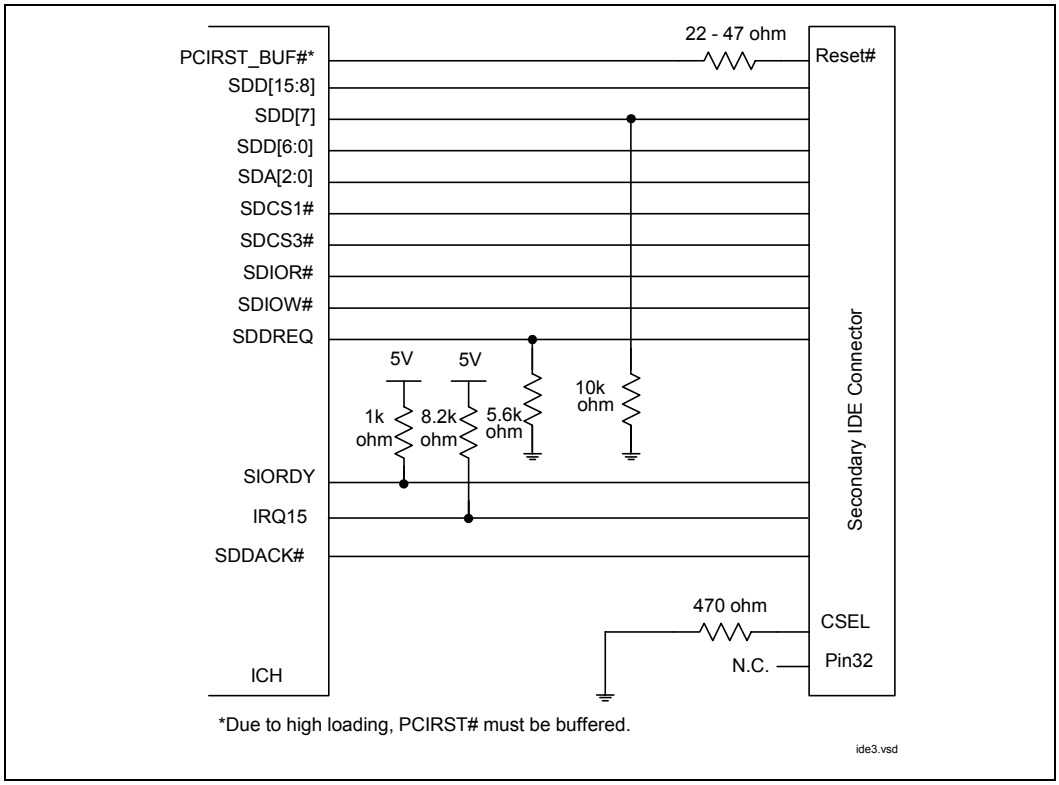


Figure 50. Resistor Schematic for Secondary IDE Connectors



6.8.2 Ultra ATA/66 Detection

The 82801AA ICH supports Ultra ATA/66 devices. The ATA/66 cable is an 80-conductor cable; however the 40 pin connectors used on motherboards for 40-conductor cables do not change as a result of this new cable. The wires in the cable alternate: ground, signal, ground, signal, ground, signal, ground, etc. All the ground wires are tied together at the connectors on the cable (and they are tied to the ground on the motherboard through the ground pins in the 40 pin connector). This cable conforms to the Small Form Factor Specification SFF-8049. This specification can be obtained from the Small Form Factor Committee.

To determine if ATA/66 mode can be enabled, the 810E chipset using the ICH requires the system BIOS to attempt to determine the cable type used in the system. The BIOS does this in one of two ways:

- Host Side Detection
- Device Side Detection

If the BIOS detects an 80-conductor cable, it may use any Ultra DMA mode up to the highest transfer mode supported by both the ICH and the IDE device. Otherwise, the BIOS can only enable modes that do not require an 80-conductor cable (example: Ultra ATA/33 Mode).

After determining the Ultra DMA mode to be used, the BIOS will configure the 810E chipset hardware and software to match the selected mode.

6.8.2.1 Ultra ATA/66 Motherboard Guidelines

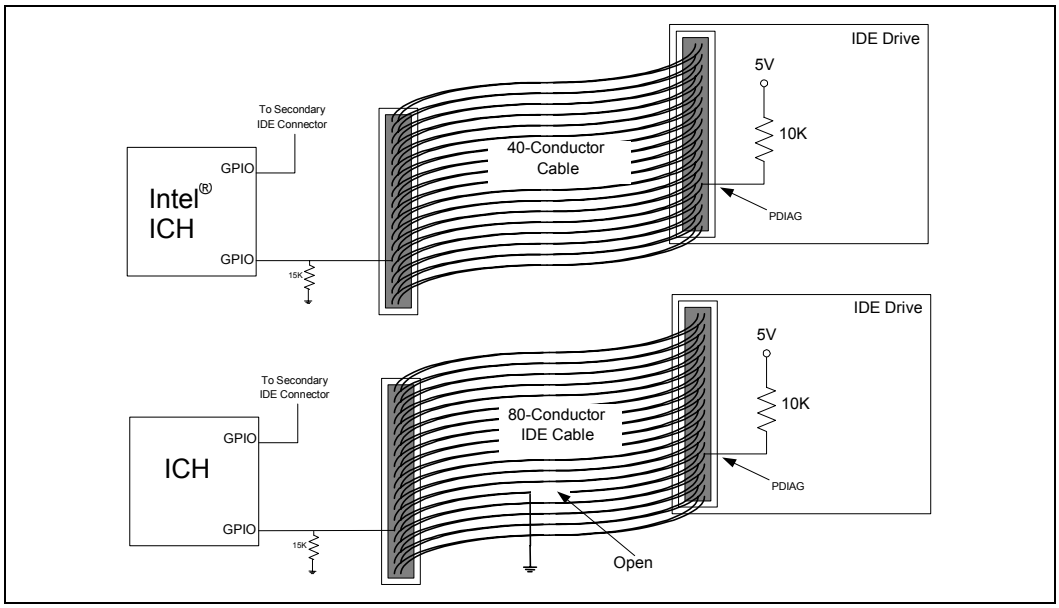
The 810E chipset can use two methods to detect the cable type. Each mode requires a different motherboard layout.

Host-Side Detection—BIOS Detects Cable Type Using GPIOs

Host side detection requires the use of two GPI pins (1 per IDE controller). The proper way to connect the PDIAG#/CBLID# signal of the IDE connector to the host is shown in the following figure. All Ultra ATA/66 devices have a 10 kΩ pull-up resistor to 5 volts. Most of the GPIO pins on the ICH and all GPIs on FWH Flash BIOS are not 5 volt tolerant. This requires a resistor divider so that 5 volts will not be driven to the ICH or FWH Flash BIOS pins. The proper value of the series resistor is 15 kΩ (as shown on The following Figure 51). This creates a 10 kΩ / 15 kΩ resistor divider and will produce approximately 3 volts for a logic high.

This mechanism allows the host, after diagnostics, to sample PDIAG#/CBLID#. If PDIAG#/ CBLIB# is high then there is 40-conductor cable in the system and ATA modes 3 and 4 should not be enabled. If PDIAG#/CBLID# is low then there is an 80-conductor cable in the system.

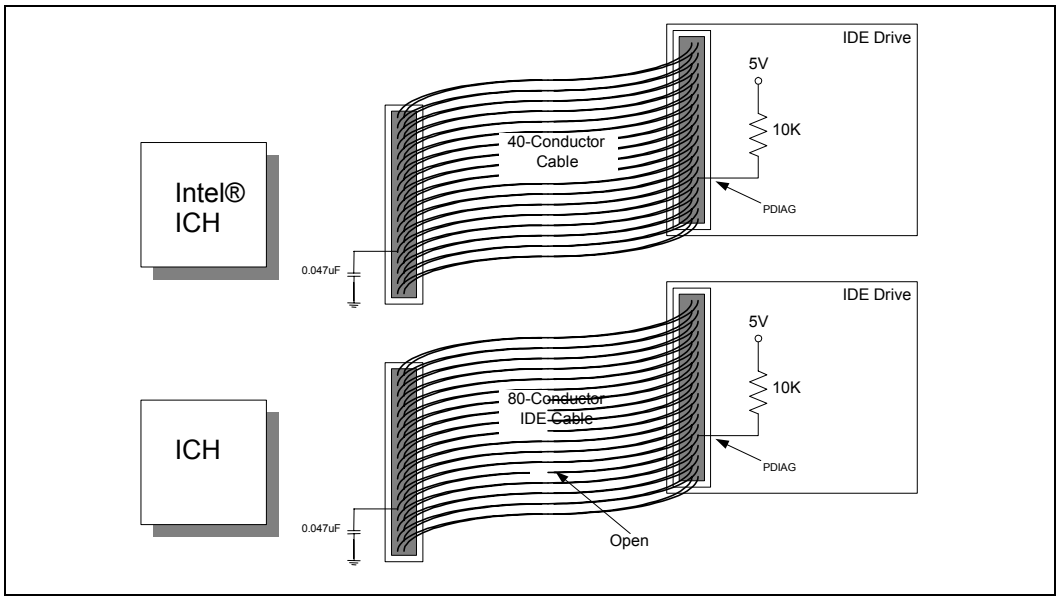
Figure 51. Host-Side IDE Cable Detection



Device-Side Detection—BIOS Queries IDE Drive for Cable Type

Device side detection requires only a 0.047 µF capacitor on the motherboard as shown in the following figure. This mechanism creates a resistor-capacitor (RC) time constant. The ATA mode 3 or 4 drive will drive PDIAG#/CBLID# low and then release it (pulled up through a 10 kΩ resistor). The drive will sample the PDIAG# signal after releasing it. In an 80-conductor cable, PDIAG#/CBLID# is not connected through and therefore the capacitor has no effect. In a 40-conductor cable, PDIAG#/CBLID# is connected though to the drive. Therefore, the signal rises more slowly. The drive can detect the difference in rise times and it reports the cable type to the BIOS when it sends the IDENTIFY_DEVICE packet during system boot as described in the ATA/66 specification.

Figure 52. Host-Side IDE Cable Detection

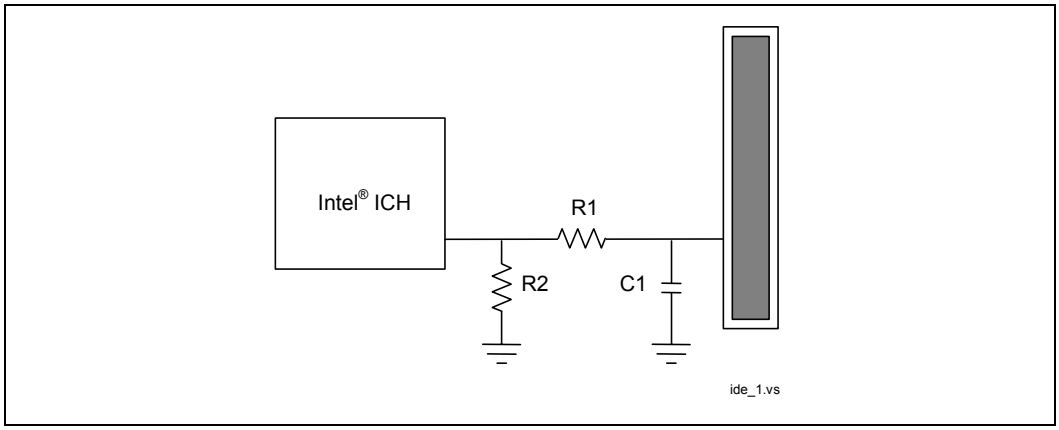


Layout for Both Host-Side and Drive-Side Cable Detection

It is possible to layout for both Host-Side and Drive-Side cable detection and decide the method to be used during assembly. The following Figure 53 shows the layout that allows for both host-side and drive-side detection.

- For Host-Side Detection
  - R1 is a 0 Ω resistor
  - R2 is a 15 kΩ resistor
  - C1 is not stuffed
- For Drive-Side Detection
  - R1 is not stuffed
  - R2 is not stuffed
  - C1 is a 0.047 µF capacitor

Figure 53. Host-Side IDE Cable Detection



6.9 AC'97

The ICH implements an AC'97 2.1 compliant digital controller. Any codec attached to the ICH AC-link should be AC'97 2.1 compliant as well. Contact your preferred codec vendor for information on AC'97 2.1 compliant products. The AC'97 2.1 specification is on the Intel website:

http://developer.intel.com/pc-supp/platform/ac97/index.htm

The ICH supports the following combinations of codecs:

Table 21. AC'97 Configuration Combinations

Primary	Secondary
Audio (AC)	None
Modem (MC)	None
Audio (AC)	Modem (MC)
Audio/Modem (AMC)	None

As shown in the above table, the ICH does not support two codecs of the same type on the link. For example, if an AMC is on the link, it must be the only codec. If an AC is on the link, another AC cannot be present.

6.9.1 Audio/Modem Riser Card (AMR)

Intel is developing a common connector specification known as the Audio/Modem Riser (AMR). This specification defines a mechanism for allowing OEM plug-in card options. The AMR specification is available on the Intel developer website:

http://developer.intel.com/pc-supp/platform/ac97/index.htm

The AMR specification provides a mechanism for AC'97 codecs to be on a riser card. This is important for modem codecs as it helps ease international certification of the modem.

6.9.2 AC'97 Routing

To ensure maximum performance from the codec, proper component placement and routing techniques are required. These techniques include properly isolating the codec, associated audio circuitry, analog power supplies, and analog ground planes from the rest of the motherboard. This includes plane splits and proper routing of signals not associated with the audio section. Contact your vendor for device specific recommendations.

Following are the basic recommendations:

- Special consideration must be given for the ground return paths for the analog signals. If isolated ground planes are used, pin B2 on the AMR connector should be used as an isolated ground pin and should be connected to an isolated ground plane to reduce noise in the analog circuits. The AMR designer and motherboard designer should jointly address any EMI issues when implementing isolated grounds.
- Digital signals routed in the vicinity of the analog audio signals must not cross the power plane split lines. Analog and digital signals should be located as far as possible from each other.
- Partition the board with all analog components grouped together in one area and all digital components in the other.
- Separate analog and digital ground planes should be provided, with the digital components over the digital ground plane, and the analog components, including the analog power regulators, over the analog ground plane. The split between the planes must be a minimum of 0.05” wide.
- Keep digital signal traces, especially the clock, as far way from analog input and voltage reference pins as possible.
- Do not completely isolate the analog/audio ground plane from the rest of the board ground plane. There should be a single point (¼” to ½ ” wide) where the analog/isolated ground plane connects to the main ground plane. The split between the planes must be a minimum of 0.05” wide.
- Any signals entering or leaving the analog area must cross the ground split in the area where the analog ground is attached to the main motherboard ground (i.e., there should not be any signals crossing the split/gap between the ground planes). Doing so will cause a ground loop. This will greatly increase EMI emissions and degrade analog and digital signal quality.
- Analog power and signal traces should be routed over the analog ground plane.
- Digital power and signal traces should be routed over the digital ground plane.
- Bypassing and decoupling capacitors should be close to the IC pins, or positioned for the shortest connections to pins, with wide traces to reduce impedance.
- All resistors in the signal path or on the voltage reference should be metal film. Carbon resistors can be used for DC voltages and the power supply path where voltage coefficient, temperature coefficient or noise are not a factor.
- Regions between analog signal traces should be filled with copper, which should be electrically attached to the analog ground plane. Regions between digital signal traces should be filled with copper, which should be electrically attached to the digital ground plane.
- Locate the crystal or oscillator close to the codec.
- The following two Figure 54, Figure 55 show the motherboard trace lengths for an ATX form factor with a codec on the motherboard and an AMR connector. Two routing methods are provided for the AC’97 interface: the tee topology and the daisy-chain topology. The AC’97 link signals can be routed using 5 mil traces with 5 mil space between the traces. NLX routing recommendations will be provided in a future revision of this document.

Figure 54. Tee Topology AC'97 Trace Length Requirements for ATX

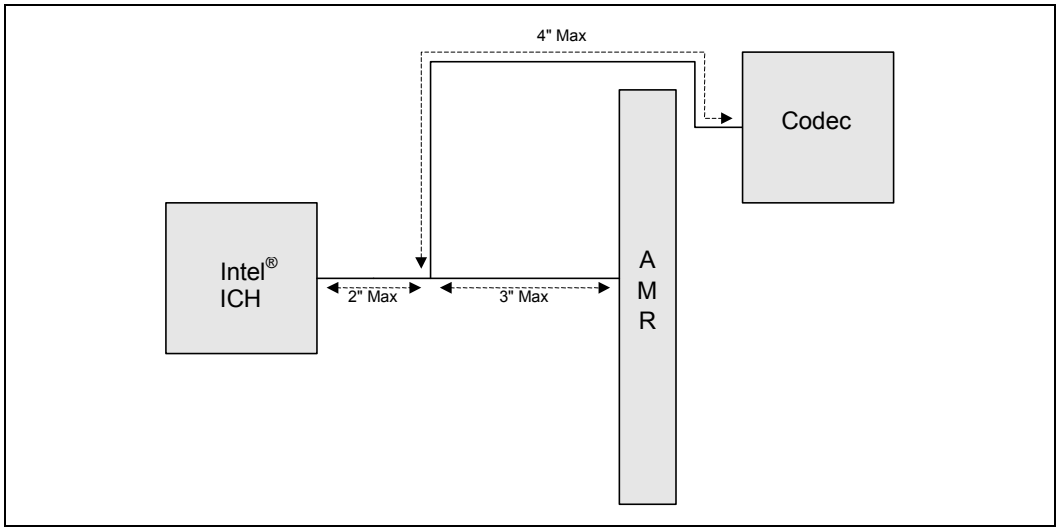
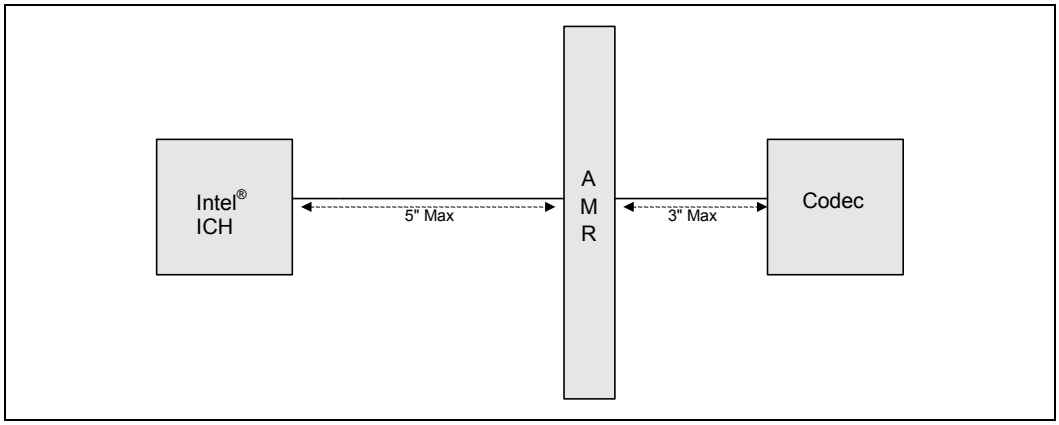


Figure 55. Daisy-Chain Topology AC'97 Trace Length Requirements for ATX



Clocking is provided from the primary codec on the link via BITCLK, and is derived from a 24.576 MHz crystal or oscillator. Refer to the primary codec vendor for crystal or oscillator requirements. BITCLK is a 12.288 MHz clock driven by the primary codec to the digital controller (ICH), and any other codec present. That clock is used as the timebase for latching and driving data.

The ICH supports wake on ring from S1-S4 via the AC'97 link. The codec asserts SDATAIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec.

If no codec is attached to the link, internal pull-downs will prevent the inputs from floating; therefore, external resistors are not required.

6.9.3 Motherboard Implementation

The following design considerations are provided for the implementation of an ICH platform using AC'97. These design guidelines have been developed to ensure maximum flexibility for board designers while reducing the risk of board related issues. These recommendations do not represent the only implementation or a complete checklist, but provides recommendations based on the ICH platform.

- Codec Implementation
  - The motherboard can implement any valid combination of codecs on the motherboard and on the riser. For ease of homologation, it is recommended that a modem codec be implemented on the AMR module; however, nothing precludes a modem codec on the motherboard.
  - Only one primary codec can be present on the link. A maximum of two present codecs can be supported in an ICH platform.
  - If the motherboard implements an active primary codec on the motherboard and provides an AMR connector, it must tie PRI_DN# to ground.
  - The PRI_DN# pin is provided to indicate a primary codec is present on the motherboard. Therefore, the AMR module and/or codec must provide a means to prevent contention when this signal is asserted by the motherboard, without software intervention.
  - Components such as FET switches, buffers, or logic states should not be implemented on the AC-link signals, except for AC_RST#. Doing this will potentially interfere with timing margins and signal integrity.
  - If the motherboard requires that an AMR module override a primary codec down, a means of preventing contention on the AC-link must be provided for the onboard codec.
  - The ICH supports Wake On Ring from S1-S4 states via the AC'97 link. The codec asserts SDATAIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec. If no codec is attached to the link, internal pull-downs prevent the inputs from floating; therefore, external resistors are not required. The ICH does not wake from the S5 state via the AC'97 link.
  - The SDATAIN[0:1] pins should not be left in a floating state if the pins are not connected and the AC-link is active—they should be pulled to ground through a weak (approximately 10 kΩ) pull-down resistor. If the AC-link is disabled (by setting the shut-off bit to 1), then the ICH's internal pull-down resistors are enabled, and thus there is no need for external pull-down resistors. However, if the AC-link is to be active, then there should be pull-down resistors *on any SDATAIN signal that has the potential of not being connected to a codec*. For example, if a dedicated audio codec is on the motherboard, and cannot be disabled via a hardware jumper or stuffing option, then its SDATAIN signal does not need a pull-down resistor. If, however, the SDATAIN signal has no codec connected, or is connected to an AMR slot, or is connected to an onboard codec that can be hardware disabled, then the signal should have an external pull-down resistor to ground.
  - In a lightly loaded system (e.g., single codec down), AC'97 signal integrity analysis should be evaluated to confirm that the signal quality on the link is acceptable by the codec used in the design. A series resistor at the driver and/or a capacitor at the codec can be implemented to compensate for any signal integrity issues. The values used are design dependent and should be verified for correct timings. The ICH AC-link output buffers are designed to meet the AC'97 2.1 specification with the specified load of 5.

- AMR Slot Special Connections
  - AUDIO_MUTE#: No connect on the motherboard.
  - AUDIO_PWRDN: No connect on the motherboard. Codecs on the AMR card should implement a powerdown pin, per the AC'97 2.1 specification, to control the amplifier.
  - MONO_PHONE: Connect top onboard audio codec if supported.
  - MONO_OUT/PC_BEEP: Connect to SPKR output from the ICH, or MONO_OUT from onboard codec.
  - PRIMARY_DN#: See discussion above.
  - +5VDUAL/+5VSB: Connect to VCC5 core on the motherboard, unless adequate power supply is available. An AMR card using this standby/dual supply should not prevent basic operation if this pin is connected to core power.
  - S/P-DIF_IN: Connect to ground on the motherboard.
  - AC_SDATAIN[3:2]: No connect on the motherboard. The ICH supports a maximum of two codecs, which should be attached to SDATAIN[1:0].
  - AC97_MSTRCLK: Connect to ground on the motherboard.
- The ICH provides internal weak pull-downs. Therefore, the motherboard does not need to provide discrete pull-down resistors.
- PC_BEEP should be routed through the audio codec. Care should be taken to avoid the introduction of a pop when powering the mixer up or down.

6.10 USB

The following are general guidelines for the USB interface:

- Unused USB ports should be terminated with 15 kΩ pull-down resistors on both P+/P- data lines.
- 15 Ω series resistors should be placed as close as possible to the ICH (<1 inch). These series resistors are there for source termination of the reflected signal.
- 47 pF caps must be placed as close to the ICH as possible, and on the ICH side of the series resistors on the USB data lines (P0±, P1±). These caps are for signal quality (rise/fall time) and to help minimize EMI radiation.
- 15 kΩ ± 5% pull-down resistors should be placed on the USB side of the series resistors on the USB data lines (P0±, P1±), and are for signal termination required by the USB specification. The length of the stub should be as short as possible.
- The trace impedance for the P0±, P1±- signals should be 45 Ω (to ground) for each USB signal P+ or P-. This may be achieved with 9 mil wide traces on the motherboard based on the stackup recommended in Figure 33. The impedance is 90 Ω between the differential signal pairs P+ and P- to match the 90 Ω USB twisted pair cable impedance. Note that the twisted pair characteristic impedance of 90 Ω is the series impedance of both wires, resulting in an individual wire presenting a 45 Ω impedance. The trace impedance can be controlled by carefully selecting the trace width, trace distance from power or ground planes, and physical proximity of nearby traces.
- USB data lines should be routed as 'critical signals' (i.e., hand routing preferred). The P+/P- signal pair should be routed together and not parallel with other signal traces to minimize crosstalk. Doubling the space from the P+/P- signal pair to adjacent signal traces will help to prevent crosstalk. The P+/P- signal traces should also be the same length. This minimizes the effect of common mode current on EMI.

- 47 pF caps should be placed as close as possible to the USB connectors to help minimize EMI radiation.

The following Figure 56 illustrates the recommended USB schematic.

Figure 56. USB Data Signals

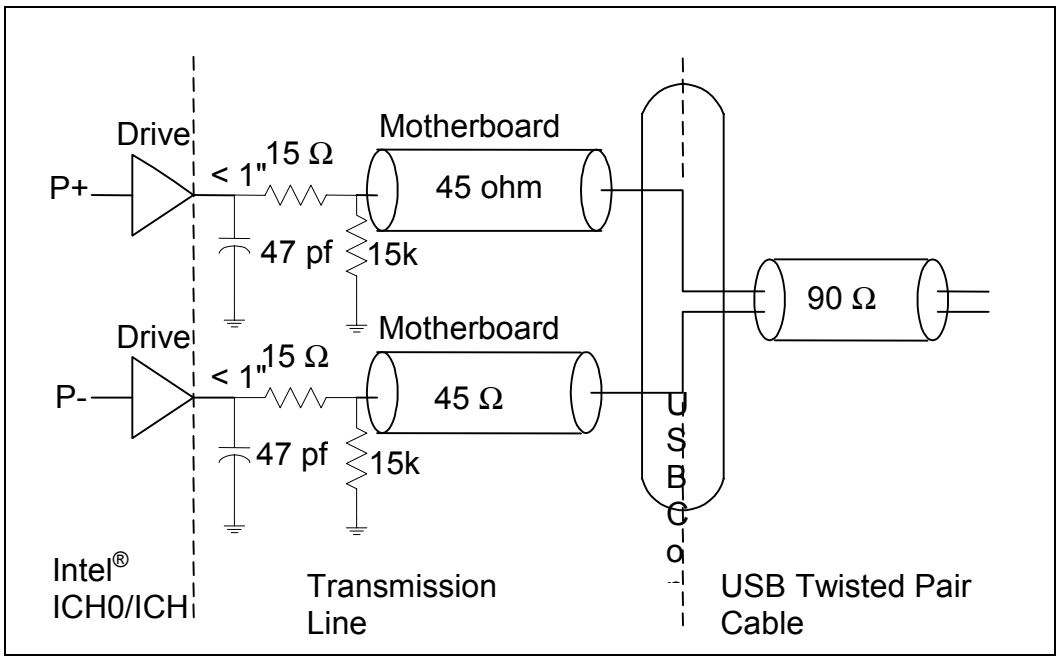


Table 22. Recommended USB Trace Characteristics

Impedance 'Z0' = 45.4 Ω
Line Delay = 160.2 ps
Capacitance = 3.5 pF
Inductance = 7.3 nH
Res @ 20° C = 53.9m Ω

6.11 IOAPIC (I/O Advanced Programmable Interrupt Controller)

Systems that do not use the ICH I/O APIC should follow these recommendations:

On the ICH:
- Tie PICCLK directly to ground
- Tie PICD0, PICD1 directly to ground

On the processor:
- PICCLK must be connected from the clock generator to the PICCLK pin on the processor
- Tie PICD0 to VCC_{CMOS} through a 150 Ω resistor

- Tie PICD1 to VCC_{CMOS} through a 150 Ω resistor

Note: If not using IOAPIC, turn off APIC clocks to ICH through I^2C.

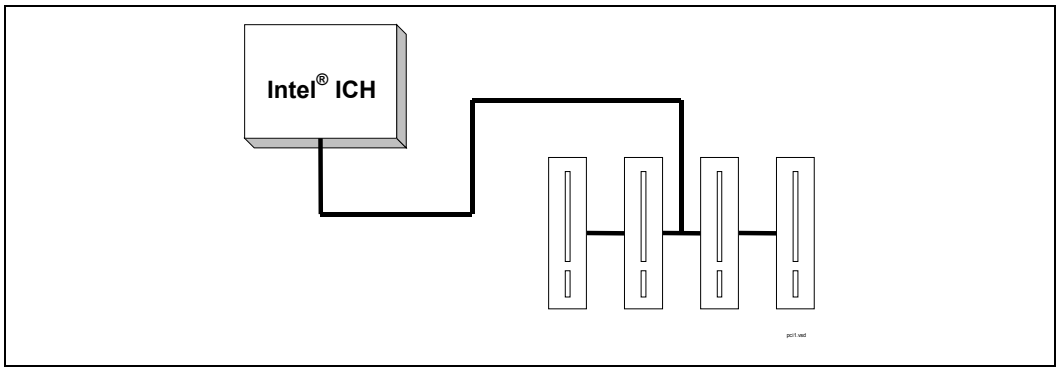
6.12 PCI

The ICH provides a PCI Bus interface that is compliant with the *PCI Local Bus Specification Revision 2.2*. The implementation is optimized for high-performance data streaming when the ICH is acting as either the target or the initiator on the PCI bus. For more information on the PCI Bus interface, please refer to the *PCI Local Bus Specification Revision 2.2*.

The ICH supports 6 PCI Bus masters (excluding ICH), by providing 6 REQ#/GNT# pairs. In addition, the ICH supports 2 PC/PCI REQ#/GNT# pairs, one of which is multiplexed with a PCI REQ#/GNT# pair.

The ICH, based on simulations done by Intel, it is recommended that four is the maximum number of PCI slots that should be connected to the ICH. This limit is due to timing and loading considerations established during simulations. If a system designer wants to have 5 PCI slots connected to the ICH, then it is recommended that they do simulations to verify proper design.

Figure 57. PCI Bus Layout Example for 4 PCI Connectors



6.13 RTC

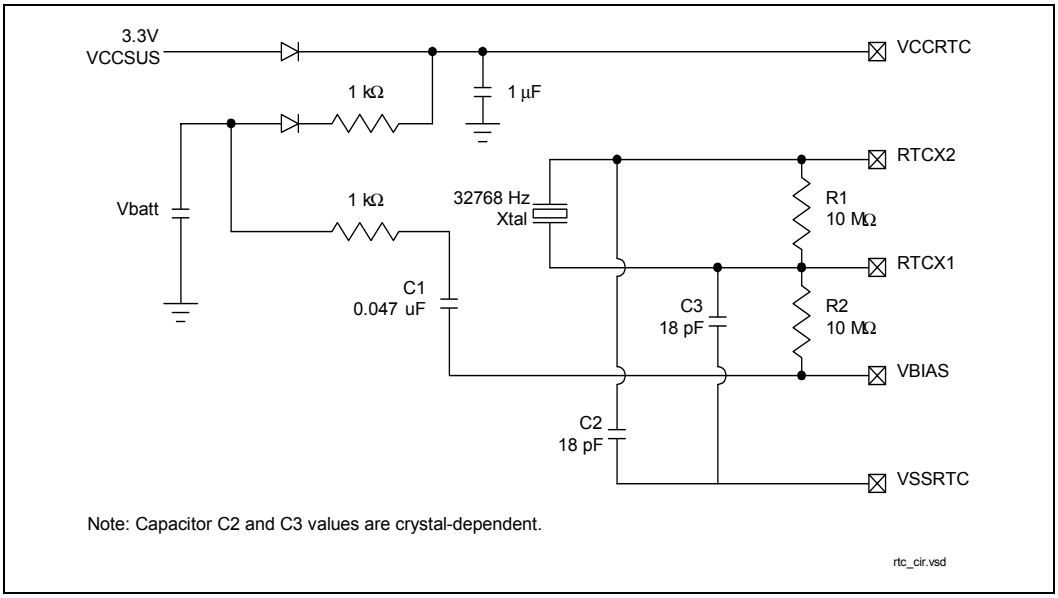
The ICH contains a real time clock (RTC) with 256 bytes of battery backed SRAM. This internal RTC module provides two key functions: a) keeping date and time, b) storing system data in its RAM when the system is powered down.

This section will present the recommended hookup for the RTC circuit for the ICH. **This circuit is not the same as the circuit used for the PIIX4.**

6.13.1 RTC Crystal

The ICH RTC module requires an external oscillating source of 32.768 kHz connected on the RTCX1 and RTCX2 pins. The following Figure 58 represents the external circuitry that comprises the oscillator of the ICH RTC.

Figure 58. External Circuitry for the Intel® ICH RTC



NOTES:

1. The exact capacitor value should be based on the crystal vendor's recommendations.
2. VccRTC: Power for RTC Well.
3. RTCX2: Crystal Input 2 – Connected to the 32.768 kHz crystal.
4. RTCX1: Crystal Input 1 – Connected to the 32.768 kHz crystal.
5. VBIAS: RTC BIAS Voltage – This pin is used to provide a reference voltage, and this DC voltage sets a current which is mirrored throughout the oscillator and buffer circuitry.
6. Vss: Ground.

6.13.2 External Capacitors

To maintain the RTC accuracy, the external capacitor C1 should be set to 2200 pF, and the external capacitor values (C2 and C3) should be chosen to provide the manufacturer's specified load capacitance (Cload) for the crystal when combined with the parasitic capacitance of the trace, socket (if used), and package. The following equation can be used to choose the external capacitance values (C2 and C3):

$$Cload = (C2*C3)/(C2+C3) + Cparasitic$$

C3 can be chosen such that C3 > C2; then, C2 can be trimmed to obtain the 32.768 kHz.

6.13.3 RTC Layout Considerations

- Keep the XTAL lead lengths as short as possible; around 1 inch is sufficient.
- Minimize the capacitance between RTCX1and RTCX2 in the routing.
- Put a ground plane under the XTAL components.
- Do not route any switching signals under the external components (unless on the other side of the board).

- The oscillator VCC should be clean; use a filter (e.g., an RC lowpass) or a ferrite inductor.
- Keep high speed switching signals (e.g., PCI signals) away from VCCRTC, RTCX1, RTCX2 and VBIAS.

6.13.4 RTC External Battery Connection

The RTC requires an external battery connection to maintain its functionality and its RAM while the ICH is not powered by the system.

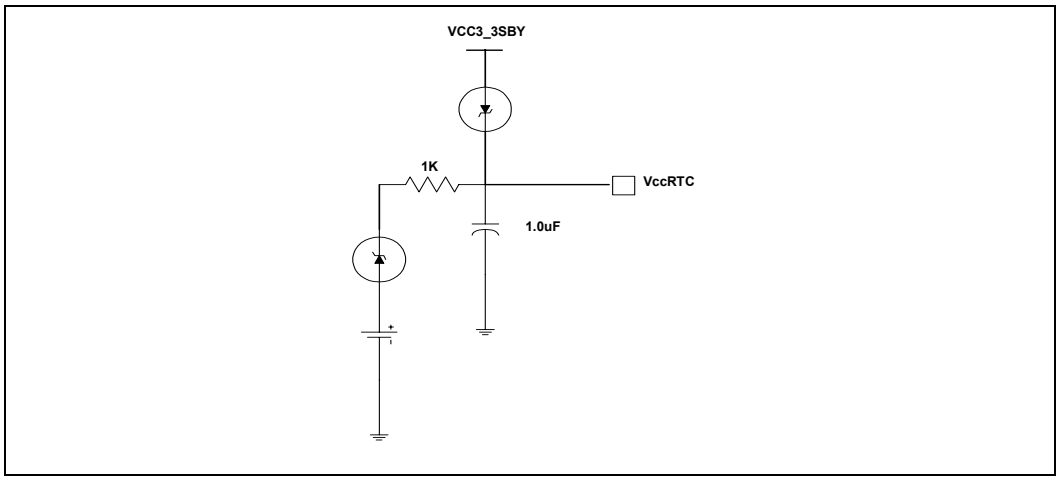
Example batteries are: Duracell* 2032, 2025, or 2016 (or equivalent), which can give many years of operation. Batteries are rated by storage capacity. The battery life can be calculated by dividing the capacity by the average current required. For example, if the battery storage capacity is 170 mA per hour (assumed usable) and the average current required is 3 uA, the battery life will be at least:

170,000 uAhr / 3 uA = 56,666 h = 6.4 years

The voltage of the battery can affect the RTC accuracy. In general, when the battery voltage decays, the RTC accuracy also decreases. High accuracy can be obtained when the RTC voltage is in the range of 3.0V to 3.3V.

The battery must be connected to the ICH via an isolation diode circuit. The diode circuit allows the ICH RTC well to be powered by the battery when the system power is not available, but by the system power when it is available. To do this, the diodes are set to be reverse-biased when the system power is not available. The following Figure 59 is an example of a diode circuitry that can be used.

Figure 59. A Diode Circuit to Connect RTC External Battery

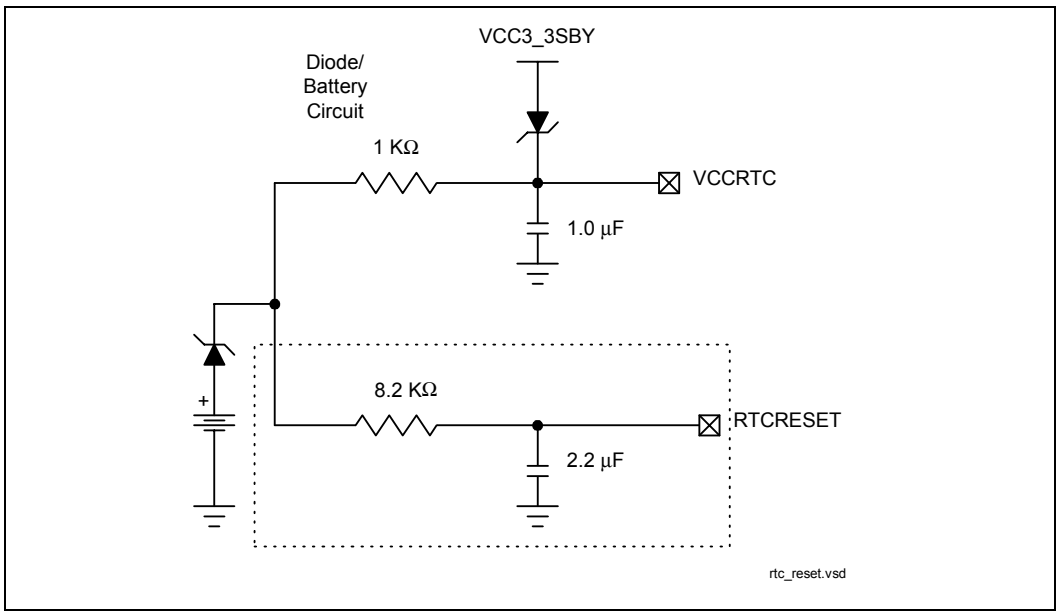


A standby power supply should be used to provide continuous power to the RTC when available, which will significantly increase the RTC battery life and thereby the RTC accuracy.

6.13.5 RTC External RTCRESET Circuit

The ICH RTC requires some additional external circuitry. The RTCRESET (RTC Well Test) signal is used to reset the RTC Well. The external capacitor (2.2 µF) and the external resistor (8.2 kΩ) between RTCRESET and the RTC battery (Vbat) were selected to create a RC time delay, such that RTCRESET goes high some time after the battery voltage is valid. The RC time delay should be in the range of 10–20 ms. When RTCRESET is asserted bit 2 (RTC_PWR_STS) in the GEN_PMCON_3 (General PM Configuration 3) register is set to 1, and remains set until software clears it. As a result, when the system boots, BIOS knows that the RTC battery has been removed.

Figure 60. RTCRESET External Circuit for the Intel® ICH RTC



This RTCRESET circuit is combined with the diode circuit (Figure 59) which allows the RTC well to be powered by the battery when the system power is not available. Figure 60 is an example of this circuitry that is used, in conjunction with the external diode circuit.

6.13.6 VBIAS DC Voltage and Noise Measurements

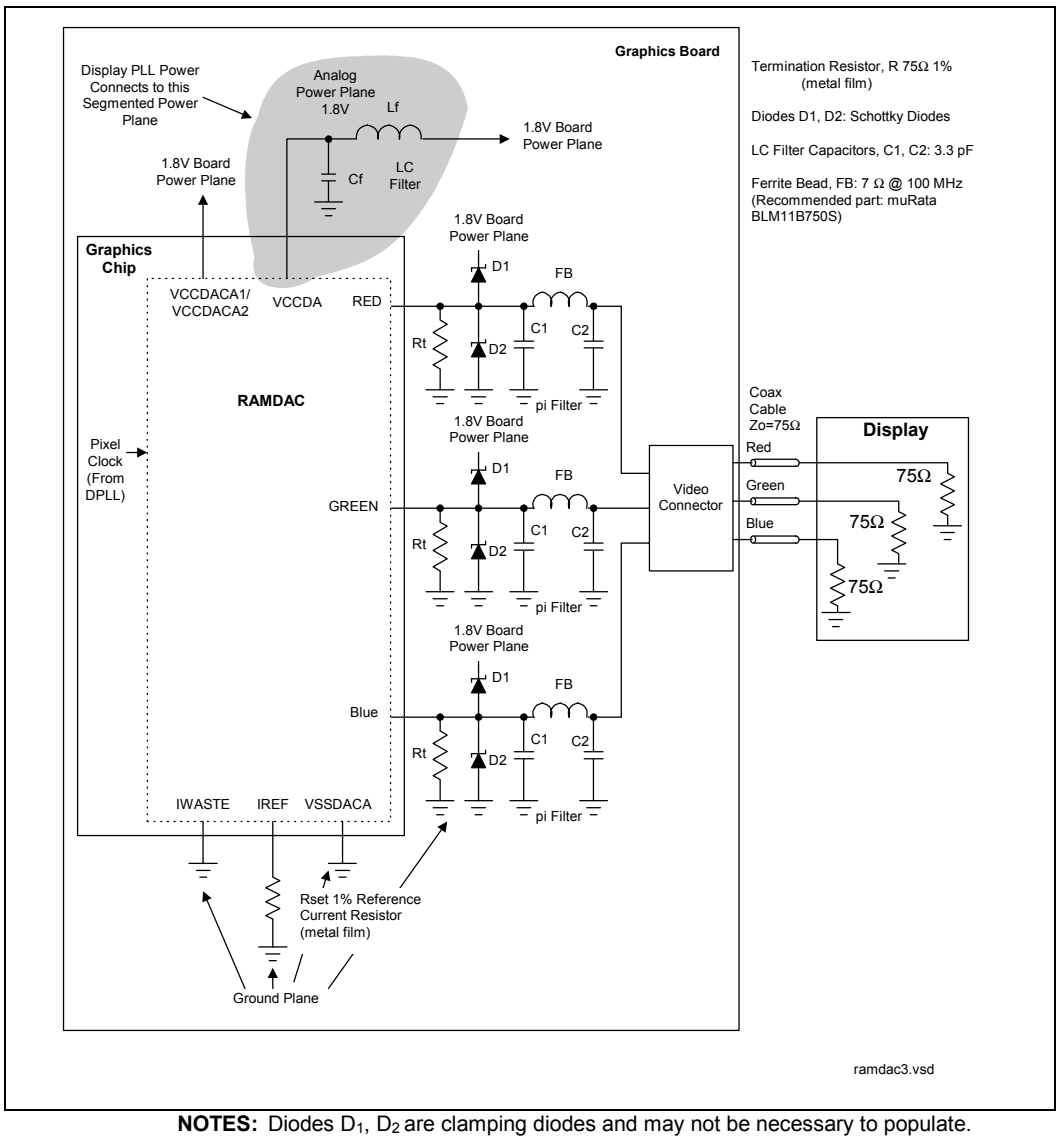
- Steady state VBIAS will be a DC voltage of about 0.38V ±.06V.
- VBIAS will be “kicked” when the battery is inserted to about 0.7–1.0V; it will come back to its DC value within a few ms.
- Noise on VBIAS must be kept to a minimum (200 mV or less).
- VBIAS is very sensitive and can not be directly probed; it can be probed through a 0.01 µF capacitor.
- Excess noise on VBIAS can cause the ICH internal oscillator to misbehave or even stop completely.

- To minimize noise of VBIAS it is necessary to implement the routing guidelines described above and the required external RTC circuitry as described in the *Intel® 82801AA (ICH) and Intel® 82801AB (ICH0) I/O Controller Hub* Datasheet.

6.14 RAMDAC/Display Interface

The following Figure 61 shows the interface of the RAMDAC analog current outputs with the display. Each DAC output is doubly-terminated with a 75 Ω resistance; one 75 Ω resistance from the DAC output to the board ground and the other termination resistance exists within the display. The equivalent dc resistance at the output of each DAC output is 37.5 Ω. The output current of each DAC flows into this equivalent resistive load to produce a video voltage without the need for external buffering. There is also an LC pi-filter which is used to reduce high-frequency glitches and noise, and reduce EMI. To maximize the performance, the filter impedance, cable impedance and load impedance should be the same. The LC pi-filter consists of two 3.3 pF capacitors and a ferrite bead with a 75 Ω impedance at 100 MHz. The LC pi-filter is designed to filter glitches produced by the RAMDAC while maintaining adequate edge rates to support high-end display resolutions.

Figure 61. Schematic of RAMDAC Video Interface



NOTES: Diodes D_1, D_2 are clamping diodes and may not be necessary to populate.

In addition to the termination resistance and LC pi-filter, there are protection diodes connected to the RAMDAC outputs to help prevent latch-up. The protection diodes must be connected to the same power supply rails as the RAMDAC. An LC filter is recommended to connect the segmented analog 1.8V power plane of the RAMDAC to the 1.8V board power plane. The LC filter is recommended to be designed for a cut-off frequency of 100 kHz.

6.14.1 Reference Resistor (Rset) Calculation

The full-swing video output is designed to be 0.7V according to the VESA video standard. With an equivalent dc resistance of 37.5 Ω (two 75 Ω in parallel - one 75 Ω termination on the board and one 75 Ω termination within the display), the full-scale output current of a RAMDAC channel is 0.7/37.5 Ω = 18.67 mA. Since the RAMDAC is an 8-bit current-steering DAC, this full-scale current is equivalent 255I, where I is a unit current. Therefore, the unit current or LSB current of the DAC signals equals 73.2 µA. The reference circuitry generates a voltage across this R_{set} resistor equal to a bandgap voltage divided-by-three (409 mV). The RAMDAC reference current generation circuitry is designed to generate a 32I reference current using the reference voltage and the R_{set} value. To generate a 32I reference current for the RAMDAC, the reference current setting resistor, R_{set}, is calculated from the following equation:

$$R_{set} = V_{REF}/32I = 0.409V/32*73.2\mu A = 174\ \Omega$$

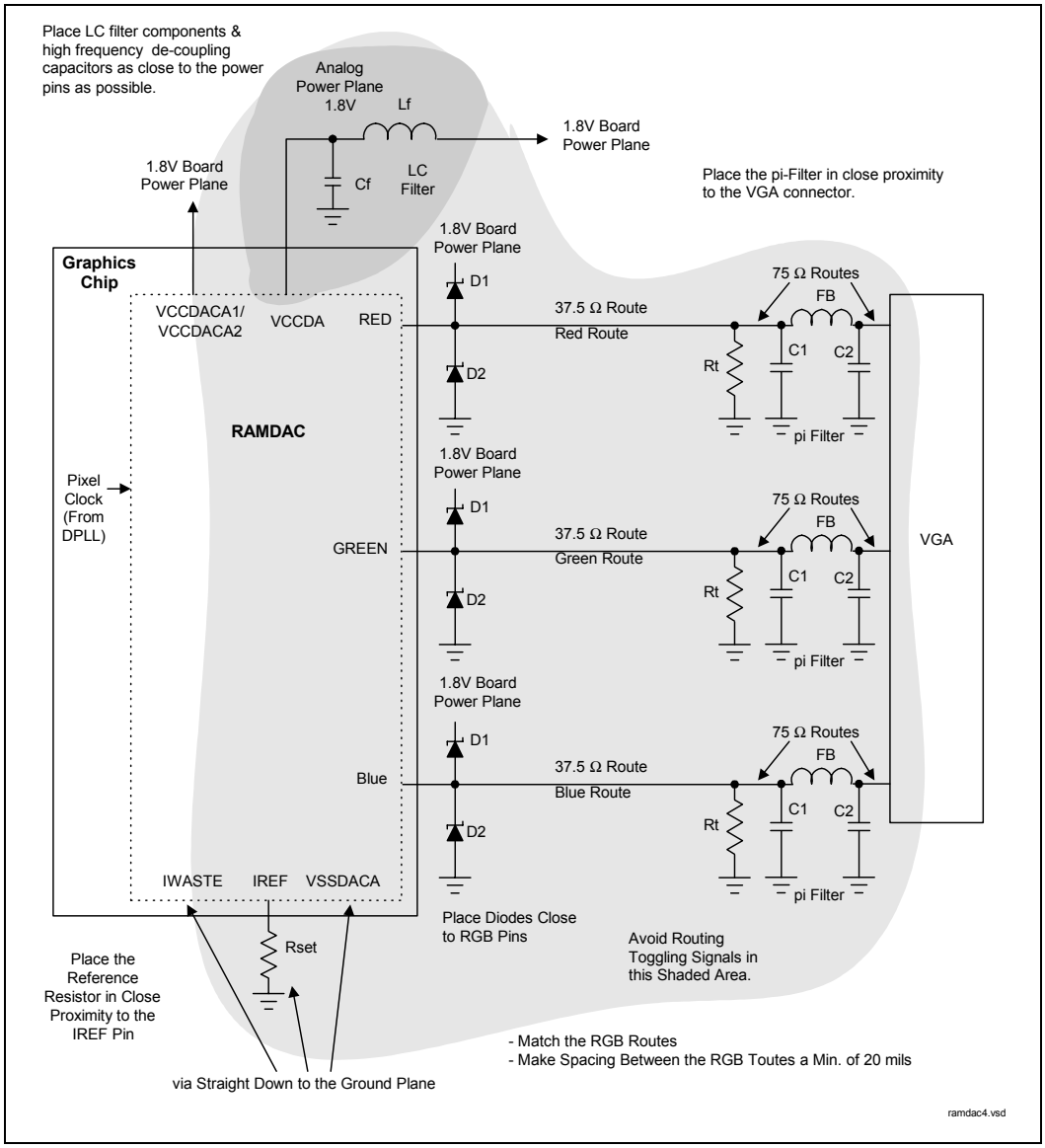
6.14.2 RAMDAC Board Design Guidelines

The RAMDAC layout is shown in the following three figures.(Figure 62, Figure 63, Figure 64) An RLC network should be used between the board power plane and the board ground plane. The recommended RAMDAC routing for a four layer board is such that the red, green and blue video outputs be routed on the top (bottom) layer over (under) a solid ground plane to maximize noise rejection characteristics of the video outputs. It is essential to avoid toggling signals from being routed next to the video output signals to the VGA connector. A 20 mil spacing between any video route and any other routes is recommended.

Matching of the video routes (red, green, and blue) from the RAMDAC to the VGA connector is also essential. The routing for these signals should be as similar as possible (i.e., same routing layer(s), same number of vias, same routing length, same bends and jogs).

The following figure shows recommended RAMDAC component placement and routing. The termination resistance can be placed anywhere along the video route from the RAMDAC output to the VGA connector as long as the impedance of the traces are designed as indicated in the following figure. The pi- filters are recommended to be placed in close proximity to the VGA connector to maximize EMI filtering effectiveness. The LC filter components for the RAMDAC/PLL power plane, de-coupling capacitors, latch-up protection diodes, and the reference resistor are recommended to be placed in close proximity to the respective pins.

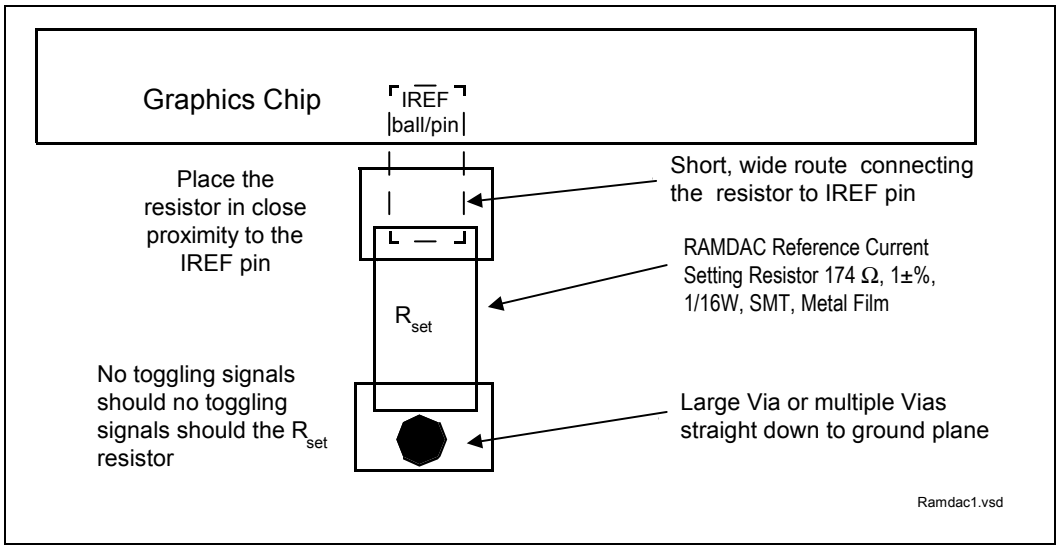
Figure 62. RAMDAC Component and Routing Guidelines



NOTES: Diodes D_1, D_2 are clamping diodes and may not be necessary to populate.

The following Figure 63 shows the recommended reference resistor placement and connections.

Figure 63. Recommended RAMDAC Reference Resistor Placement and Connections



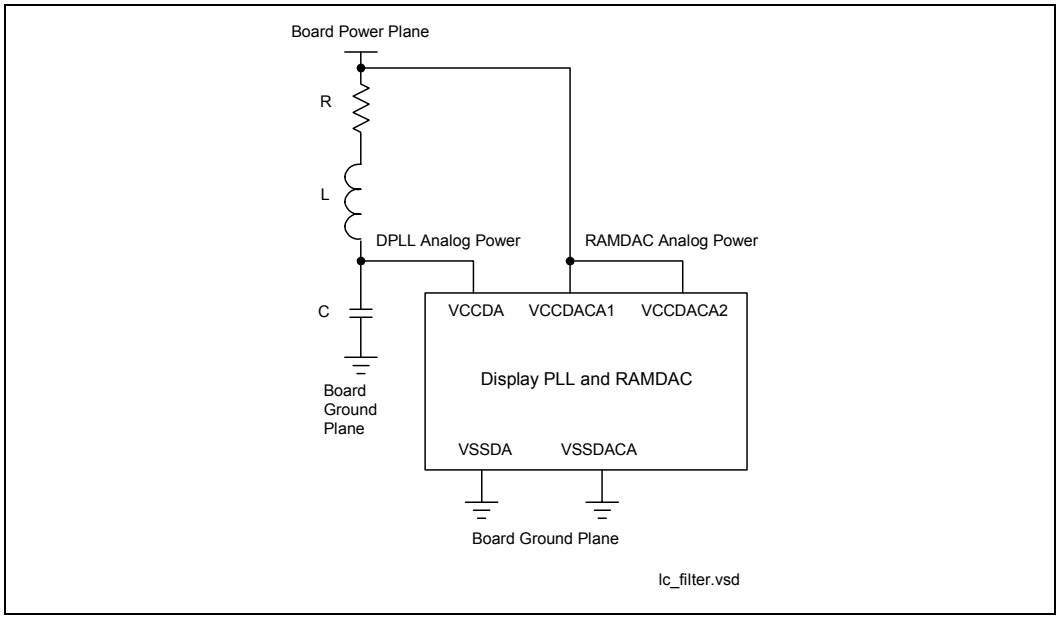
6.15 DPLL Filter Design Guidelines

The Intel® 810E Chipset contains sensitive phase-locked loop circuitry, the DPLL, that can cause excessive dot clock jitter. Excessive jitter on the dot clock may result in a "jittery" image. An LC filter network connected to the DPLL analog power supply is recommended to reduce dot clock jitter.

The DPLL bandwidth varies with the resolution of the display and can be as low as 100 kHz. In addition, the DPLL jitter transfer function can exhibit jitter peaking effects in the range from 100 kHz to a few megahertz. A low-pass LC filter is recommended for the display PLL analog power supply designed to attenuate power supply noise with frequency content from 100 kHz and above so that jitter amplification is minimized.

The following figure is a block diagram showing the recommended topology of the filter connection (parasitics not shown). The display PLL analog power rail (VCCDA) is connected to the board power plane through an LC filter. The RAMDAC analog power rail (VCCDACA1 and VCCDACA2) are connected directly to the 1.8V board power plane.

Figure 64. Recommended LC Filter Connection



The resistance from the inductor to the board 1.8V power plane represents the total resistance from the board power plane to the filter capacitor. This resistance, which can be a physical resistor, routing/via resistance, parasitic resistance of the inductor or combinations of these, acts as a damping resistance for the filter and effects the response of the filter.

The LC filter topology shown in the above Figure 64 is the preferred choice since the RAMDAC minimum voltage level requirement does not place constraints on the LC filter for the DPLL. The maximum current flowing into the DPLL analog power is approximately 30 mA, much less than that of the RAMDAC, and therefore, a filter inductor with a higher dc resistance can be tolerated. With the topology in the above Figure 64, the filter inductor dc current rating must be at least 30 mA and the maximum IR drop from the board power plane to the VCCDA ball should be 100 mV or less (corresponds to a series resistance equal to or less than 3.3 Ω. This larger dc resistance tolerance improves the damping and the filter response.

6.15.1 Filter Specification

The low-pass filter specification with the input being the board power plane and the output measured across the filter capacitor is defined as follows for the filter topology shown in Figure 64.

- pass band gain < 0.2 dB
- dc IR drop from board power plane to the DPLL VCCDA ball < 100 mV (and a maximum dc resistance < 3.3 Ω)
- filter should support a dc current > 30 mA
- minimum attenuation from 100 kHz to 10 MHz = 10 dB (desired attenuation > 20 dB)

- a magnetically shielded inductor is recommended

The resistance from the board power plane to the filter capacitor node should be designed to meet the filter specifications outlined above. This resistance acts as a damping resistance for the filter and affects the filter characteristics. This resistance includes the routing resistance from the board power plane connection to the filter inductor, the filter inductor parasitic resistance, the routing from the filter inductor to the filter capacitor, and resistance of the associated vias. Part of this resistance can be a physical resistor. A physical resistor may not be needed depending on the resistance of the inductor and the routing/via resistance.

The filter capacitance should be chosen with as low of an ESR (equivalent series resistance) and ESL (equivalent series inductance) as possible to achieve the best filter performance. The parasitics of the filter capacitor can alter the characteristics of the filter significantly and even cause the filter to be ineffective at the frequencies of interest. The LC filter must be simulated with all the parasitics of the inductor, capacitor, and associated routing parasitics along with tolerances.

6.15.2 Recommended Routing/Component Placement

- The filter capacitance should be placed as close to the VCCDA ball as possible so that the routing resistance from the filter capacitor lead to the package VCCDA ball is < 0.1 Ω.
- The VSSDA ball should via straight down to the board ground plane.
- The filter inductor should be placed in close proximity to the filter capacitor and any routing resistance should be inserted between the board power plane connection and the filter inductor.
- If a discrete resistor is used for the LC filter, the resistor should be placed between the board power plane connection and the filter inductor.

6.15.3 Example LC Filter Components

Table 23 and Table 24 shows example LC components and resistance for the LC filter topology shown in Figure 64.

Table 23. DPLL LC Filter Component Example

Component	Manufacturer	Part No.	Description
Capacitor	KEMET	T495D336MD16AS	33 µF ±20%, 16VDC, ESR=0.225 Ω @ 100 kHz, ESL=2.5nH
Inductor	muRATA	LQG11A68NJ00	68 nH ±5%, 300 mA, Max dc resistance = 0.8 Ω, size=0603
Resistance			< 3.3 Ω

The resistance of the filter is defined as the total resistance from the board power plane to the filter inductor. If a discrete resistor is used as part of this resistance, the tolerance and temperature coefficient should be accounted for so that the maximum dc resistance in this path from the board power plane connection to the DPLL VCCDA ball is less than 3.3 Ω to meet the IR drop requirement.

Table 24. Additional DPLL LC Filter Component Example

Component	Manufacturer	Part No.	Description
Capacitor	KEMET	T495D336MD16AS	33 □F ±20%, 16VDC, ESR=0.225 Ω @ 100 kHz, ESL=2.5 nH
Inductor	muRATA	LQG21NR10K10	100 nH ±10%, 250 mA, Max dc resistance = 0.26 Ω, size=0805, magnetically shielded

As an example, Figure 65 is a Bode plot showing the frequency response using the capacitor and inductor values shown in Table 25. The capacitor and inductor values were held constant while the resistance was swept for four different combinations of resistance (the resistance of the discrete/trace resistor and the resistance of the inductor), each resulting in a different series resistance. In addition, different values for the resistance of the inductor were assumed based on its max and typical DC resistance. This is summarized in Table 25. This yielded the four different frequency response curves shown in Figure 65.

Figure 65. Frequency Response (see Table 25)

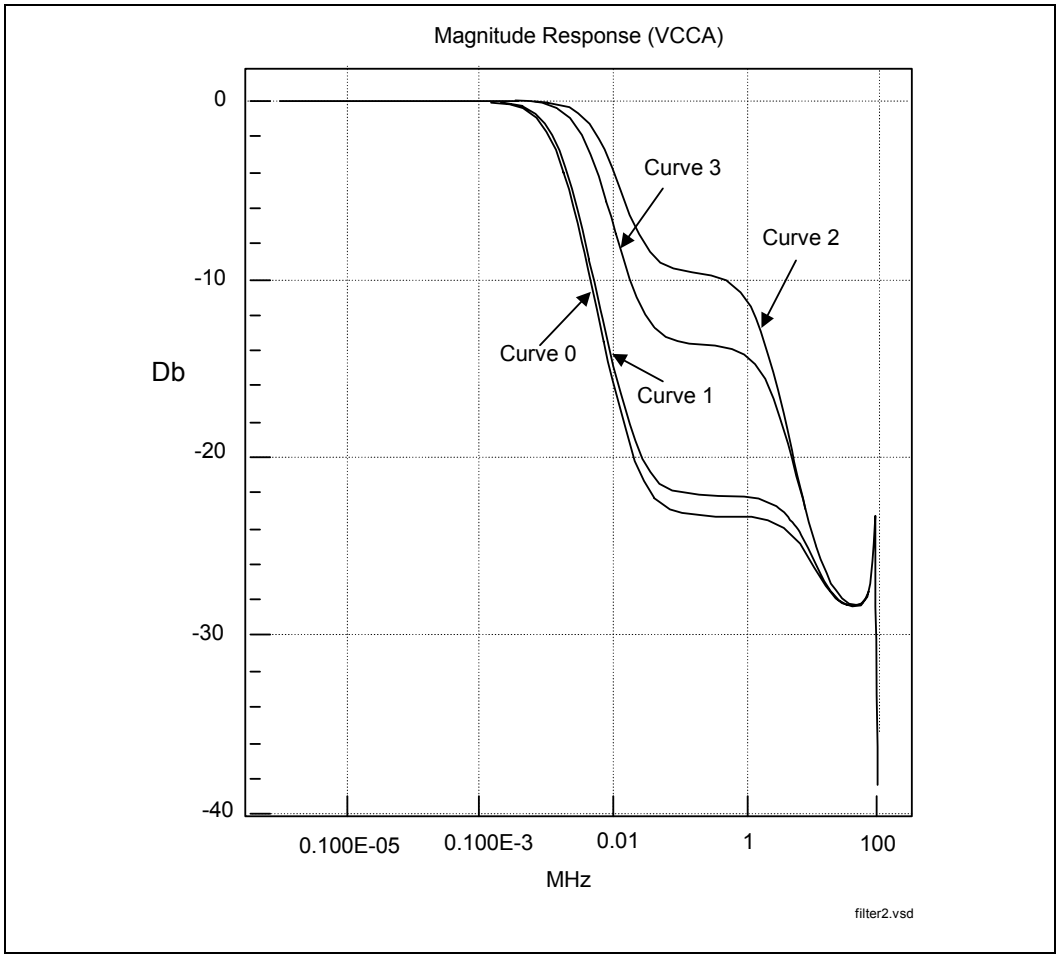


Table 25. Resistance Values for Frequency Response Curves

Curve	RTRACE + RDISCRETE	RIND
0	2.2 Ω	0.8 Ω
1	2.2 Ω	0.4 Ω
2	0 Ω	0.4 Ω
3	0 Ω	0.8 Ω

As series resistance (R_{TRACE} + $R_{DISCRETE}$ + R_{IND}) increases, the filter response (i.e., attenuation in PLL bandwidth) improves. There is a limit of 3.3 Ω total series resistance of the filter to limit DC voltage drop.

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7 Clocking

7.1 Clock Generation

There is only one clock generator component required in an 810E chipset system. The CK810E clock chip is pin compatible with the CK810 clock chip, which comes in a single 56-pin SSOP package.

There is one pin function change in the CK810E relative to the CK810, the REFCLK Reset Strap:

Table 26. REFCLK Reset Strap for CK810 vs. CK810E

At reset	APIC Clock Strap	System Bus Freq Select (SEL1)
After reset	14 MHz Clock	14 MHz Clock
Reset default	Internal Pull-up for 33 MHz APIC Clock Populate External 10 kΩ Resistor to Ground for 16 MHz	Internal Pull-down for 66 MHz or 100 MHz Bus Freq Select (SEL0) External Drive to 1 to Select 133 MHz System Bus

The CK810E is a mixed voltage component. Some of the output clocks are 3.3V and some of the output clocks are 2.5V. As a result, the CK810E device requires both 3.3V and 2.5V. These power supplies should be as clean as possible. Noise in the power delivery system for the clock driver can cause noise on the clock lines. The CK810E provides the clock frequencies indicated in Table 27.

Table 27. Intel® 810E Chipset Clocks (2-DIMM)

Number	Clock	Frequency
3	Processor Clocks	66/100/133 MHz
9	SDRAM Clocks	100 MHz
8	PCI Clocks	33 MHz
2	APIC Clocks	16.67/33 MHz
2	48 MHz Clocks	48 MHz
2	3V66 MHz Clocks	66 MHz
1	REF Clock	14.31818 MHz

The DCLKREF signal from the external clock synthesizer to the GMCH is a 48 MHz signal. This signal has no length requirements, except those specified in the Design Guide. However, care in routing this signal relative to the DIMM slots is important. Future board designs should attempt to route the DCLKREF trace so that the trace is not parallel to the DIMM slots or does not pass underneath the DIMM slots. This prevents noise coupling of memory-related signals into the 48 MHz clock signal.

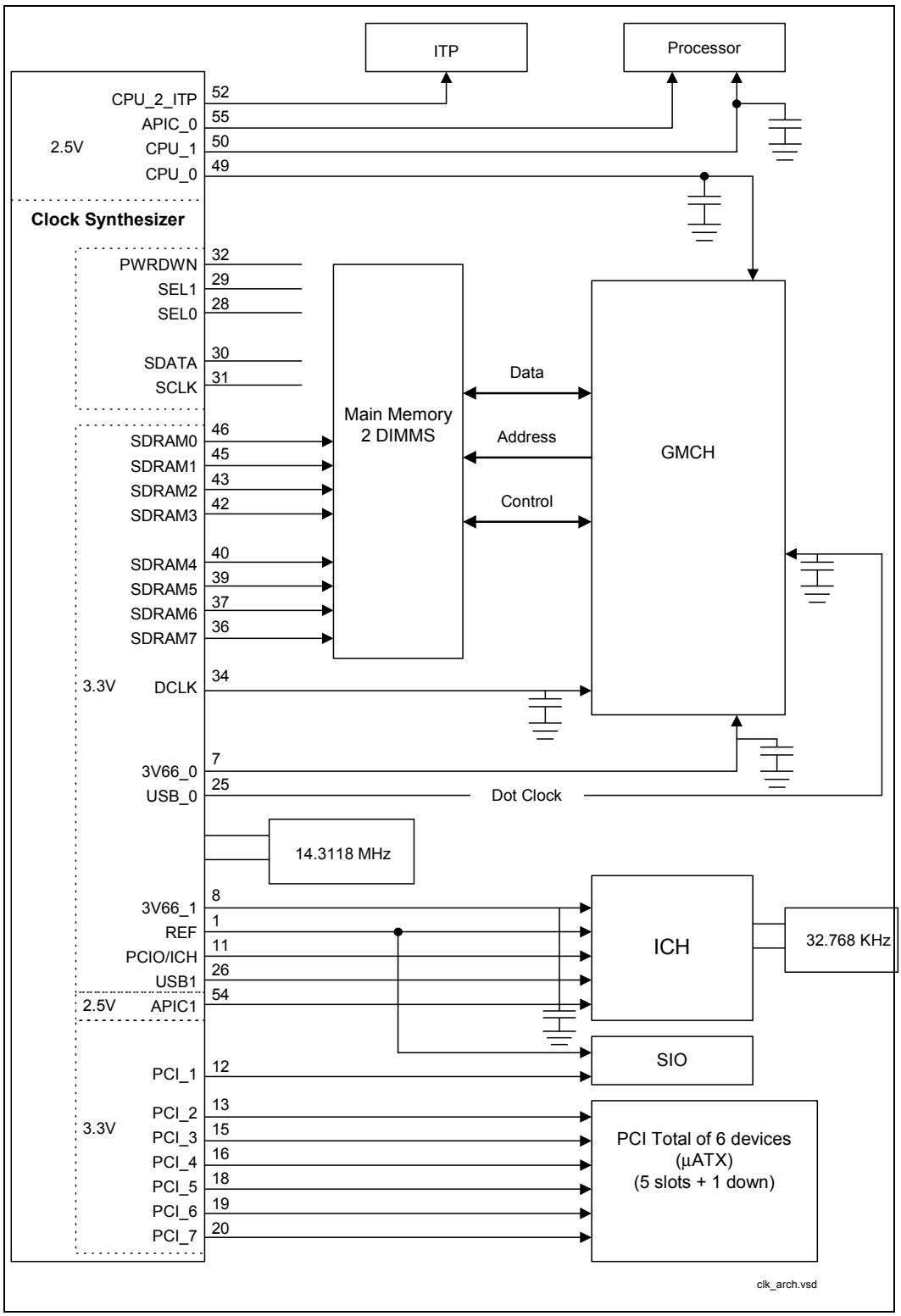
Features (56 Pin SSOP Package)

- Three copies of processor clock 66/100/133 MHz (2.5V) (Processor, GMCH, ITP)
- Nine copies of 100 MHz (all the time) SDRAM clock (3.3V) (SDRAM[0:7], DClk)
- Eight copies of PCI clock (33 MHz) (3.3V)
- Two copies of APIC clock @16.67 MHz or 33 MHz, synchronous to processor clock (2.5V)
- Two copy of 48 MHz clock (3.3V) [Non SSC]
- Two copies of 3V66 MHz clock (3.3V)
- One copy of REF clock @14.31818 MHz (3.3V) also used as input strap to determine APIC frequency
- 66/100/133 MHz processor operation (selectable at power up only)
- Ref. 14.31818 MHz Xtal oscillator input
- Power Down Pin
- Spread spectrum support
- I^2C Support for turning off unused clocks

7.2 Clock Architecture

The Intel 810E chipset clock architecture is illustrated in Figure 66.

Figure 66. Intel® 810E Chipset Clock Architecture



7.3 Clock Routing Guidelines

Table 28 shows the group skew and jitter limits.

Table 28. Group Skew and Jitter Limits at the Pins of the Clock Chip

Signal Group	Pin-Pin Skew	Cycle-Cycle Jitter	Nominal Vdd	Skew, Jitter Measure Point
Processor	175 ps	250 pS	2.5V	1.25V
SDRAM	250 ps	250 pS	3.3V	1.50V
APIC	250 ps	500 pS	2.5V	1.25V
48 MHz	250 ps	500 pS	3.3V	1.50V
3V66	175 ps	500 pS	3.3V	1.50V
PCI	500 ps	500 pS	3.3V	1.50V
REF	N/A	1000 pS	3.3V	1.50V

Table 29 shows the signal group and resistor tolerance.

Table 29. Signal Group and Resistor

Signal Group	Resistor
Processor	33 Ω ± 5%
SDRAM	22 Ω ± 5%
DCLK	33 Ω ± 5%
3V66	22 Ω ± 5%
PCI	33 Ω ± 5%
TCLK	22 Ω ± 5%
OCLK/RCLK	33 Ω ± 5%
48 MHz	33 Ω ± 5%
APIC	33 Ω ± 5%
REF	10 Ω ± 5%

Table 30 shows the layout dimensions for the clock routing.

Note: All the clock signals must be routed on the same layer which reference to a ground plane.

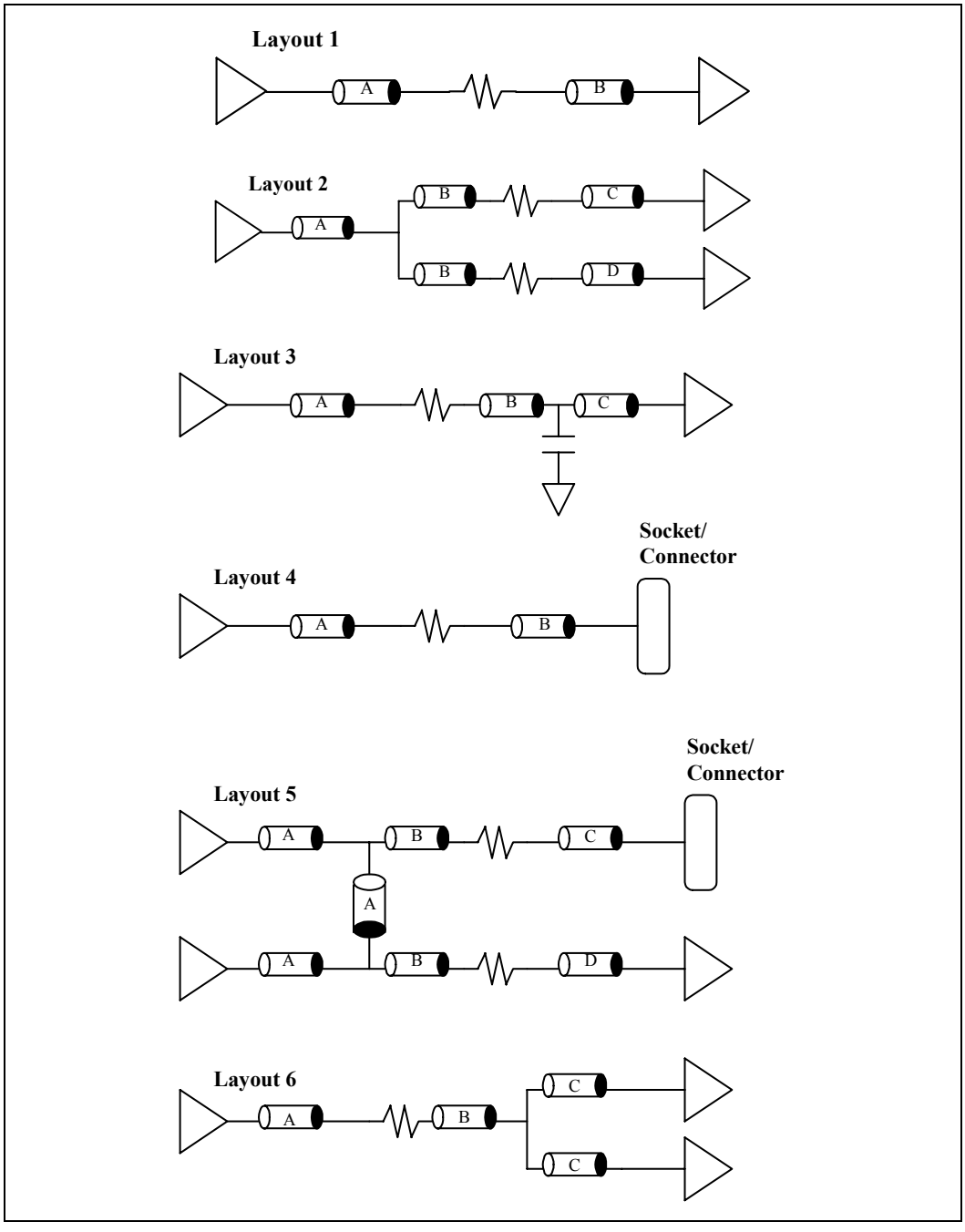
Table 30. Layout Dimensions

Group	Receiver	Resistor	Cap	Topology	A	B	C	D
MCLK	DIMM	22 Ω	N/A	Layout 1	0.5”	X	N/A	N/A
Processor: Pentium III FC-PGA Processor 100/133 MHz	Segment C => Pentium III FC-PGA Processor Segment D => GMCH	33 Ω	N/A	Layout 5	0.1”	0.5”	X+4.8"	X+7.1”
Processor: Celeron® processor 66/100 MHz	Segment C => Celeron processor socket Segment D => GMCH	33 Ω	N/A	Layout 5	0.1”	0.5”	X+5.4"	X+7.1”
DCLK	GMCH	33 Ω	22 pF	Layout 3	0.5”	X+3.2”	0.5”	N/A
3V66	GMCH	22 Ω	18 pF	Layout 3	0.5”	X+1.4”	0.5”	N/A
3V66	ICH	22 Ω	18 pF	Layout 3	0.5”	X+1.4”	0.5”	N/A
PCI	PCI device	33 Ω	N/A	Layout 1	0.5”	X+3.0” to X+9.3”	N/A	N/A
PCI	PCI socket	33 Ω	N/A	Layout 4	0.5”	X+0.0” to X+6.0”	N/A	N/A
PCI	ICH	33 Ω	N/A	Layout 1	0.5”	X+4.4”	N/A	N/A
TCLK	SDRAM	22 Ω	N/A	Layout 6	0.5”	1.5” to 2.5”	0.75” to 1.25”	N/A
OCLK/RCLK	GMCH	33 Ω	N/A	Layout 1	0.5”	3.25” to 3.75”	N/A	N/A
APIC	PPGA	33 Ω	N/A	Layout 4	0.5”	Y	N/A	N/A
APIC	ICH	33 Ω	N/A	Layout 1	0.5”	Y+2.4”	N/A	N/A

NOTES:
1. W, X, Y and Z trace lengths are arbitrary. Below are some suggested values: X=5.0 inches, Y=4.2 inches.

Figure 67 shows the different topologies used for the clock routing guidelines.

Figure 67. Different Topologies for the Clock Routing Guidelines

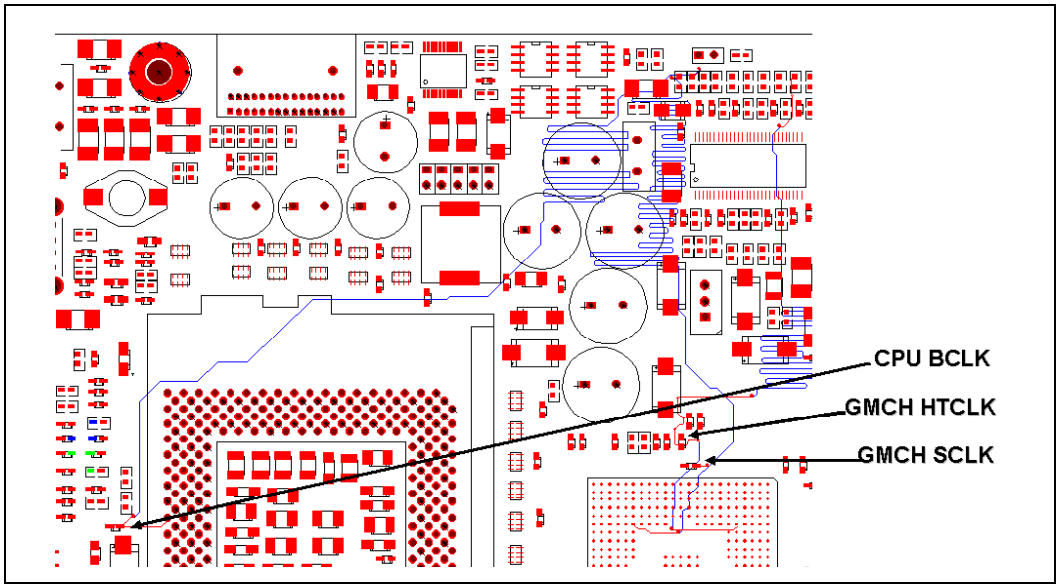


7.4 Capacitor Sites

Intel recommends 0603 package capacitor sites placed as close as possible to the clock input receivers for AC tuning for the following signal groups:

- GMCH
- Processor
- SDRAM/DCLK
- 3V66
- 3V66 to the ICH

Figure 68. Example of Capacitor Placement Near Clock Input Receiver



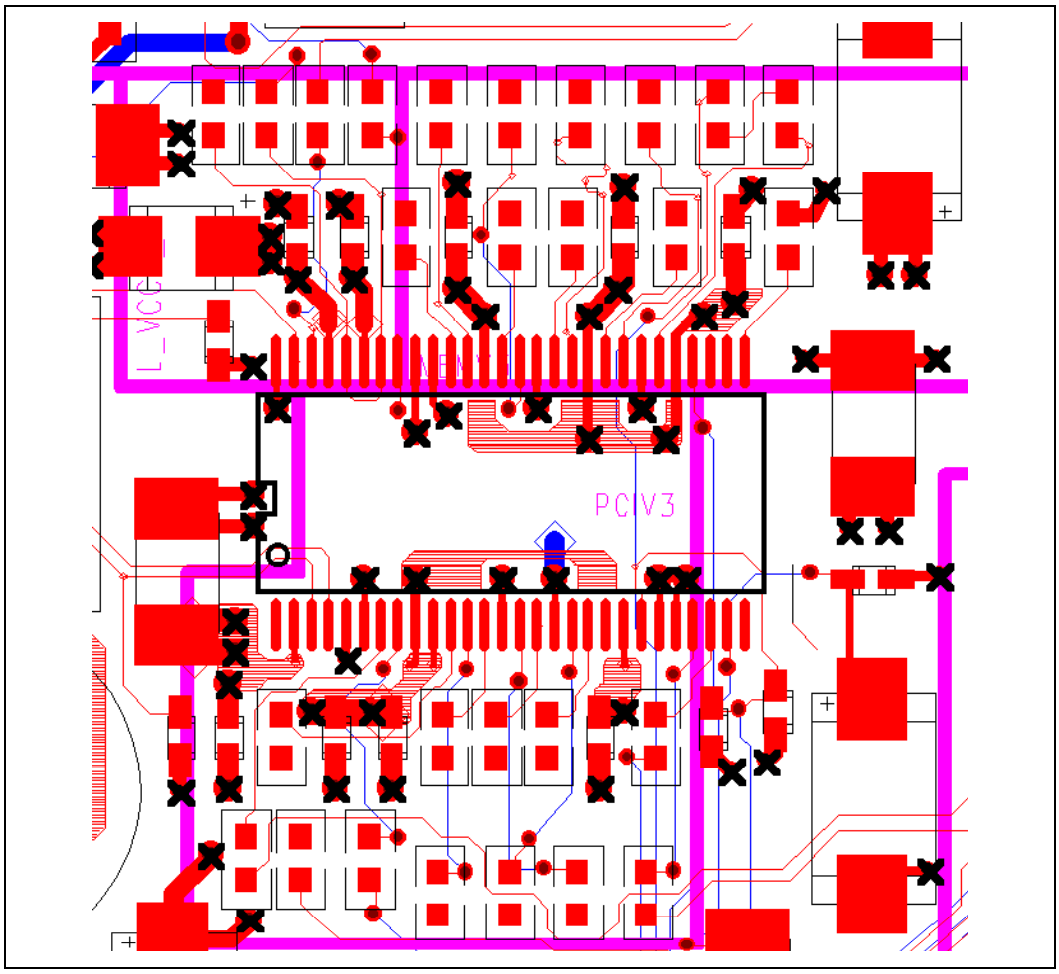
7.5 Clock Power Decoupling Guidelines

Several general layout guidelines should be followed when laying out the power planes for the CK810E clock generator.

- Isolate power planes to the each of the clock groups.
- Place local decoupling as close to power pins as possible and connect with short, wide traces and copper.
- Connect pins to appropriate power plane with power vias (larger than signal vias).
- Bulk decoupling should be connected to plane with 2 or more power vias.
- Minimize clock signal routing over plane splits.
- Do not route any signals underneath the clock generator on the component side of the board.
- An example signal via is a 14 mil finished hole with a 24–26 mil path. An example power via is an 18 mil finished hole with a 33–38 mil path. For large decoupling or power planes with large current transients it is recommended to use a larger power via.

An example of clock power layout is presented in Figure 69.

Figure 69. Example of Clock Power Plane Splits and Decoupling



7.6 Clock Skew Requirements

To ensure correct system functionality, certain clocks must maintain a skew relationship to other clocks as summarized in Section 7.6.1.

7.6.1 IntraGroup Skew Limits

Clocks within each group must maintain appropriate skew relationship to each other. These requirements are summarized in Table 31.

Table 31. Clock Skew Requirements

Group Pair	Skew Limit	Measurement Point of Receiver
Processor BCLK to GMCH HTCLK	350 ps window	Pin on top of PPGA PKG GMCH Ball
GMCH SCLK to DIMM Clocks	±630 ps Referenced to GMCH SCLK	GMCH Ball DRAM Component Pin on Module
GMCH HubCLK to ICH HubCLK	575 ps window	GMCH Ball ICH Ball

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8 Power Delivery

This chapter contains power delivery guidelines. Table 32 provides definitions for power delivery terms used in this chapter.

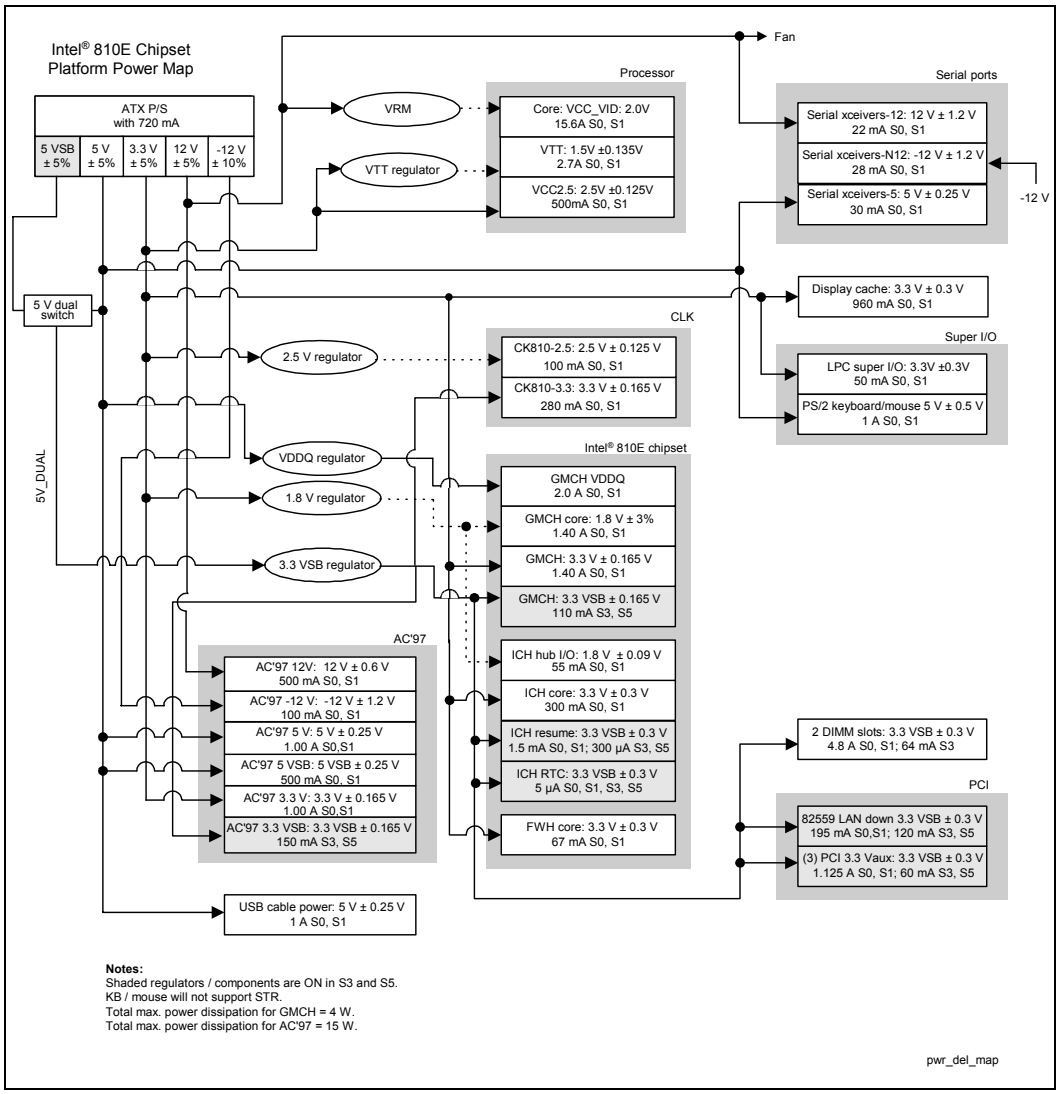
Table 32. Power Delivery Definitions

Term	Description
Suspend-To-RAM (STR)	In the STR state, the system state is stored in main memory and all unnecessary system logic is turned off. Only main memory and logic required to wake the system remain powered. This state is used in the Customer Reference Board (CRB) to satisfy the S3 ACPI power management state.
Full-power operation	During full-power operation, all components on the motherboard remain powered. Note that full-power operation includes both the full-on operating state and the S1 (CPU stop-grant state) state.
Suspend operation	During suspend operation, power is removed from some components on the motherboard. The CRB supports two suspend states: Suspend-to-RAM (S3) and Soft-off (S5).
Power rails	An ATX power supply has 6 power rails: +5V, -5V, +12V, -12V, +3.3V, 5VSB. In addition to these power rails, several other power rails are created with voltage regulators on the CRB.
Core power rail	A power rail that is only on during full-power operation. These power rails are on when the PSON signal is asserted to the ATX power supply. The core power rails that are distributed directly from the ATX power supply are: ± 5V, ±12V and +3.3V.
Standby power rail	A power rail that in on during suspend operation (these rails are also on during full-power operation). These rails are on at all times (when the power supply is plugged into AC power). The only standby power rail that is distributed directly from the ATX power supply is: 5VSB (5V Standby). There are other standby rails that are created with voltage regulators on the motherboard.
Derived power rail	A derived power rail is any power rail that is generated from another power rail. For example, 3.3VSB is usually derived (on the motherboard) from 5VSB using a voltage regulator (on the CRB, 3.3VSB is derived from 5V_DUAL).
Dual power rail	A dual power rail is derived from different rails at different times (depending on the power state of the system). Usually, a dual power rail is derived from a standby supply during suspend operation and derived from a core supply during full-power operation. Note that the voltage on a dual power rail may be misleading.

Figure 70 shows the power delivery architecture for an example 810E chipset universal platform-based system. This power delivery architecture supports the “Instantly Available PC Design Guidelines” via the suspend-to-RAM (STR) state. During STR, only the necessary devices are powered. These devices include: main memory, the ICH resume well, PCI wake devices (via 3.3 Vaux), AC’97, and optionally USB. (USB can be powered only if sufficient standby power is available.) To ensure that enough power is available during STR, a thorough power budget should be completed. The power requirements should include each device’s power requirements, both in suspend and in full power. The power requirements should be compared with the power budget supplied by the power supply. Due to the requirements of main memory and the PCI 3.3 Vaux (and possibly other devices in the system), it is necessary to create a dual power rail.

The solutions in this Design Guide are only examples. Many power distribution methods achieve the similar results. When deviating from these examples, it is critical to consider the effect of a change.

Figure 70. Power Delivery Map



In addition to the power planes provided by the ATX power supply, an **instantly available** 810E chipset for use with universal socket 370 platform (using Suspend-to-RAM) requires six power planes to be generated on the board. The requirements for each power plane are documented in this section. In addition to on-board voltage regulators, the CRB will have a 5V Dual Switch.

5V Dual Switch

This switch will power the 5V Dual plane from the 5V core ATX supply during full-power operation. During Suspend-to-RAM, the 5V Dual plane will be powered from the 5V Standby power supply. Note: the voltage on the 5V Dual plane **is not 5V!** There is a resistive drop through the 5V Dual Switch that must be considered. Therefore, NO COMPONENTS should be connected directly to the 5V Dual plane. On the CRB, the only devices connected to the 5V Dual plane are voltage regulators (to regulate to lower voltages).

Note: This switch is not required in an Intel 810E chipset for use with universal socket 370 platform that does not support Suspend-to-RAM (STR).

VTT

This power plane is used to power the AGTL/AGTL+ termination resistors. Refer to the latest revisions of the Pentium III processor (CPUID=068xh) and Celeron processor (CPUID=068xh) datasheets.

Note: This regulator is required in ALL designs.

1.8V

The 1.8V plane powers the GMCH core and the ICH hub interface I/O buffers. This power plane has a total power requirement of approximately 1.7A. The 1.8V plane should be decoupled with a 0.1 µF and a 0.01 µF chip capacitor at *each* corner of the GMCH and with a single 1 µF and 0.1 µF capacitor at the ICH.

Note: This regulator is required in ALL designs.

VDDQ

The VDDQ plane is used to power the GMCH AGP interface and the graphics component AGP interface. Refer to the AGP Interface Specification Revision 2.0 (http://www.agpforum.org) and ECR#43 and ECR#44 for specific VDDQ delivery requirements.

For the consideration of component long-term reliability, the following power sequence is strongly recommended while the AGP interface of GMCH is running at 3.3V. If the AGP interface is running at 1.5V, the following power sequence recommendation is no longer applicable. The power sequence recommendations are:

- During the power-up sequence, the 1.8V must ramp up to 1.0V **Before** 3.3V ramps up to 2.2V
- During the power-down sequence, the 1.8V CAN NOT ramp below 1.0V **Before** 3.3V ramps below 2.2V
- The same power sequence recommendation also applies to the entrance and exit of S3 state, since MCH power is compete off during the S3 state.

Refer to Section 8.3.2 for more information on the power ramp sequence requirement between 3.3V and 1.8V. System designers need to be aware of this requirement while designing the voltage regulators and selecting the power supply. For further details on the voltage sequencing

requirements, refer to the *Intel® 810E Chipset Family: 82810E Graphics and Memory Controller Hub (GMCH) Datasheet*.

3.3VSB

The 3.3VSB plane powers the I/O buffers in the resume well of the ICH and the PCI 3.3Vaux suspend power pins. The 3.3Vaux requirement state that during suspend, the system must deliver 375 mA to each *wake-enabled* card and 20 mA to each *non wake-enabled* card. During *full-power* operation, the system must be able to supply 375 mA to each card. Therefore, the total current requirement is:

- *Full-power Operation:* 375 mA * number of PCI slots
- *Suspend Operation:* 375 mA + 20 mA * (number of PCI slots – 1)

In addition to the PCI 3.3Vaux, the ICH suspend well power requirements must be considered as shown in Figure 70.

Note: This regulator is required in ALL designs.

1.8VSB

The 1.8VSB plane powers the logic to the resume well of the ICH. This should not be used for VCMOS.

8.1 Thermal Design Power

The Thermal Design power (TDP) is defined as the estimated maximum possible expected power generated in a component by a realistic application. It is based on extrapolations in both hardware and software technology over the life of the product. It does not represent the expected power generated by a power virus.

The TDP of the 82810E GMCH component is 4.0W.

8.1.1 Pull-up and Pull-down Resistor Values

The pull-up and pull-down values are system dependent. The appropriate value for a system can be determined from an AC/DC analysis of the pull-up voltage used, the current drive capability of the output driver, the input leakage currents of all devices on the signal net, the pull-up voltage tolerance, the pull-up/pull-down resistor tolerance, the input high-voltage/low-voltage specifications, the input timing specifications (RC rise time), etc. Analysis should be performed to determine the minimum/maximum values usable on an individual signal. Engineering judgment should be used to determine the optimal value. This determination can include cost concerns, commonality considerations, manufacturing issues, specifications, and other considerations.

A simplistic DC calculation for a pull-up value is:

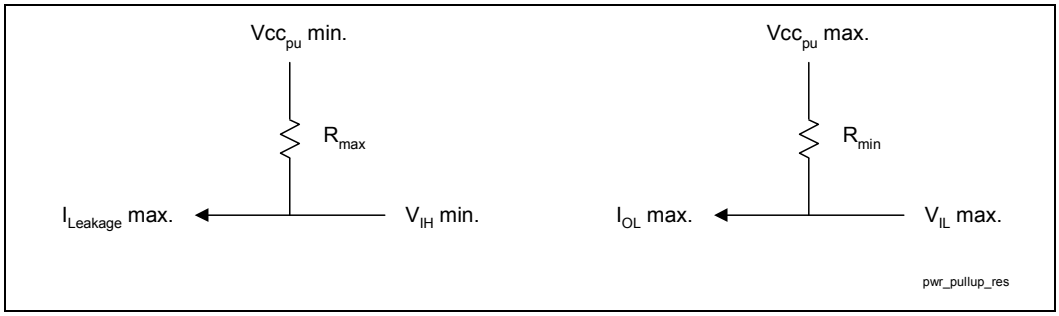
$$R_{MAX} = (Vcc_{PU}\ MIN - V_{IH}\ MIN) / I_{LEAKAGE}\ MAX$$

$$R_{MIN} = (Vcc_{PU}\ MAX - V_{IL}\ MAX) / I_{OL}\ MAX$$

Since $I_{LEAKAGE}$ MAX is normally very small, R_{MAX} may not be meaningful. R_{MAX} also is determined by the maximum allowable rise time. The following calculation allows for t, the maximum allowable rise time, and C, the total load capacitance in the circuit, including the input capacitance of the devices to be driven, the output capacitance of the driver, and the line capacitance. This calculation yields the largest pull-up resistor allowable to meet the rise time t.

$$R_{MAX} = -t / (C * \ln(1-(V_{IH}\ MIN / Vcc_{PU}\ MIN)))$$

Figure 71. Pull-up Resistor Example



8.2 ATX Power Supply PWRGOOD Requirements

The PWROK signal must be glitch free for proper power management operation. The ICH sets the PWROK_FLR bit (ICH GEN_PMCON_2, General PM Configuration 2 Register, PM-dev31: function 0, bit 0, at offset A2h). If this bit is set upon resume from S3 powerdown, the system will reboot and control of the system will not be given to the program running when entering the S3 state. System designers should insure that PWROK signal designs are glitch free.

8.3 Power Management Signals

- A power button is required by the ACPI specification.
- PWRBTN# is connected to the front panel on/off power button. The ICH integrates 16 ms debouncing logic on this pin.
- AC power loss circuitry has been integrated into the ICH to detect power failure.
- It is recommended that the ATXPWROK signal from the power supply connector be routed through a Schmitt trigger to square off and maintain its signal integrity. It should not be connected directly to logic on the board.
- PWROK logic from the power supply connector can be powered from the core voltage supply.
- RSMRST# logic should be powered by a standby supply, while making sure that the input to the ICH is at the 3 V level. The RSMST# signal requires a minimum time delay of 1 ms from the rising edge of the standby power supply voltage. A Schmitt trigger circuit is recommended to drive the RSMRST# signal. To provide the required rise time, the 1 ms delay should be placed before the Schmitt trigger circuit. The reference design implements a 20 ms delay at the input of the Schmitt trigger to ensure that the Schmitt trigger inverters have sufficiently powered up before switching the input. Also, ensure that voltage on RSMRST# does not exceed VCC (RTC).
- It is recommended that 3.3 V logic be used to drive RSMRST# to alleviate rise time problems when using a resistor divider from VCC5.
- The PWROK signal to the chipset is a 3 V signal.
- The core well power valid to PWROK asserted at the chipset is a minimum of 1 ms.
- PWROK to the chipset must be deasserted after RSMRST#.
- PWRGOOD signal to processor is driven with an open-collector buffer pulled up to 2.5 V, using a 330 Ω resistor.
- RI# can be connected to the serial port if this feature is used. To implement ring indicate as a wake event, the RS232 transceiver driving the RI# signal must be powered when the ICH suspend well is powered. This can be achieved with a serial port transceiver powered from the standby well that implements a shutdown feature.
- SLP_S3# from the ICH must be inverted and then connected to PSON of the power supply connector to control the state of the core well during sleep states.
- For an ATX power supply, when PSON is Low, the core wells are turned on. When PSON is high, the core wells from the power supply are turned off.

8.3.1 Power Button Implementation

The following items should be considered when implementing a power management model for a desktop system. The power states are as follows:

S1 – Stop Grant – (processor context not lost)

S3 – STR (Suspend to RAM)

S4 – STD (Suspend to Disk)

S5 – Soft-off

- Wake: Pressing the power button wakes the computer from S1–S5.
- Sleep: Pressing the power button signals software/firmware in the following manner:
- If SCI is enabled, the power button will generate an SCI to the OS.
  - The OS will implement the power button policy to allow orderly shutdowns.
  - Do not override this with additional hardware.
- If SCI is not enabled:
  - Enable the power button to generate an SMI and go directly to soft-off or a supported sleep state.
  - Poll the power button status bit during POST while SMIs are not loaded and go directly to soft-off if it gets set.
  - Always install an SMI handler for the power button that operates until ACPI is enabled.
- Emergency Override: Pressing the power button for 4 seconds goes directly to S5.
  - This is only to be used in EMERGENCIES when system is not responding.
  - This will cause the user data to be lost in most cases.
- Do not promote pressing the power button for 4 seconds as the normal mechanism to power the machine off. This violates ACPI.
- To be compliant with the latest PC9x specification, machines must appear to the user to be off when in the S1–S4 sleeping states. This includes:
  - All lights, except a power state light, must be off.
  - The system must be inaudible: silent or stopped fan, drives off.

Note: Contact Microsoft for the latest information concerning PC9x and Microsoft Logo programs.

8.3.2 1.8V/3.3V Power Sequencing

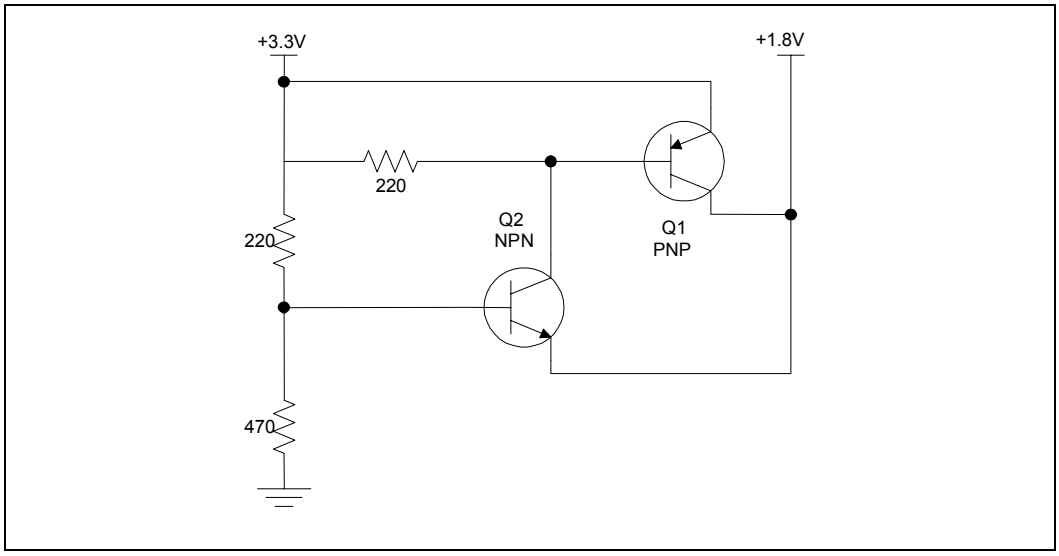
The ICH has two pairs of associated 1.8V and 3.3V supplies. These are {VCC1.8, VCC3.3} and {VCCSus1_8, VCCSus3_3}. These pairs are assumed to power up and power down together. **The difference between the two associated supplies must never be greater than 2.0V.** The 1.85V supply may come up before the 3.3V supply without violating this rule (though this is generally not practical in a desktop environment, since the 1.8V supply is typically derived from the 3.3V supply by means of a linear regulator).

One serious consequence of violation of this "2V Rule" is electrical overstress of oxide layers, resulting in component damage.

The majority of the ICH I/O buffers are driven by the 3.3V supplies, but are controlled by logic that is powered by the 1.8V supplies. Thus, another consequence of faulty power sequencing arises if the 3.3V supply comes up first. In this case the I/O buffers will be in an undefined state until the 1.8V logic is powered up. Some signals that are defined as "Input-only" actually have output buffers that are normally disabled, and the ICH may unexpectedly drive these signals if the 3.3V supply is active while the 1.8V supply is not.

Figure 72 shows an example power-on sequencing circuit that ensures the “2V Rule” is obeyed. This circuit uses a NPN (Q2) and PNP (Q1) transistor to ensure the 1.8V supply tracks the 3.3V supply. The NPN transistor controls the current through PNP from the 3.3V supply into the 1.8V power plane by varying the voltage at the base of the PNP transistor. By connecting the emitter of the NPN transistor to the 1.8V plane, current will not flow from the 3.3V supply into 1.8V plane when the 1.8V plane reaches 1.8V.

Figure 72. Example 1.8V/3.3V Power Sequencing Circuit



When analyzing systems that may be "marginally compliant" to the 2V Rule, please pay close attention to the behavior of the ICH's RSMRST# and PWROK signals, since these signals control internal isolation logic between the various power planes:

- RSMRST# controls isolation between the RTC well and the Resume wells.
- PWROK controls isolation between the Resume wells and Main wells

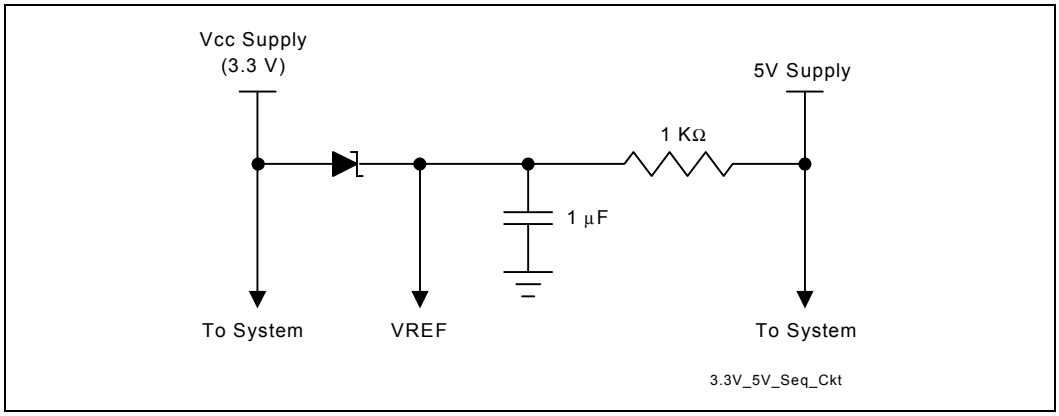
If one of these signals goes high while one of its associated power planes is active and the other is not, a leakage path will exist between the active and inactive power wells. This could result in high, possibly damaging, internal currents.

8.3.3 3.3V/V5REF Sequencing

V5REF is the reference voltage for 5V tolerance on inputs to the ICH. V5REF must be powered up before or simultaneously to VCC3.3. It must also power down after or simultaneous to VCC3.3. The rule must be followed in order to ensure the safety of the ICH. If the rule is violated, internal diodes will attempt to draw power sufficient to damage the diodes from the VCC3.3 rail. Figure 73 shows a sample implementation of how to satisfy the V5REF/3.3V sequencing rule.

This rule also applies to the stand-by rails, but in most platforms, the VCCSus3_3 rail is derived from the VCCSus5 and therefore, the VCCSus3_3 rail will always come up after the VCCSus5 rail. As a result, V5REF_Sus will always be powered up before VCCSus3_3. In platforms that do not derive the VCCSus3_3 rail from the VCCSus5 rail, this rule must be comprehended in the platform design. As an additional consideration, during suspend the only signals that are 5V tolerant are USBOC. If these signals are not needed during suspend, V5REF_Sus can be hooked to the VCCSus3_3 rail.

Figure 73. 3.3V/V5REF Sequencing Circuitry



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9 Design Checklist

9.1 Design Review Checklist

This checklist highlights design considerations that should be reviewed prior to manufacturing a motherboard that implements an 810E chipset universal socket 370 platform. This is not a complete list and does not guarantee that a design will function properly. Beyond the items contained in the following text, refer to the most recent version of the Design Guide for more detailed instructions on designing a motherboard.

9.1.1 Design Checklist Summary

The following tables provide design considerations for the various portions of a design. Each table describes one of those portions, and is titled accordingly. Contact your Intel Field Representative for questions or issues regarding interpretation of the information contained in these tables.

Table 33. AGTL+ Connectivity Checklist for 370-Pin Socket Processors

Processor Pin	I/O	Recommendations
A[35:3]# [1]	I/O	• Connect A[31:3]# to GMCH. Leave A[35:32]# as No Connect (not supported by chipset).
ADS# [1]	I/O	• Connect to GMCH.
AERR#	I/O	• Leave as No Connect (not supported by chipset).
AP[1:0]#	I/O	• Leave as No Connect (not supported by chipset).
BERR#	I/O	• Leave as No Connect (not supported by chipset).
BINIT#	I/O	• Leave as No Connect (not supported by chipset).
BNR# [1]	I/O	• Connect to GMCH.
BP[3:2]#	I/O	• Leave as No Connect.
BPM[1:0]	I/O	• Leave as No Connect.
BPRI# [1]	I	• Connect to GMCH.
BREQ[0]# (BR0#)	I/O	• 10 Ω pull-down resistor to ground.
D[63:0]# [1]	I/O	• Connect to GMCH.
DBSY# [1]	I/O	• Connect to GMCH.
DEFER# [1]	I	• Connect to GMCH.
DEP[7:0]#	I/O	• Leave as No Connect (not supported by chipset).
DRDY# [1]	I/O	• Connect to GMCH.
HIT# [1]	I/O	• Connect to GMCH.

Processor Pin	I/O	Recommendations
HITM# [1]	I/O	• Connect to GMCH.
LOCK# [1]	I/O	• Connect to GMCH.
REQ[4:0]# [1]	I/O	• Connect to GMCH.
RESET#	I	• 56 Ω pull-up resistor to VTT, connect to GMCH, 240 Ω series resistor to ITP.
RESET2# [2]	I	• Driven by same signal as RESET#.
RP#	I/O	• Leave as No Connect (not supported by chipset).
RS[2:0]#	I	• Connect to GMCH.
RSP#	I	• Leave as No Connect (not supported by chipset).
TRDY# [1]	I	• Connect to GMCH.

Table 34. CMOS Connectivity Checklist for 370-Pin Socket Processors

Processor Pin	I/O	Recommendations
A20M#	I	• 150 Ω pull-up resistor to VCC_{CMOS} / Connect to ICH.
FERR#	O	• 150 Ω pull-up resistor to VCC_{CMOS} / Connect to ICH.
FLUSH#	I	• 150 Ω pull-up resistor to VCC_{CMOS} (not used by chipset).
IERR#	O	• 150 Ω pull-up resistor to VCC_{CMOS} if tied to custom logic or leave as No Connect (not used by chipset).
IGNNE#	I	• 150 Ω pull-up resistor to VCC_{CMOS} / Connect to ICH.
INIT#	I	• 150 Ω pull-up resistor to VCC_{CMOS} / Connect to ICH & FWH.
LINT0/INTR	I	• 150 Ω pull-up resistor to VCC_{CMOS} / Connect to ICH.
LINT1/NMI	I	• 150 Ω pull-up resistor to VCC_{CMOS} / Connect to ICH.
PICD[1:0]	I/O	• 150 Ω pull-up resistor to VCC_{CMOS} / Connect to ICH.
PREQ#	O	• ~200–330 Ω pull-up resistor to VCC_{CMOS} / Connect to ITP.
PWRGOOD	I	• 150–330 Ω pull-up to 2.5V, output from the PWRGOOD logic.
SLP#	I	• 150 Ω pull-up resistor to VCC_{CMOS} / Connect to ICH.
SMI#	I	• 150 Ω pull-up resistor to VCC_{CMOS} / Connect to ICH.
STPCLK#	I	• 150 Ω pull-up resistor to VCC_{CMOS} / Connect to ICH.
THERMTRIP#	O	• 150 Ω pull-up resistor to VCC_{CMOS} and connect to power off logic, or leave as No Connect.

Table 35. TAP Checklist for a 370-Pin Socket Processor

Processor Pin	I/O	Recommendations
TCK	I	• 39 Ω pull-down resistor to ground / Connect to ITP.
TDI	I	• 200–330 Ω pull-up resistor to VCC_{CMOS} / Connect to ITP.
TDO	O	• 150 Ω pull-up resistor to VCC_{CMOS} / Connect to ITP.
TMS	I	• 39 Ω pull-up resistor to VCC_{CMOS} / Connect to ITP.
TRST#	I	• 500- 680 Ω pull-down resistor to ground / Connect to ITP.
PRDY#	I	• Pull-up resistor that matches GTL characteristic impedance to VTT / 240 Ω series resistor to ITP.

NOTES:
1. The ITP connector is different than the one previously specified for other Intel IA-32 processors. It is the female counterpart to the previously specified connector and is specifically for use with processors utilizing 1.5V CMOS TAP I/O signals.
2. The Pentium III processor requires an ITP with a 1.5V tolerant buffer board. Previous ITPs are designed to work higher voltages and may damage the processor if they are connected to an Pentium III processor.

Table 36. Miscellaneous Checklist for 370-Pin Socket Processors

Processor Pin	I/O	Recommendations
BCLK	I	• Connect to clock generator / 22–33 Ω series resistor (though OEM needs to simulate based on driver characteristics). To reduce pin-to-pin skew, tie host clock outputs together at the clock driver then route to the GMCH and processor.
BSEL0	I/O	• **Case 1, 66/100/133 MHz support:** 1 kΩ pull-up resistor to 3.3V, connect to CK810E SEL0 input, connect to GMCH LMD29 pin via 10 kΩ series resistor. • **Case 2, 100/133 MHz support:** 1 kΩ pull-up resistor to 3.3V, connect to PWRGOOD logic such that a logic low on BSEL0 negates PWRGOOD.
BSEL1	I/O	• 1 kΩ pull-up resistor to 3.3V, connect to CK810E REF pin via 10 kΩ series resistor, connect to GMCH LMD13 pin via 10 kΩ series resistor.
CLKREF	I	• Connect to divider on VCC2.5 or VCC3.3 to create 1.25V reference with a 4.7 µF decoupling capacitor. Resistor divider must be created from 1% tolerance resistors. **Do not use VTT as source voltage for this reference!**
CPUPRES#		• Tie to ground, leave as No Connect, or could be connected to PWRGOOD logic to gate system from powering on if no processor is present. If used, 1 kΩ–10 kΩ pull-up resistor to any voltage.
EDGCTRL	I	• 51 Ω ±5% pull-up resistor to VCC_{CORE}.
PICCLK	I	• Connect to clock generator / 22–33 Ω series resistor (though OEM needs to simulate based on driver characteristics).
PLL1, PLL2	I	• Low pass filter on VCC_{CORE} provided on motherboard. Typically a 4.7 uH inductor in series with VCC_{CORE} is connected to PLL1 then through a series 33 µF capacitor to PLL2.
RTTCTRL5[1] (S35)		• 110 Ω ±1% pull-down resistor to ground.
SLEWCTRL (E27)		• 110 Ω ±1% pull-down resistor to ground.

Processor Pin	I/O	Recommendations
THERMDN	O	• No Connect if not used; otherwise connect to thermal sensor using vendor guidelines.
THERMDP	I	• No Connect if not used; otherwise connect to thermal sensor using vendor guidelines.
VCC1.5	I	• Connected to same voltage source as VTT. Must have some high and low frequency decoupling.
VCC2.5	I	• Connected to 2.5V voltage source. Should have some high and low frequency decoupling.
VCC_{CMOS}	O	• Used as pull-up voltage source for CMOS signals between processor and chipset and for TAP signals between processor and ITP. Must have some decoupling (HF/ LF) present.
VCC_{CORE}	I	• 10 ea (min) 4.7 µF in 1206 package all placed within the PGA370 socket cavity. • 8 ea (min) 1 µF in 0612 package placed in the PGA370 socket cavity.
$VCORE_{DET}$ (E21)	O	• For the Intel® Celeron® processor (CPUID=068xh), Pentium III processor (CPUID=068xh), and future 0.13 micron socket 370 processors, $VCORE_{DET}$ must float.
VID[3:0]	O	• Connect to on-board VR or VRM. For on-board VR, 10 kΩ pull-up resistor to power-solution compatible voltage required (usually pulled up to input voltage of the VR). Some of these solutions have internal pull-ups. Optional override (jumpers, ASIC, etc.) could be used. May also connect to system monitoring device.
VID[4]	N/A	• Connect regulator controller pin to ground (not on processor).
VREF[7:0]	I	• Connect to VREF voltage divider made up of 75 Ω and 150 Ω 1% resistors connected to VTT. • Decoupling Guidelines: • Four ea. (min) 0.1 µF in 0603 package placed within 500 mils of VREF pins.
VTT	I	• Connect AH20, AK16, AL13, AL21, AN11, AN15, and G35 to 1.5V regulator. Provide high and low frequency decoupling. • Decoupling Guidelines: — 19 ea (min) 0.1 µF in 0603 package placed within 200 mils of AGTL+ termination resistor packs (r-paks). Use one capacitor for every two (r-paks). — 4 ea (min) 0.47 µF in 0612 package
No Connects	N/A	• The following pins must be left as no-connects: AK30, AM2, F10, G37, L33, N33, N35, N37, Q33, Q35, Q37, R2, W35, X2, Y1

Table 37. GMCH Checklist

Checklist Line Items	Comments
VCCDA	• VCCDA needs to be connected to an isolated power plane.
HCLK, SCLK	• 22 pF capacitor to ground as close as possible to GMCH.
GTLREFA, GTLREFB	• Refer to the latest design guide for the correct GTLREF generation circuit.
HUBREF	• Refer to the latest design guide for the correct HUBREF generation circuit. Also, place a 0.1 µF capacitor as close as possible to GMCH to ground.
IWASTE	• Tie to ground.
IREF	• Place a resistor as close as possible to GMCH and via straight to VSS plane. A 174 Ω 1% resistor is recommended.
LTVCL, LTVDA	• 10 kΩ (approximate) pull-up resistor to 3.3V if digital video out is not implemented.
LTCLK	• Series resistor 22 Ω ± 2%.
OCLK/RCLK	• Series resistor 33 Ω ± 2%.
LMD[27:31] Reset strapping options:	**Strapping options:** For a 1, use a 10 kΩ (approximate) pull-up resistor to 3.3V; a 0 is default (due to internal pull-down resistors). LMD31: 0 = Normal operation 1 = XOR TREE for testing purposes LMD30: 0 = Normal operation 1 = Tri-state mode for testing purposes (will tri-state all signals) LMD29: 0 = System bus frequency = 66 MHz 1 = System bus frequency = 100 MHz LMD28: The value on LMD28 sampled at the rising edge of CPURST# reflects if the IOQD (In-Order Queue Depth) is set to 1 or 4. 0 = IOQD = 4 1 = IOQD = 1 LMD27: The PMOS-Kicker should be “OFF” for either processor. This is accomplished by treating LMD27 the same as any other LMD pin. Do not externally pull it up or down. LMD26: **Set to socket** for Intel® Celeron® processors (CPUID=068xh) and Intel® Pentium® III processors (CPUID=068xh). **Set to slot** for Intel® Pentium® III processors that use 0.13 micron technology. LMD13: 0= LMD29 determines host bus frequency 1= host bus frequency is 133 MHz
HCOMP	• **Option 1—RCOMP Method:** Tie the HCOMP pin to a 40 Ω 1% or 2% (or 39 Ω 1%) pull-up resistor to 1.8V via a 10 mil wide, very short (~0.5 inches) trace. • **Option 2—ZCOMP Method:** The HCOMP pin must be tied to a 10 mil trace that is AT LEAST 18 inches long. This trace must be un-terminated and care should be taken when routing the signal to avoid crosstalk (1520 mil separation between this signal and any adjacent signals is recommended). This signal may not cross power plane splits.

Table 38. System Memory Checklist

Checklist Line Items	Recommendations
Pin 147	• Connect to Ground (since the 810E chipset does not support registered DIMMs).
WP (Pin 81 on the DIMMs)	• Add a 4.7 kΩ pull-up resistor to 3.3V. This is a recommendation to write-protect the DIMM's EEPROM.
MAA[7:4], MAB[7:4]	• Add 10 Ω series resistors to the MAA[7:4], MAB[7:4] as close as possible to GMCH for signal integrity.

Table 39. Display Cache Checklist

Checklist Line Items	Recommendations
CKE	• 4.7 kΩ pull-up resistor to VCC3.

Table 40. ICH Checklist

Checklist Line Items	Comments
PME#, PWRBTN#, LAD[3:0]#/FWH[3:0]#	No external pull-up resistors on those signals with integrated pull-ups.
SPKR	Optional strapping: Internal pull-up resistor is enabled at reset for strapping; after reset, the internal pull-up resistor is disabled. Otherwise, connect to motherboard speaker logic.
AC_SDOUT	Optional strapping: Internal pull-down resistor is enabled at reset for strapping. after reset, the internal pull-down resistor is disabled. Otherwise, connect to AC'97 logic.
AC_BITCLK	Internal pull-down resistor is enabled only when the AC link shut-off bit in the ICH is set. Otherwise, connect to AC'97 logic.
AC_SDIN[1:0]	Internal pull-down resistors are enabled only when the AC link shut-off bit in the ICH is set. Use 10 kΩ (approximate) pull-down resistors on both signals if using AMR. For onboard AC'97 devices, use a 10 kΩ (approximate) pull-down resistor on the signal that is not used. Otherwise, connect to AC'97 logic.
PDD[15:0], PDIOW#, PDIOR#, PDREQ, PDDACK#, PIORDY, PDA[2:0], PDCS1#, PDCS3#, SDD[15:0], SDIOW#, SDIOR#, SDREQ, SDDACK#, SIORDY, SDA[2:0], SDCS1#, SDCS3#, IRQ14, IRQ15	No external series termination resistors on those signals with integrated series resistors.
PCIRST#	The PCIRST# signal should be buffered to the IDE connectors.

Checklist Line Items	Comments
No floating inputs (including bi-directional signals):	Unused core well inputs should be tied to a valid logic level (either pulled up to 3.3V or pulled down to ground). Unused resume well inputs must be either pulled up to 3.3VSB or pulled down to ground. Ensure ALL unconnected signals are OUTPUTS ONLY!
PDD[15:0], SDD[15:0]	PDD7 and SDD7 need a 10 kΩ (approximate) pull-down resistor. No other pull-ups/pull-downs are required. Refer to ATA ATAPI-4 specification.
PIORDY, SDIORDY	Use approximately 1 kΩ pull-up resistor to 5V.
PDDREQ, SDDREQ	Use approximately 5.6 kΩ pull-down resistor to ground.
IRQ14, IRQ15	Need 8.2 kΩ (approximate) pull-up resistor to 5V.
HL11	No pull-up resistor required. A test point or no-stuff resistor is needed to be able to drive the ICH into NAND tree mode for testing purposes.
VccRTC	No Clear CMOS Jumper on VccRTC. Use a jumper on RTCRST# or a GPI, or use a safe-mode strapping for Clear CMOS.
SMBus: SMBCLK SMBDATA	The SMBus signals can be pulled up to VCC3.3 standby. Isolate any devices that are not on the same power plane as the SMBus pull-ups in any states where VCC3.3 standby is on and VCC3.3 is off. The value of the SMBus pull-ups should reflect the number of loads on the bus. For most implementations with 45 loads, 4.7kΩ resistors are recommended. OEMs should conduct simulation to determine exact resistor value.
APICD[0:1], APICCLK	If the APIC is used: 150 Ω (approximate) pull-ups on APICD[0:1] and connect APICCLK to the clock generator. If the APIC is not used: The APICCLK can either be tied to GND or connected to the clock generator, but not left floating.
ICH RTC Oscillator Circuitry:	Refer to the circuit (resistor values and capacitor values, etc.) shown in the Design Guide.
GPI[8:13]	Ensure all wake events are routed through these inputs. These are the only GPIs that can be used as ACPI compliant wake events because they are the only GPI signals in the resume well that have associated status bits in the GPE1_STS register.
HL_COMP	There are 2 options for HL_COMP: **Option 1 —** RCOMP Method: Tie the COMP pin to a 40 Ω 1% or 2% (or 39 Ω 1%) pull-up resistor to 1.8V via a 10 mil wide, very short (~0.5 inch) trace (targeted for a nominal trace impedance of 40 Ω). **Option 2 —** ZCOMP Method: The COMP pin must be tied to a 10mil trace that is AT LEAST 18 inches long. This trace must be un-terminated and care should be taken when routing the signal to avoid crosstalk (1520 mil separation between this signal and any adjacent signals is recommended). This signal may not cross power plane splits.
5V_REF	Refer to the most recent version of the Design Guide for implementation of the voltage sequencing circuit.
SERIRQ	Need 8.2 kΩ (approximate) pull-up resistor to 3.3V.
SLP_S3#, SLP_S5#	No pull-ups required. These signals are always driven by the ICH.
CLK66	Needs 18 pF tuning capacitor as close as possible to ICH.

Checklist Line Items	Comments
PCI_GNT# signals	No external pull-ups are required on PCI_GNT# signals. However, if external pull-ups are implemented, they must be pulled up to 3.3V.
GPIO27/ALERTCLK GPIO28/ ALERTDATA	Add a 10 kΩ pull-up resistor to 3VSB (3 volt standby) on both of these signals.

Table 41. IDE Checklist

Checklist Line Items	Comments
CBLID#/PDIAG# (cable detect):	Refer to the latest design guide for the correct circuit. NOTE: All ATA66 drives will have the capability to detect cables.
PDD[15:0], PDIOW#, PDIOR#, PDREQ, PDDACK#, PIORDY, PDA[2:0], PDCS1#, PDCS3#, SDD[15:0], SDIOW#, SDIOR#, SDREQ, SDDACK#, SIORDY, SDA[2:0], SDCS1#, SDCS3#, IRQ14, IRQ15	No external series termination resistors required on those signals with integrated series resistors.
IDE Reset	This signal requires a 22 Ω–47 Ω series termination resistor and should be connected to buffered PCIRST#.
PDD[15:0], SDD[15:0]	PDD7 and SDD7 need a 10 kΩ (approximate) pull-down resistor to ground. Refer to ATA ATAPI-4 specification.
PIORDY, SDIORDY	Need 1 kΩ (approximate) pull-up resistor to 5V.
IRQ14, IRQ15	Need 8.2 kΩ to 10 kΩ pull-up resistor to 5V.
PDDREQ, SDDREQ	Need 5.6 kΩ (approximate) pull-down resistor to ground.
CSEL	Need 470 Ω (approximate) pull-down resistor to ground.
IDEACTP#, IDEACTS#	Can use a 10 kΩ (approximate) pull-up resistor to 5V for HD LED implementation.
IOCS16#	Leave as No Connect.

Table 42. USB / Keyboard / Mouse Checklist

Checklist Line Items	Comments
D-/D+ data lines	To provide nominal target trace impedance of 45 Ω, should be 9 mils wide based on the recommended stackup presented in Section 6.2.
D-/D+ data lines	Use 15 Ω series resistors.
VCC USB (Cable power)	Power off 5 volt standby, if wake on USB is to be implemented, If there is adequate standby power. It should be powered off of 5 volt core instead of 5 volt standby if adequate standby power is not available.
Voltage Drop Considerations	The resistive component of the fuses, ferrite beads and traces must be considered when choosing components and Power/GND trace width. This must be done such that the resistance between the Vcc5 power supply and the host USB Port is minimized. Minimizing this resistance will minimize voltage drop seen along that path during operating conditions.
Fuse	A minimum of 1A fuse should be used. A larger fuse may be necessary to minimize the voltage drop.
Voltage Droop Considerations	Sufficient bypass capacitance should be located near the host USB receptacles to minimize the voltage droop that occurs upon the hot attach of a new device. See the most recent version of the USB specification for more information.

Table 43. AC'97 Checklist

Checklist Line Items	Comments
AC_SDIN[1:0]	AC_SDIN[0] is recommended to be used for an onboard audio codec. Only one primary codec can be present on the link. A maximum of two active codecs are supported in an ICH platform. The SDATAIN[0:1] pins should not be left in a floating state if the pins are not connected and the AC-link is active, they should be pulled to ground through a weak (approximately 10 kΩ) pull-down resistor.
PRI_DN#	If the motherboard implements an active primary codec on the motherboard and provides an AMR connector, it must tie PRI_DN# to ground. The PRI_DN# pin is provided to indicate a primary codec is present on the motherboard. Therefore, the AMR module and/or codec must provide a means to prevent contention when this signal is asserted by the motherboard, without software intervention.
AC-link	Components such as FET switches, buffers, or logic gates, should not be implemented on the AC-link signals, except AC_RST#, without doing thorough simulation and analysis. Doing so will potentially interfere with timing margins and signal integrity A means of preventing contention on the AC-link must be provided for an onboard codec if the motherboard requires that an AMR module with a primary codec take precedence over an onboard primary codec.
AUDIO_MUTE#:	No connect on the motherboard.
AUDIO_PWRDN	Codecs on the AMR card should implement the EAPD powerdown pin, per the AC'97 2.1 specification, to control the amplifier.
MONO_PHONE	Connect to onboard audio codec if supported.

Checklist Line Items	Comments
MONO_OUT/ PC_BEEP	Connect to SPKR output from ICH or MONO_OUT from onboard codec.
PRIMARY_DN#	See discussion above.
+5VDUAL/+5VSB	If an adequate power supply is available, this pin should be connected to +5Vdual or +5Vsby. In the event that these planes cannot support the required power, it can be connected to VCC5 core on the motherboard. An AMR card using this standby/dual supply should not prevent basic operation if this pin is connected to core power.
S/P-DIF_IN	Connect to ground on the motherboard.
AC_SDIN[3:2]	No connect on the motherboard. The ICH supports a maximum of two codecs, which should be attached to SDIN[1:0].
AC97_MSTRCLK	Connect to ground on the motherboard.
PC_BEEP	Should be routed through the audio codec. Care should be taken to avoid the introduction of a pop when powering the mixer up or down.

Table 44. FWH Flash BIOS Checklist

Checklist Line Items	Comments
No floating inputs.	Unused FGPI pins need to be tied to a valid logic level.
INIT#	FWH Flash BIOS INIT# must be connected to processor INIT#.
RST#	FWH Flash BIOS RST# must be connected to PCIRST#.
ID[3:0]	For a system with only one FWH Flash BIOS device, tie ID[3:0] to ground.

Table 45. LPC Super I/O Checklist

Checklist Line Items	Comments
LPC_PME#	Do not connect LPC PME# to PCI PME#. If the design requires the Super I/O to support wake from any suspend state, connect Super I/O LPC_PME# to a resume well GPI on the ICH.
LPC_SMI#	This signal can be connected to any ICH GPI. The GPI_ROUTE register provides the ability to generate an SMI# from a GPI assertion.
LFRAME#	This signal is actively driven by ICH and does not require a pull-up resistor.
LAD[0:3]	No additional pull-up resistors required. These signals have integrated pull-ups in the ICH.
LDREQ[0]#	This signal is actively driven by the Super I/O and does not require a pull-up resistor.

Table 46. Clock Synthesizer Checklist

Checklist Items	Recommendations
REFCLK	• Connects to R-RefCLK, USB_CLK, SIO_CLK14, and ICHCLK14.
ICH_3V66/3V66_0, DOTCLK	• Passes through 33 Ω resistor. • When signal is input for ICH, it is pulled down through a 18 pF capacitor to GND.
DCLK/DCLK_WR	• Passes through 33 Ω resistor. • When signal is input for GMCH, it is pulled down through a 22 pF capacitor to GND.
CPUHCLK/CPU_0_1	• Passes through 33 Ω resistor. • When signal is input for 370PGA, decouple through a 18 pF capacitor to GND.
R_REFCLK	• REFCLK passed through 10 kΩ resistor. • When signal is input for 370PGA, pull-up through 1 kΩ resistor to VCC3.3 and pass through 10 kΩ resistor.
USB_CLK, ICH_CLK14	• REFCLK passed through 10 Ω resistor.
XTAL_IN, XTAL_OUT	• Passes through 14.318 MHz oscillator. • Pulled down through 18 pF capacitor to GND.
SEL1_PU	• Pulled up via MEMV3 circuitry through 8.2 kΩ resistor.
FREQSEL	• Connected to clock frequency selection circuitry through 10 kΩ resistor.
L_VCC2_5	• Connects to VDD2_5[0…1] through ferrite bead to VCC2.5.
GMCHHCLK/CPU_1, ITPCLK/CPU_2, PCI_0/PCLK_OICH, PCI_1/PCLK_1, PCI_2/PCLK_2, PCI_3/PCLK_3, PCI_4/PCLK_4, PCI_5/PCLK_5, PCI_6/PCLK_6, APICCLK_CPU/APIC_0, APICCLK)ICH/APIC_1, USBCLK/USB_0, GMCH_3V66/3V66_1, AGPCLK_CONN	• Passes through 33 Ω resistor.
MEMCLK0/DRAM_0, MEMCLK1/DRAM_1, MEMCLK2/DRAM_2, MEMCLK3/DRAM_3, MEMCLK4/DRAM_4, MEMCLK5/DRAM_5, MEMCLK6/DRAM_6, MEMCLK7/DRAM_7, SCLK	• Pass through 22 Ω resistor.

Table 47. Power Delivery Checklist

Checklist Items	Recommendations
All voltage regulator components meet maximum current requirements.	• Consider all loads on a regulator, including other regulators.
All regulator components meet thermal requirements.	• Ensure the voltage regulator components and dissipate the required amount of heat.
VCC1.8	• VCC1.8 power sources must supply 1.8 V and be between 1.71 V to 1.89 V.
If devices are powered directly from a dual rail (i.e., not behind a power regulator), then the RDSon of the FETs used to create the dual rail must be analyzed to ensure there is not too much voltage drop across the FET.	• “Dual” voltage rails may not be at the expected voltage.
Dropout voltage	• The minimum dropout for all voltage regulators must be considered. Take into account that the voltage on a dual rail may not be the expected voltage.
Voltage tolerance requirements are met.	• See the individual component specifications for each voltage tolerance.
Total power consumption in S3 must be less than the rated standby supply current.	• Adequate power must be supplied by power supply.

10 Third-Party Vendor Information

This design guide has been compiled to give an overview of important design considerations while providing sources for additional information. This chapter includes information regarding various third-party vendors who provide products to support the 810E chipset platform for use with the universal socket 370.

Note: The list of vendors can be used as a starting point for the designer. Intel does not endorse any one vendor, nor guarantee the availability or functionality of outside components. Contact the manufacturer for specific information regarding performance, availability, pricing and compatibility.

Table 48. Super I/O

Vendors	Contact	Phone
SMC	Dave Jenoff	(909) 244-4937
National	Robert Reneau	(408) 721-2981
ITE	Don Gardenhire	(512)388-7880
Winbond	James Chen	(02) 27190505 - Taipei office

Table 49. Clock Generation

Vendors	Contact	Phone
Cypress	John Wunner	206-821-9202 x325
ICS	Raju Shah	408-925-9493
IC Works	Jeff Keip	408-922-0202, x1185
IMI	Elie Ayache	408-263-6300, x235
PERICOM	Ken Buntaran	408-435-1000

Table 50. Memory Vendors

http://developer.intel.com/design/motherbd/se/se_mem.htm

Table 51. Voltage Regulator Vendors

Vendors	Contact	Phone
Linear Tech Corp.	Stuewart Washino	408-432-6326
Celestica	Dariusz Basarab	416-448-5841
Corsair Microsystems	John Beekley	888-222-4346
Delta Electronics	Colin Weng	886-2-6988, x233(Taiwan)
N. America: Delta Products Corp.	Maurice Lee	510-770-0660, x111

Table 52. Flat Panel

Vendors	Contact	Phone
Silicon Images Inc	John Nelson	408-873-3111

Table 53. AC'97

Vendors	Contact	Phone
Analog Devices	Dave Babicz	781-461-3237
AKM	George Hill	408-436-8580
Cirrus Logic (Crystal)	David Crowell	512-912-3587
Creative Technologies Ltd./ Ensoniq Corp.	Steve Erickson	408-428-6600 x6945
Diamond Multimedia Systems	Theresa Leonard	360-604-1478
ESS Technology	Bill Windsor	510-492-1708
Euphonics, Inc.	David Taylor	408-554-7201
IC Ensemble Inc.	Steve Allen	408-969-0888 x106
Motorola	Pat Casey	508-261-4649
PCTel, Inc.	Steve Manuel	410-965-2172
Conexant (formerly Rockwell)	Tom Eichenberg	949-221-4164
SigmaTel	Spence Jackson Arron Lyman	512-343-6636 512-343-6636 x11
Staccato Systems	Bob Starr	650-853-7035
Tritech Microelectronics, Inc.	Rod Maier	408-941-1360
Yamaha	Jose Villafuerte (US) Kazunari Fukaya (Japan)	408-467-2300 (0539) 62-6081

Table 54. TMDS Transmitters

Vendors	Component	Contact	Phone
Silicon Images	SII164	John Nelson	(408) 873- 3111
Texas Instrument	TFP420	Greg Davis (gdavis@ti.com)	(214) 480-3662
Chrontel	CH7301	Chi Tai Hong (cthong@chrontel.com)	(408) 544-2150

Table 55. TV Encoders

Vendors	Component	Contact	Phone
Chrontel	CH7007 / CH7008	Chi Tai Hong (cthong@chrontel.com)	(408)544-2150
Chrontel	CH7010 / CH7011	Chi Tai Hong (cthong@chrontel.com)	(408)544-2150
Conexant	CN870 / CN871	Eileen Carlson (eileen.carlson@conexant.com)	(858) 713-3203
Focus	FS450 / FS451	Bill Schillhammer (billhammer@focusinfo.com)	(978) 661-0146
Philips	SAA7102A	Marcus Rosin (marcus.rosin@philips.com)	None
Texas Instrument	TFP6022/ TFP6024	Greg Davis (gdavis@ti.com)	(214) 480-3662

Table 56. Combo TMDS Transmitters/TV Encoders

Vendors	Component	Contact	Phone
Chrontel	CH7009/ CH7010	Chi Tai Hong (cthong@chrontel.com)	(408) 544-2150
Texas Instrument	TFP6422/ TFP6424	Greg Davis (gdavis@ti.com)	(214) 480-3662

Table 57. LVDS Transmitter

Vendors	Component	Contact	Phone
National Semiconductor	387R	Jason Lu (Jason.Lu@nsc.com)	(408) 721-7540