Intel 430HX PCIset

82439HX (TXC)

Specification Update

Release Date: July 1996

Order Number 297652-001

The Intel 430HX PCIset may contain design defects or errors known as errata. Characterized errata that may cause the Intel 430HX PCIset's behavior to deviate from published specifications are documented in this specification.

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REVISION HISTORY

Date of Revision	Version	Description
July 1996	-001	Initial Release.

PREFACE

This document is an update to the specifications contained in the *Intel 430HX PCIset TXC Datasheet (Order Number 290551)*, and contains issues affecting all designs using the production revisions of the Intel 430HX PCIset (A-1 82439HX).

This document is intended for hardware system manufactures and software developers of applications, operating systems or tools. It contains Specification Changes, Errata, Specification Clarifications, and Documentation Changes.

Nomenclature

Specification Changes are modifications to the current published specifications. These modifications will be reflected in the future releases of the affected specification.

Errata are design defects or errors. Characterized errata may cause the Intel 430HX PCIset's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Clarifications describes a specification in greater detail or highlights complex design situations that may require implementation changes.

Documentation Changes include typos, errors, or omissions from the current published specification. The changes will be incorporated in the next revision of the documents.

S-Specs are temporary exceptions to the published standard specifications.

82439HX TXC Component Marking Information

Stepping	S-Spec	Top Marking	Notes
A-3	**S U115**	**82439HX S U115**	**Production**
A-2	**S U102**	**82439HX *S U102***	**Production**
A-1	**S U087**	**82439HX *S U087***	**Production**

Component Identification via Programming Interface

The 82439HX (TXC) stepping can be identified by the following register contents:

82439HX Stepping	Vendor ID[1]	Device ID[2]	Revision Number[3]
A-1	8086h	1250h	01h
A-2	8086h	1250h	02h
A-3	8086h	1250h	03h

(1) The Vendor ID corresponds to bits 15-0 of the Vendor ID Register located at offset 00-01h in the PCI configuration.

(2) The Device ID corresponds to bits 15-0 of th e Device ID Register located at offset 02-03h in the PCI configuration space.

(3) The Revision Number correspond to bits 7-0 of the Revision ID Register located at offset 08h in the PCI configuration space.

SUMMARY TABLE OF CHANGES

The following table indicates the Specification Changes, Errata, Specification Clarifications, or Documentation Changes which apply to all currently available steppings and planned steppings. Intel intends to account for the outstanding issues through documentation or specification changes as noted. This table uses the following notations:

CODES USED IN SUMMARY TABLE

X:	Specification Change or Clarification that applies to this stepping or to this product line.
Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix	There are no plans to fix this erratum.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.
Shaded:	This erratum is either new or modified from the previous version of this document.

82439HX TXC

NO.	A1	A2	A3	Plans	SPECIFICATION CHANGES
1	X	X	X	Doc	Error reporting on SERR#
2	X	X	X	Doc	DRAM timing with ECC enabled
3	X	X	X	Doc	PCI protocol violation with 32 clock retry and ECC
4	X	X	X	Doc	Missing snoop cycle with 32 clock retry and ECC
5	X	X	X	Doc	12x8 asymmetric DRAM not supported
6	X	X	X	Doc	DRAM cache refresh during PCI peer-to-peer traffic
7	X	X	X	Doc	512K cache with SCFMI bit set
8	X	X	X	Doc	Enabling delayed transactions

NO.	A1	A2	A3	Plans	ERRATA
1	X	Fixed	Fixed		ECC non-detection of single/double bit errors on partial memory writes
2	X	Fixed	Fixed		Spurious SERR# during PCI-to-PCI peer transfers in ECC/parity modes
3	X	X	Fixed		Snoop ahead during PCI read cycle (DP systems)

SPECIFICATION CHANGES

1. Error Reporting on SERR#

PROBLEM: SERR# generation (for uncorrectable ECC errors) using the ERRSTS register does not function as defined in the current specification. The original definition for this register states that an SERR# should be generated by first clearing the MEF bit in the ERRSTS register by writing a '1' to this bit. Once the MEF bit has been cleared, writing a '1' to the MEF bit again will cause an SERR# to be generated. This definition is incorrect. When the MEF bit has been set due to an uncorrectable ECC error, a write of any value (1 or 0) to the MEF bit will clear the bit. In addition, a write of any value (1 or 0) to the MEF bit will cause an SERR# to be generated.

IMPLICATION: When the BIOS writes to the ERRSTS register, SERR# may be generated even though no error has occurred. In addition, any write to the ERRSTS register will clear the MEF and SEF bits.

WORKAROUND: The workaround is to disable SERR# (by setting PCICMD[SERRE] = '0') before ANY write to the ERRSTS register except the ones which are done for the explicit purpose of generating a SERR#. In addition, before any write to the ERRSTS register, the MEF and SEF bits must be checked, since any write to this register will clear these bits. For example, when software is writing to the ERRSTS register for clearing SEF or MEF bits, SERR# should be disabled. In systems which use SMI# for reporting ECC errors, when SERR# is asserted due to an uncorrectable error, the SMI routine should do the following in sequence :

1. Read the ECC error flags (MEF, SEF) to determine that an uncorrectable error has occurred.
2. Disable SERR# by setting PCICMD[SERRE] = '0'.
3. Clear MEF bit by writing '1' to it.
4. Enable SERR# again.
5. Write '1' to MEF bit to create an NMI event.

STATUS: This specification change will be reflected in future revisions of the 82439HX documentation. The system BIOS should be changed as described above.

2. DRAM Timing with ECC Enabled

PROBLEM: Systems that support ECC must set the burst rate (for reads and writes) to x-3-3-3 (or x-4-4-4).

IMPLICATION: Currently, x-2-2-2 timings are only supported for systems designed for up to 4 DRAM SIMMs and which do not use external MA buffers. In addition, 60ns EDO DRAMs are required to meet the x-2-2-2 timings. Any systems meeting the above requirements and which support ECC must use x-3-3-3 burst timings, instead of x-2-2-2. All other systems will already have x-3-3-3 (or x-4-4-4), and hence there is no system impact.

WORKAROUND: When ECC is enabled, the read and write burst timings in the DRAMT register must be programmed to x-3-3-3 (or x-4-4-4).

STATUS: This specification change will be reflected in future revisions of the 82439HX documentation. When ECC is enabled, the DRAM read timings should be programmed as defined above.

3. PCI Protocol Violation with 32 Clock Retry and ECC

PROBLEM: The following scenario may result in a PCI protocol violation by the TXC:

1) A PCI master initiates a write to DRAM.

2) The DRAM buffers are full and draining very slowly, resulting in a 32 clock retry to the PCI master.

3) The DRAM buffer becomes available during the same clock that the retry is generated on the PCI bus.

The TXC will assert STOP# (to retry the cycle after 30 clocks) and then on the next clock deassert STOP# and assert TRDY#. This is a violation of PCI protocol. This scenario only occurs when ECC is enabled, because read-modify-write cycles required for ECC partial writes cause the slow buffer drain.

IMPLICATION: The above scenario will cause a PCI protocol violation to occur. As a result, the 32 clock retry feature is no longer supported when ECC is enabled.

WORKAROUND: For ECC systems, the 32 clock retry feature should be disabled. The feature can be disabled by setting bit 2 at Register Offset 4FH to 1.

STATUS: This specification change will be reflected in future revisions of the 82439HX documentation.

4. Missing Snoop Cycle with 32 Clock Retry and ECC

PROBLEM: The following scenario may result in a missed snoop cycle by the TXC:

1) A PCI master initiates a write to DRAM.

2) The DRAM buffers are full and draining very slowly, resulting in a 32 clock retry to the PCI master.

3) The DRAM buffer becomes available during the same clock that the 32 clock retry counter expires.

The TXC will not generate a snoop cycle for the corresponding PCI write cycle. This scenario only occurs when ECC is enabled, because read-modify-write cycles required for ECC partial writes cause the slow buffer drain.

IMPLICATION: The above scenario will result in a snoop cycle being missed, which may cause data corruption. As a result, the 32 clock retry feature is no longer supported when ECC is enabled.

WORKAROUND: For ECC systems, the 32 clock retry feature should be disabled. The feature can be disabled by setting bit 2 at Register Offset 4FH to 1.

STATUS: This specification change will be reflected in future revisions of the 82439HX documentation.

5. 12x8 Asymmetric DRAM Not Supported

PROBLEM: Due to lack of availability, 12x8 asymmetric DRAMs were not tested with the 82439HX. As a result, this type of DRAM is no longer supported.

IMPLICATION: 12x8 Asymmetric DRAMs are not supported on an Intel 430HX PCIset platform.

WORKAROUND: Do not use 12x8 asymmetric DRAM.

STATUS: This specification change will be reflected in future revisions of the 82439HX documentation.

6. DRAM Cache Refresh During PCI Peer to Peer Traffic

PROBLEM: If a PCI peer to peer cycle occurs at the same time as a CPU to DRAM cycle, and then a DRAM cache refresh request occurs, the system will lock up.

IMPLICATION: For systems using a DRAM cache, the above scenario will cause a system lock-up.

WORKAROUND: For single processor systems using a DRAM cache, register 51, bit 5 in the 82439HX should be set to a one. For dual processor systems using a DRAM cache and using the cC0 (or later) stepping of the Pentium(TM) Processor, register 51, bit 5 in the 82439HX should also be set to a one. For dual processor systems using earlier steppings of the Pentium Processor, the DRAM cache is not supported.

STATUS: This specification change will be reflected in future revisions of the 82439HX documentation.

7. 512K Cache with SCFMI Bit Set

PROBLEM: When the SCFMI (Secondary Cache Force Miss and Invalidate) bit is set and the L2 cache size is 512k, the TXC does not execute a writeback for all modified lines.

IMPLICATION: Incorrect data will be stored in memory, since the writeback for a modified line did not occur.

WORKAROUND: When attempting to flush the L2 cache, the BIOS should read twice the size of the L2 cache just before setting the SCFMI bit. If the cache size is 512K, then the BIOS should read two non-overlapping, cacheable 512K regions from DRAM. This forces any modified lines to be written back to the memory. Please refer to the Intel 430HX PCIset BIOS Specification for more details.

STATUS: This specification change will be reflected in future revisions of the Intel 430HX PCIset documentation.

8. Enabling Delayed Transactions

PROBLEM: Due to previous errata on the A-1 PIIX3 and A-1/A-2 TXC, the delayed transaction feature in the PIIX3 was disabled. Systems using the A-3 TXC and B-0 PIIX3 should enable delayed transactions.

IMPLICATION: None.

WORKAROUND: For the A-3 TXC and B-0 PIIX3 combination, Delayed Transactions (PIIX3 Function 0, 82h[0]), North Bridge Retry Enable (PIIX3 Function 0, 6Ah[7]), and TXC 4Fh[7] bits should all be set to '1'. When enabling, the PIIX3 bits should be set first and then the TXC 4Fh[7]. When disabling, the reverse order should be followed.

STATUS: This specification change will be reflected in future revisions of the Intel 430HX PCIset documentation.

ERRATA

1. ECC Non-Detection of Single/Double Bit Errors on Partial Memory Writes

PROBLEM: When the 82439HX performs a partial write to main memory (data less than a Qword) in ECC mode, the following happens:

1. A read-merge-write cycle must occur so that the proper checkbits can be regenerated across the entire 64 bits to be written into DRAM.
2. With ECC enabled, if either a single bit or double bit error was present in the Qword being read from DRAM, then the error should be flagged (via SEF or MEF) and then reported via SERR#. The 82439HX A0 and A1 steppings do not provide this signaling.

IMPLICATION: The above scenario does not flag errors (information that could prove useful to isolate a problematic SIMM or DIMM).

WORKAROUND: The 82439HX A-1 step provides single bit error correction. For ECC systems that require single bit error correction, the 82439HX can provide this level of reliability. For systems which require multiple bit ECC (servers for example), it is recommended that the customer use a stepped version of the 82439HX.

STATUS: This will be fixed on the A-2 stepping of the 82439HX.

2. Spurious SERR# During PCI to PCI Peer Transfers in ECC/Parity Modes

PROBLEM: An unexpected or spurious SERR# may occur during a PCI peer to peer memory read transaction. The 82439HX may signal an SERR# for a non-DRAM access. The scenario only occurs if a PCI master is performing a memory read from a PCI slave (peer to peer transaction). This PCI memory access must be located above the top of memory, but below the 512M boundary.

IMPLICATION: The above scenario could generate a false system NMI.

WORKAROUND : There are two possible workarounds:

1. Have BIOS relocate all PCI devices (PCI memory slaves) which receive peer initiated accesses above 512M.
2. In a system using 2-6 RAS lines, BIOS will qualify the SERR# with DRB7. If no DRAM is populated in bank 7, then the SERR# would not be valid, and could be ignored. This workaround is valid for only ECC mode.

STATUS: This will be fixed on the A-2 stepping of the 82439HX.

3. Snoop Ahead During PCI Read Cycle (Dual Processor Systems)

PROBLEM: During testing in a DP server environment a specific scenario was discovered that may cause incorrect data to be forwarded to a PCI master during a read cycle. The scenario is as follows:

a) The write buffers fill up due to continual CPU to DRAM writes.

b) A PCI master (other than the PIIX3) issues a write to DRAM and the subsequent snoop cycle is clean.

c) Another PCI master (other than the PIIX3) initiates a burst read to DRAM.

d) The snoop for the burst read finishes on the same clock edge that the previous write data is forwarded to the merging buffer.

e) The subsequent snoop ahead hits a modified line.

f) The writeback for the modified line is merged to the wrong location.

This issue was found in a DP server environment. Although no UP system failures or effects have been found after extensive testing, the workaround given below is recommended for all new UP and DP systems.

IMPLICATION: The above scenario will cause incorrect data to be forwarded to the PCI master that issued the burst read cycle.

WORKAROUND: The snoop ahead feature in the TXC should be disabled by setting Register 50, bit 1 to a one. In addition, Register 4F, bit 6 in the TXC should be set to one. The delayed transaction feature in the PIIX3 must also be disabled by setting Register 82, bit 0 to zero.

STATUS: This will be fixed on the A-3 stepping of the 82439HX.

SPECIFICATION CLARIFICATIONS

There are no Specification Clarifications to include in this revision.

DOCUMENTATION CHANGES

There are no Documentation Changes to include in this revision.