Intel® 82801DB I/O Controller Hub 4 (ICH4) / Intel® 82801DBL I/O Controller Hub 4-L (ICH4-L)

Specification Update

February 2006

Notice: The Intel® 82801DB ICH4 / Intel® 82801DBL ICH4-L products may contain design defects or errors known as errata which may cause the products to deviate from published specifications. Current characterized errata are documented in this specification update.

Document Number: 290745-025

The Intel® 82801DB I/O Controller Hub 4 (ICH4) and Intel® 82801DBL I/O Controller Hub 4-L (ICH4-L) products may contain design defects or errors known as errata which may cause the products to deviate from published specifications. Current characterized errata are available on request.
Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Contents

Revision History

Version	Description	Date
-001	Initial Release.	May 2002
-002	Added: ICH4 B0 Engineering Sample mark. **Specification Clarifications:** 12-Clock Retry Enable, USB Legacy Keyboard Mouse Control, RTC Voltage, Voh8 Characteristics, Power Sequencing **Documentation Changes:** GPIO Table, TCO Timer. Modified: Documentation Changes: PCI Device Rev ID.	July 2002
-003	Modified: Errata: AC'97 Underrun FIFO Error Bit Not Set, AC'97 Overrun FIFO Error Bit Not Set. Added: ICH4 B0 Production Mark Errata: RTC I/O Read, Excessive VccSus3_3 Current on G3 to S5 Transition, AC'97 FIFO Error Bit Software Overrun. Specification Clarifications: LPC LPCPD# Protocol Clarification, CPU Dead Alert Clarification. Documentation Changes: USB PORTSC Correction, GPIO[2]].	August 2002
-004	Added: Specification Clarifications: MTT Requirement Documentation Changes: Frequency Strap Correction	September 2002
-005	Added: **Specification Clarifications:** Native Mode IDE/ ACPI S3 Resume Hang Avoidance, THRMTRIP# **Documentation Changes:** Prefetch Flush Enable	October 2002
-006	Added: **Specification Change:** Power Sequencing **Specification Clarification:** Primary & Secondary IDE Status Register **Documentation Changes:** TCO_STS Bit Correction, Power Sequencing, IDE Section Corrections, IDE Interrupt Status Bit	November 2002
-007	Modified: Erratum: Excessive VccSus3_3 Current On G3 to S5 Transition Erratum Added: Specification Change: Delayed Transaction Discard Timer Specification Clarification: PCI Master Requirement Documentation Change: Section 9.7.5 Correction	March 2003
-008	Modified: Erratum: LPC Reset Timing Specification Clarification: CPU Dead Alert Clarification	May 2003

Version	Description	Date
-009	Added: Errata: PCI Non-linear Addressing Erratum Specification Clarifications: SMBus Byte Done Status Clarification, CTS Bit Clarification Documentation Changes: USB Overcurrent Correction, Figure 2-22 (RTC Circuit) Correction	June 2003
-010	Added: Documentation Changes: PME Wake Doc Change	July 2003
-011	Added: Erratum: MW DMA Mode-1 Tdh Erratum Documentation Changes: APM I/O Decode Correction, Memory Map Table Change	August 12003
-012	Added: Specification Clarifications: PERR# Implementation Documentation Changes: SMBus Host_Busy Correction	September 2003
-013	Added: Errata: LPC Starvation Erratum	January 2004
-014	Added: ICH4L Support Specification Change	March 2004
-015	Added: Erratum: USB Buffer Overrun Erratum Specification Clarifications: Port 63/65/67 and GPI ACPI Clarifications	May 2004
-016	Added: Specification Clarifications: USB CONFIGFLAG Clarification	June 2004
-017	Added: Specification Clarifications: CTS Clarification	August 2004
-018	Added: Erratum: USB2 Incorrect Periodic Frame List Pointer Fetch	September 2004
-019	Added: Documentation Change: GEN2_DEC Correction	November 2004
-020	Added: New Pb-Free Marks Specification Clarifications: GPIO Note Change	January 2005
-021	Added: Specification Clarifications: GPI_ROUT Clarification	February 2005
-022	Added: Errata: Full-speed USB ISOC End of Packet Specification Clarifications: LPC Cycle Clarification	March 2005
-023	Added: Documentation Change: 20-THRMTRIP# Timing Correction.	October 2005
-024	Added: Documentation Change: 21-USB Port Number Documentation Corrections.	November 2005
-025	Added: Document Change: 22-GPIO[13:11] & GPIO[8:0] Documentation Clarification	February 2006

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Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Note: All references to ICH4 refer to both ICH4 and ICH4-L, unless specified otherwise.

Affected Documents/Related Documents

Title	Document Number
Intel® 82801DB I/O Controller Hub 4 (ICH4) Datasheet	290744

Nomenclature

Errata are design defects or errors. Errata may cause the ICH4's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present in all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

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Summary Tables of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications, or Documentation Changes that apply to the Intel® 82801DB I/O Controller Hub 4 (ICH4) and Intel® 82801DBL I/O Controller Hub 4-L (ICH4-L). Intel intends to fix some of the errata in a future stepping of the component(s), and to account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X: Specification Change, Erratum, Specification Clarification or Documentation Change that applies to a stepping or to this product line.

(No mark) or
(Blank Box): This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Status

Doc: Document change or update that will be implemented.

PlanFix: This erratum is intended to be fixed in a future stepping of the product.

Fixed: This erratum has been previously fixed.

No Fix: There are no plans to fix this erratum.

Bar: This item is either new or modified from the previous version of the document.

Errata (Sheet 1 of 2)

Erratum Number	Steppings		Status	ERRATA
	A1	B0		
1	X	X	No Fix	SMBus Arbitration Erratum
2	X	X	No Fix	Intel® ICH4 LPC Reset Timing
3	X	X	No Fix	Intel® ICH4 Master Abort Mode
4	X	X	No Fix	SE0 during Resume Causes Disconnect
5	X	X	Fixed	AC ‘97 Underrun FIFO Error Bit Not Set
6	X	X	Fixed	AC ‘97 Overrun FIFO Error Bit Not Set
7	X		Fixed	RTC I/O Read
8	X	X	PlanFix	Excessive VccSus3_3 Current On G3 to S5 Transition

Errata (Sheet 2 of 2)

Erratum Number	Steppings		Status	ERRATA
	A1	B0		
9		X	No Fix	AC'97 FIFO Error Bit Software Overrun
10	X	X	No Fix	PCI Non-linear Addressing Erratum
11	X	X	No Fix	MW DMA Mode-1 Tdh Erratum
12	X	X	No Fix	LPC Starvation Erratum
13	X	X	No Fix	USB Buffer Overrun Erratum
14	X	X	No Fix	USB2 Incorrect Periodic Frame List Pointer Fetch
15	X	X	No Fix	Full-speed USB ISOC End of Packet

Specification Changes

Number	Status	SPECIFICATION CHANGES
1	Doc	Power Sequencing
2	Doc	Delayed Transaction Discard Timer
3	Doc	Intel® ICH4-L Support

Specification Clarifications (Sheet 1 of 2)

Number	SPECIFICATION CLARIFICATIONS
1	12-Clock Retry Enable
2	USB Legacy Keyboard Mouse Control
3	RTC Voltage
4	Voh8 Characteristics
5	Power Sequencing
6	LPC LPCPD# Protocol Clarification
7	CPU Dead Alert Clarification
8	MTT Requirement
9	Native Mode IDE/ACPI S3 Resume Hang Avoidance
10	THRMTRIP#
11	Primary & Secondary IDE Status Register
12	PCI Master Requirement
13	SMBus Byte Done Status Clarification
14	CTS Bit Clarification
15	PERR# Implementation
16	Port 63/65/67 Clarification
17	GPI ACPI Clarification
18	USB CONFIGFLAG Clarification
19	CTS Clarification

Specification Clarifications (Sheet 2 of 2)

Number	SPECIFICATION CLARIFICATIONS
20	GPIO Note Change
21	GPI_ROUT Clarification
22	LPC Cycle Clarification

Documentation Changes

Number	DOCUMENTATION CHANGES
1	PCI Device Rev ID
2	GPIO Table
3	TCO Timer
4	USB PORTSC Correction
5	GPIO[22]
6	Frequency Strap Correction
7	Prefetch Flush Enable
8	TCO_STS Bit Correction
9	Power Sequencing
10	IDE Section Corrections
11	IDE Interrupt Status Bit
12	Section 9.7.5 Correction
13	USB Overcurrent Correction
14	Figure 2-22 (RTC Circuit) Correction
15	PME Wake Doc Change
16	APM I/O Decode Correction
17	Memory Map Table Change
18	SMBus Host_Busy Correction
19	GEN2_DEC Correction
20	THRMTRIP# Timing Correction
21	USB Port Number Documentation Corrections.
22	GPIO[13:11] & GPIO[8:0] Documentation Clarification

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Identification Information

Markings

Stepping	S-Spec	Top Marking	Notes
A1	QC97	82801DB	Engineering Sample
A1	SL66K	82801DB	Production
B0	QD45	82801DB	Engineering Sample
B0	SL6DM	82801DB	Production
B0	QF29	82801DBL	Engineering Sample
B0	SI7CN	82801DBL	Production
B0	SL8DE	82801DB	Production Pb-Free
B0	QI89	82801DB	Engineering Sample Pb-Free

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Errata

1. SMBus Arbitration Erratum

Problem: ICH4 will not detect a bus collision when attempting to STOP at the end of a SMBus transaction as a master. If there is another external Bus Master attempting to access the bus at the same time and wins the arbitration during STOP bit, ICH4 does not set the Bus Error bit.

Implication: A master attempting a transfer that had actually "lost" may think that its transaction was completed when it was not completed.

Workaround: None.

Status: There are no plans to fix this erratum. For the steppings affected, see the *Summary Tables of Changes*.

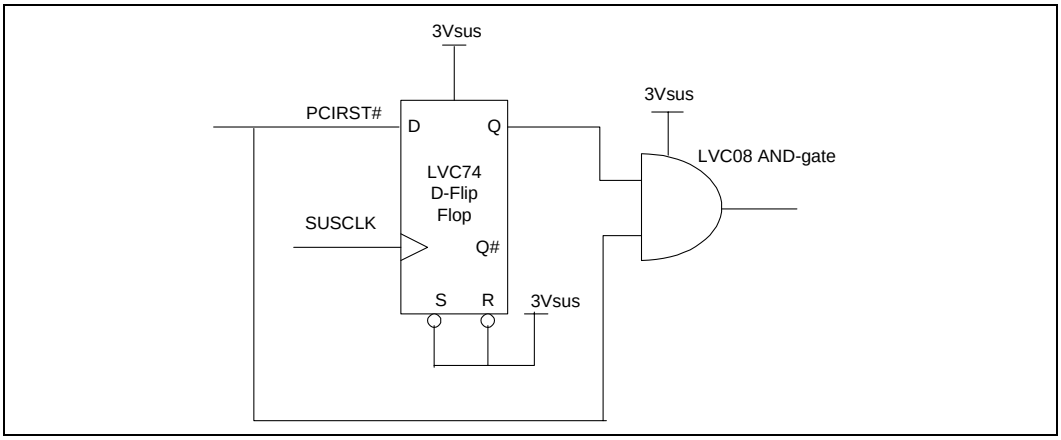
2. Intel® ICH4 LPC Reset Timing

Problem: The ICH4 specified 1–3 RTC timing of SUS_STAT# inactive to PCIRST# inactive violates the LPC Specification (Rev 1.0) of "at least 60 µs." LPC Specification Rev 1.1 is not violated by this erratum.

Implication: Some LPC devices may not properly reset resulting in failure of the system to boot or resume from a sleep state.

Workaround: Use any one of these three workarounds:

1. Delay PCIRST# by 1 SUSCLK using a D-flop and an AND gate to the LPC devices.



2. Do a CF9 hard reset within the first 100 ms of POST.
3. Do not connect the SUS_STAT# to the SIO PD input; instead, implement an external pull-up resistor on the PD input of the SIO.

Status: There are no plans to fix this erratum. For the steppings affected, see the *Summary Tables of Changes*.

3. Intel® ICH4 Master Abort Mode

Problem: ICH4 Master Abort Mode (BRIDGE_CNT – Bridge Control Register, D30:F0, offset 3E–3Fh, bit 5) is a new function. It was implemented incorrectly. A missing qualification can cause a Target Abort signal to a PCI agent that was uninvolved in the transfer.

Implication: ICH4 could Target Abort the wrong bus master.

Workaround: De-feature Master Abort Mode. Power on default is Master Abort Mode bit is disabled. BIOS needs to make sure this bit is not enabled.

Status: There are no plans to fix this erratum. For the steppings affected, see the *Summary Tables of Changes.*

4. SE0 during Resume Causes Disconnect

Problem: A transient SE0 during an upstream resume signal from the USB peripheral to the ICH4 while the system is in S3/S4 sleep states will cause the ICH4 to register a disconnect. This violates the USB Specification, Revision 1.1.

Implication: The implication is Operating System dependent. It can range from additional latency on a resume before the USB device is functional (after a resume), to the USB device no longer works after a resume - in which case a system reboot must be done to obtain USB device functionality. In all cases the rest of the system does resume.

Workaround: None

Status: There are no plans to fix this erratum. For the steppings affected, see the *Summary Tables of Changes.*

5. AC ’97 Underrun FIFO Error Bit Not Set

Problem: The ICH4 may not set the FIFO Error Bit in the Output Status Register after an underrun error occurs on a highly stressed system in the vicinity of the end of an AC ’97 output stream. The bit affected depends on what stream causes the error:
PCM Out - POSR (D31:F5: I/O Offset NABMBAR + 16h: Bit 4)
S/PDIF Out - SPSR (D31:F5: I/O Offset MBBAR + 66h: Bit 4)
Modem Out - MOSR (D31:F6: I/O Offset MBAR + 16h: Bit 4)

Implication: Driver vendors typically do not use this status bit in their production drivers.

Workaround: None

Status: This erratum has been previously fixed. For the steppings affected, see the *Summary Tables of Changes.*

6. AC '97 Overrun FIFO Error Bit Not Set

Problem: The ICH4 may not set the FIFO Error Bit in the Input Status Register after an overrun error occurs on a highly stressed system in the vicinity of the end of an AC' 97 input stream. The bit affected depends on what stream causes the error:
PCM In - PISR (D31:F5: I/O Offset NABMBAR + 06h: Bit 4)
PCM 2 In - PI2SR (D31:F5: I/O Offset MBBAR + 56h: Bit 4)
Microphone In - MCSR (D31:F5: I/O Offset NABMBAR + 26h: Bit 4)
Microphone 2 In - MC2SR (D31:F5: I/O Offset MBBAR + 46h: Bit 4)
Modem In - MISR (D31:F6: I/O Offset MBAR + 06h: Bit 4)

Implication: Driver vendors typically do not use this status bit in their production drivers.

Workaround: None

Status: This erratum has been previously fixed. For the steppings affected, see the *Summary Tables of Changes.*

7. RTC I/O Read

Problem: Under certain conditions, a CPU generated I/O read to RTC registers 0-9 may return an incorrect value. The issue occurs on read paths and the RTC registers are not impacted. This issue has only been found using a synthetic test environment and has not been reported using commercially available software.

Implication: An operating system which synchronizes the time/date value with RTC registers may get incorrect value.

Workaround: A BIOS workaround is available. See ICH4 BIOS Specification and updates for implementation details.

Status: This erratum has been previously fixed. For the steppings affected, see the *Summary Tables of Changes*

8. Excessive VccSus3_3 Current on G3 to S5 Transition

Problem: Some ICH4 devices may have excessive current on the VccSus3_3 supply only when the system transitions from G3 to S5 state (from no AC power to AC plugged in - but system off). This current may be as high as approximately 185 mA.

Implication: Leakage through USB ports may cause some USB peripherals to temporarily become non-functional on the first boot after AC power is applied.

Workaround: Choice depends on motherboard design and USB peripheral power source.

Systems containing motherboards with its USB bus powered by 5V core

- For bus powered USB peripherals (choose any one of the three or any combination)

1) Early in BIOS POST, if GEN_PMCON_3:[PWR_FLR]=1 (indicates AC power was lost and restored) then perform a hard reset (I/O write of 0Eh to CF9 Reset Register). Adds approximately 4 seconds to cold boot time.

2) Disconnect and reattach USB peripherals while the system is on after AC power is restored.

3) Restart the system by shutting it down, then turning it back on - keeping AC power applied.

-For self powered USB peripherals: Disconnect the USB peripheral, remove its power, restore its power and finally reconnect the USB peripheral all while the system is on after AC power is applied.

Systems containing motherboards with its USB bus powered by 5V_Auxiliary

-For bus powered USB peripherals: Disconnect and reattach the USB peripheral while the system is on after AC power has been restored.

- For self powered USB peripherals: Disconnect the USB peripheral, remove its power, restore its power and finally reconnect the USB peripheral all while the system is on after AC power is applied.

Status: Planned Fix. For the steppings affected, see the *Summary Tables of Changes.*

9. AC '97 FIFO Error Bit Software Overrun

Problem: The ICH4 may set the FIFOE Bit in the Input Status Register after a software overrun error occurs on a highly stressed system. The ICH4 should only set the FIFOE bit on a hardware overrun.

Bit affected depends on which stream is currently running:

PCM IN - PISR (D31:F5: I/O Offset NABMBAR+06h:bit-4)

Mic IN - MCSR (D31:F5: I/O Offset NABMBAR+26h:bit-4)

Mic 2 IN - MC2SR (D31:F5: I/O Offset MBBAR+46h:bit-4)

PCM 2 IN - PI2SR (D31:F5: I/O Offset MBBAR+56h:bit-4)

Modem IN - MISR (D31:F6: I/O Offset MBAR+06h:bit-4)

Implication: No data was lost because the software did not expect an additional sample. Driver vendors typically do not use this status bit in their production drivers.

Workaround: None.

Status: There are no plans to fix this erratum. For the steppings affected, see the *Summary Tables of Changes.*

10. PCI Non-linear Addressing Erratum

Problem: If PCI Memory Read Multiple or Memory Read Line transaction falls at the last DW of a 32 byte cache line boundary and non-linear addressing (cache-line wrap mode) is used the ICH4 will pre-fetch data past the cache line boundary. All subsequent PCI bus master reads will get incorrect data. Subsequent CPU cycles to PCI/LPC will get blocked behind the surplus data resulting in a system hang.

Implication: None known.

- System hang only seen in synthetic test environment.

- No known commercial PCI devices support cache-line wrap mode using Memory Read Multiple or Memory Read Line.

Workaround: None.

Status: No Fix. For the steppings affected, see the *Summary Tables of Changes.*

11. MW DMA Mode-1 Tdh Erratum

Problem: Data hold time of MW DMA Mode-1 writes may not meet ATA Specification.

Implication: None known.

Workaround: Program the controller to PIO Mode-4 instead.

Status: No Fix. For the steppings affected, see the *Summary Tables of Changes.*

12. LPC Starvation Erratum

Problem: Latency issues on LPC may occur if a PCI bus master is performing large upstream bursts to memory and no other PCI devices are requesting the bus. If an LPC cycle occurs during an upstream PCI burst, the completion of the LPC cycle may get delayed until the PCI device completes its transaction and de-asserts its REQ#.

Implication: Under certain operating conditions, latency on the LPC bus may cause delays in accessing data from an LPC based device.

Workaround: None.

Status: No Fix. For the steppings affected, see the *Summary Tables of Changes.*

13. USB Buffer Overrun Erratum

Problem: If a USB full-speed isochronous or asynchronous inbound transaction is on the verge of an overrun event (requires 20 µs of system latency) and the USB FIFO begins to empty during a 30 ns window immediately prior to the overrun event actually occurring, extra data can be sent to memory. This erratum has only been reproduced with synthetic test environments and not with real world applications.

Implication: Extra data may be sent to memory and/or data could be erroneously written beyond the boundary of the USB buffer allocation. This may result in unpredictable system behavior. There is no known exposure with real world applications.

Workaround: None.

Status: No Fix. For the steppings affected, see the *Summary Tables of Changes*

14. USB2 Incorrect Periodic Frame List Pointer Fetch

Problem: The USB2 controller may fetch an incorrect periodic frame list pointer when the periodic activity is heavily scheduled and there are large latencies on descriptor requests to memory when running HS isochronous or interrupt traffic.

Note: This has only been reproduced in synthetic test environments.

Implication: There may be intermittent audio pops or lost video frames on USB2 HS devices when the system is heavily loaded in synthetic test environments.

Workaround: None.

Status: No Fix. For the steppings affected, see the *Summary Tables of Changes.*

15. Full-speed USB ISOC End of Packet

Problem: If a Full-speed USB ISOC OUT transaction occurs very late in the USB frame such that the payload cannot be contained in that frame, then a bit-stuff error is created as defined in the USB 2.0 specification and flagged to both host software and the device. When this occurs, and a specific data pattern is present, then the End of Packet (EOP) will not be sent. In this event, devices attached to that UHCI controller may not detect the subsequent Start of Frame (SOF) due to lack of EOP.

Implication: None, the resulting bit-stuff error and device not detecting SOF are recoverable events by USB 2.0 system design.

Workaround: None.

Status: No Fix.

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Specification Changes

1. Power Sequencing

Table 17-19 (Power Sequencing and Reset Signal Timings), t170 is being changed from 5 ms to 18 ms (minimum).

2. Delayed Transaction Discard Timer

Section 8.1.27 describes the ICH4 Configuration Register. Bit-2 is now defined as indicated.

2	**Delayed Transaction Discard Timer** — R/W. When set to 1 this bit shortens all delayed transaction discard timers from 32 µs to 4 µs. Note: Setting this bit may improve system performance issues with certain non-optimally behaved PCI devices but may violate the PCI-to-PCI Bridge Architecture Specification Rev 1.1 (section 5.3.2).

3. Intel® ICH4-L Support

The ICH4-L device is a functional subset of the ICH4. USB2 functionality is disabled on the ICH4-L and the USB2 related registers in ICH4 PCI Configuration Space are not available in the ICH4-L.

The ICH4-L's PCI Device ID's and Rev ID's are listed below:

Table 1. PCI Device Revision ID Table

Device Function	Description	Intel® ICH4-L Dev ID	B0 Rev ID
D30, F0	P2P Bridge	2448h	82h
D31, F0	P2L Bridge	24C0h	02h
D31, F1	IDE	24C1h	02h
D31, F3	SMBus	24C3h	02h
D31, F5	AC '97 Audio	24C5h	02h
D31, F6	AC '97 Modem	24C6h	02h
D8, F0	LAN	103Ah	82h
D29, F0	USB UHCI #1	24C2h	02h
D29, F1	USB UHCI #2	24C4h	02h
D29, F2	USB UHCI #3	24C7h	02h

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Specification Clarifications

1. 12-Clock Retry Enable

- In Section 8.1.27 replace the description for Bit[1] with the following. There is no relationship between this bit and PCI locked cycles:

1	**12-Clock Retry Enable** — R/W. System BIOS must set this bit for PCI compliance. 0 = If this bit is not set, the ICH4 will insert as many wait states as needed to complete the PCI to memory cycle. 1 = The ICH4 will retry a PCI to memory cycle (reads or writes) if the ICH4 is not able to complete the transfer in 12 PCI clocks.

2. USB Legacy Keyboard Mouse Control

- In Section 11.1.16 (USB_LEGKEY) add the following note to bits [15, 11:8, 6]:

Note: This bit reports same value in all USB UHCI controllers.

- In Section 11.1.16 (USB_LEGKEY) add the following note to bits [7, 5, 3:0]:

Note: Setting this bit in any controller enables the function.

3. RTC Voltage

- In Table 17-6 (Other DC Characteristics) replace VccRTC with the following:

VccRTC	Powered by Coin Cell Battery	2.0	3.3	V	
	Powered by Power Supply	2.0	3.6	V	

4. V_{OH8} Characteristics

- In Table 17-5 (DC Output Characteristics) remove the 12 mA spec from the HI 1.5 mode rows of V_{OH8} as shown below. This spec no longer applies.

V_{OH8}	Output High Voltage	0.9(VccHI)		V	–1 mA	HI 1.0 Mode
		VSWING–50 mV	VSWING+50 mV	V		HI 1.5 Mode Terminator High Voltage Note 2
		VSWING–50 mV	VSWING+50 mV	V		HI 1.5 Mode Output High Voltage Note 3

- Below Table 17-5 (DC Output Characteristics) replace note 2 with the following:

  The condition for the Terminator High Voltage is ZPU = ZTARG(VccHI/VSWING – 1).

5. Power Sequencing

- In Table 17-19 (Power Sequencing and Reset Signal Timings) replace t173 with the following:

t173	VccSus supplies active to LAN_RST# high, RSMRST# high	10	—	ms		17-18 17-20

- In Table 17-19 (Power Sequencing and Reset Signal Timings) replace t176 with the following:

t176	Vcc3_3, Vcc1_5, VccHI supplies active to PWROK, VRMPWRGD active	10	—	ms		17-18 17-20

- In Table 17-20 (Power Management Timings) replace t184 with the following:

t184	V_CPU_IO active to STPCLK# and CPUSLP# inactive, and processor Frequency Strap signals high		50	ns		17-20

6. LPC LPCPD# Protocol Clarification

The LPC specification defines the LPCPD# protocol where there is at least 30 uS from LPCPD# assertion to LRST# assertion. This specification explicitly states that this protocol only applies to entry/exit of low power states (which does not include asynchronous reset events). The ICH4 will assert both SUS_STAT# (connects to LPCPD#) and PCIRST# (connects to LRST#) at the same time when the core logic is reset (via CF9, PWROK, SYS_RESET#, etc.). This is not inconsistent with the LPC LPCPD protocol.

7. CPU Dead Alert Clarification

Section 5.13.2 describes the “Processor Missing Event Status” and how an Alert Message can be sent via LAN. This feature is meant to function when a processor is installed in the socket (but is non-functional) and was not intended to alert when the processor was not installed. When the processor is not installed, VRMPWRGD is programmed not to assert which prevents TCO Timer operation. It is this timer that is used to set the SECOND_TO_STS bit in TCO2_STS (TCOBase+06h), used for the alert.

To enable this messaging without a processor installed in the socket, external logic, monitoring processor socket signal SKTOCC#, should drive VID:[4] low which will enable the VRM to drive its CPUPWRGD signal, which in turn will allow the CPU Dead Alert to function under this empty socket condition. This technique only applies to configurations in which processor “socket sense” is used.

8. MTT Requirement

Section 8.1.28, *MTT - Multi-Transaction Timer Register*, of D30:F0, must be set to greater than 16 clocks.

9. Native Mode IDE / ACPI S3 Resume Hang Avoidance

System BIOS must clear the Interrupt bit (bit-2) in Bus Master Status Register for BOTH primary and secondary channels prior to passing control to the OS during resume from S3 state (STR). This ensures that the pending IDE interrupt(s) are cleared when the control is passed to the OS. The registers are located in I/O space via BM_BASE register (Bus0:D31;Function-1:Register 20-23h)

at offset 02h and offset 0Ah, respectively. Failure to do this may result in system hang when the OS starts executing resume sequence from S3 (STR) under certain conditions. These conditions include a combination of the following:

- Only a single channel of IDE is enabled (either Primary or Secondary)

- Native IDE Mode capability is reported by the BIOS

-OS is capable of dynamically switching from Legacy IDE Mode to Native IDE Mode.

A system hang may occur if there exists a pending IDE interrupt status bit during the legacy IDE Mode to Native Mode sequence, the OS may not clear the IDE interrupt(s), resulting in an apparent hang condition (interrupt storm).

10. THRMTRIP#

The following note is added to the end of section 5.12.8.5.

Note: A CPU thermal trip event will set the AFTERG3_EN bit, clear the PWRBTN_STS bit, clear the GPE0_EN & GPE1_EN register bits, and clear the SMB_WAK_STS bit only if SMB_WAK_STS was set due to SMBus slave receiving message and not set due to SMBAlert.

11. Primary and Secondary IDE Status Register

System BIOS must clear the Interrupt Status bit (bit-7) in Bus Master IDE Status Register for BOTH primary and secondary channels before returning from an INT 13 read or write command. This ensures that the pending IDE interrupt(s) are cleared before exiting the routine. The registers are located in I/O space via BM_BASE register (Bus0:Device31;Function1;Register20-23h) at offset 02h and 0Ah, respectively.

A system hang may occur of there exists a pending IDE interrupt status bit during Native IDE read/write operations resulting in an apparent hang condition (interrupt storm).

12. PCI Master Requirement

Add the following Note to section 5.1.1 (PCI Bus Interface)

Note: PCI bus masters should not use memory area locations as a target if that area is programmed to be anything but Read/Write.

13. SMBus Byte Done Status Clarification

The note associated with the Byte Done Status bit in Section 13.2.1 Host Status is being replaced with the following:

Note: When the last byte of a block message is received, the host controller will set this bit. However, it will not immediately set the INTR bit (bit-1 in this register). When the INTR bit is set. Thus, for a block message of n-bytes, the Intel® ICH4 may generate n+1 interrupts. The interrupt handler needs to be implemented to handle these cases.

14. CTS Bit Clarification

The following note is added to bit-3 of GEN_PMCON_2 register in section 9.8.1.2.

Note: The CF9 reset in the description refers to CF9h type core well reset which includes SYSRST#, PWROK, SMBus hard reset, TCO Timeout. This type of reset will clear the CTS bit.

15. PERR# Implementation

The ICH4 does not escalate a data parity mismatch reported by a PCI device (PERR#) across the PCI-to-PCI bridge. The PCI Specification or P2P bridge spec does not require PERR# escalation across PCI-to-PCI bridge.

For certain applications, it may be desirable to generate an SMI or NMI upon PERR# assertion by a PCI device. The device/driver is expected to handle such situations by retrying the transactions or escalation to the OS via device driver. Alternatively, external circuitry can be added to platforms to drive SMI or NMI upon PERR# assertion.

16. Port 63/65/67 Clarification

Table 6-2 (Fixed I/O Ranges Decoded by Intel(R) ICH4 incorrectly lists ports 63, 65 and 67 as addresses decoded by the processor I/F. These addresses are entirely removed from this table.

17. GPI ACPI Clarification

Section 5.12.6.3 incorrectly indicates that some GPIs, specifically GPI[7:0] are not ACPI compliant when they actually are. The paragraph above Table 5-42 and Table 5-42 are changed as indicated:

“It is important to understand that the various GPIs have different levels of functionality when used as wake events. The GPIs that reside in the core power well can only generate wake events from an S1 state. Table 5-42 summarizes the use of GPIs as wake events.”

GPI	Power Well	Wake From	Notes
GPI[7:0]	Core	S1	ACPI Compliant
GPI[13:11, 8]	Suspend	S1-S5	ACPI Compliant

18. USB CONFIGFLAG Clarification

The paragraph associated with Section 12.2.2.8 (CONFIGFLAG - Configure Flag Register) is completely replaced with the paragraph below:

This register is in the suspend power well. It is only reset by hardware when the suspend power is initially applied or in response to a host controller reset.

19. CTS Clarification

The following note is added to the description of the CTS bit (Section 9.8.1.2):

Note: The CF9h reset in this description refers to the CF9h type core well reset which includes SYS_RESET#, PWROK/VRMPWRGD low, SMBus hard reset, and TCO timeout. This type of reset will clear the CTS bit.

20. GPIO Note Change

The following is added to Note 1 of Table 5-51 (GPIO Implementation); “and therefore may be subject to further design constraints.”

21. GPI_ROUT Clarification

Add to the GPI_ROUT register bit description (Section 9.8.1.5 bits 1:0): “Software must set this bit field to generate the appropriate type of interrupt, depending on how the SCI_EN bit is set. For example, if the SCI_EN bit is set, then this field must be programmed to 00b or 10b. If the SCO_EN bit is cleared, then this field must be programmed to 00b or 01b. Software must also update this field if the SCI_EN bit is changed.”

22. LPC Cycle Clarification

The following changes are made to Table 5-2 LPC Cycle Types Supported in section 5.3.1.1:

- “See Note 1” is removed from the comment column for both I/O Read and I/O Write cycle types.”
- “See Note 1 is added to the comment column for both Memory Read and Memory Write cycle types.”

§

Documentation Changes

1. PCI Device Revision ID

PCI Revision ID Register Values (PCI Offset 08h) for all ICH4 functions are shown below.

This information is not found in the datasheet. This is the standard reference document.

Table 2. PCI Device Revision ID Table

Device Function	Description	ICH4 Dev ID	A1 Rev ID	B0 Rev ID	Comments
D30, F0	P2P Bridge	244Eh	81h	82h	
D31, F0	P2L Bridge	24C0h	01h	02h	
D31, F1	IDE	24CBh	01h	02h	
D31, F3	SMBus	24C3h	01h	02h	
D31, F5	AC '97 Audio	24C5h	01h	02h	
D31, F6	AC '97 Modem	24C6h	01h	02h	
D8, F0	LAN	103Ah	81h[1]	82h	
D29, F0	USB UHCI #1	24C2h	01h	02h	
D29, F1	USB UHCI #2	24C4h	01h	02h	
D29, F2	USB UHCI #3	24C7h	01h	02h	
D29, F7	USB EHCI	24CDh	01h	02h	

NOTE:
1. Loaded from EEPROM. If EEPROM contains either 0000h or FFFFh in the device ID location, then 103Ah is used. Lan Device ID's correspond to each of the PHY types listed:
   1039h 82562ET/EZ,
   103Ah 82562ET/EZ (CNR),
   103Bh 82562EM/EX,
   103Ch 82562EM/EX (CNR),

2. GPIO Table

- Replace Table 5-51 (GPIO Implementation with the following table:

GPIO	Type	Alternate Function (1)	Power Well	Tolerant	Notes
GPI[0]	Input Only	REQ[A]#	Core	5.0 V	• GPIO_USE_SEL bit 0 enables REQ/GNT[A]# pair. • Input active status read from GPE0_STS register bit 0. • Input active high/low set through GPI_INV register bit 0.

GPIO	Type	Alternate Function (1)	Power Well	Tolerant	Notes
GPI[1]	Input Only	REQ[B]# or REQ[5]#	Core	5.0 V	• GPIO_USE_SEL bit 1 enables REQ/GNT[B]# pair (34). • Input active status read from GPE0_STS register bit 1. • Input active high/low set through GPI_INV register bit 1.
GPI[2:5]	Input Only	PIRQ[E:H]#	Core	5.0 V	• GPIO_USE_SEL bits [2:5] enable PIRQ[E:H]#. • Input active status read from GPE0_STS register bits [2:5]. • Input active high/low set through GPI_INV register bits [2:5].
GPI[6]	Input Only	Unmuxed	Core	5.0 V	• Input active status read from GPE0_STS register bit 6. • Input active high/low set through GPI_INV register bit 6.
GPI[7]	Input Only	Unmuxed	Core	5.0 V	• Input active status read from GPE0_STS register bit 7. • Input active high/low set through GPI_INV register bit 7
GPI[8]	Input Only	Unmuxed	Resume	3.3 V	• Input active status read from GPE0_STS register bit 8. • Input active high/low set through GPI_INV register bit 8.
GPIO[9:10]	N/A	N/A	N/A		• Not implemented
GPI[11]	Input Only	SMBALERT#	Resume	3.3 V	• GPIO_USE_SEL bit 11 enables SMBALERT# • Input active status read from GPE0_STS register bit 11. • Input active high/low set through GPI_INV register bit 11.
GPI[12]	Input Only	Unmuxed	Resume	3.3 V	• Input active status read from GPE0_STS register bit 12. • Input active high/low set through GPI_INV register bit 12.
GPI[13]	Input Only	Unmuxed	Resume	3.3 V	• Input active status read from GPE0_STS register bit 13. • Input active high/low set through GPI_INV register bit 13.
GPIO[14:15]	N/A	N/A	N/A		• Not Implemented
GPO[16]	Output Only	GNT[A]#	Core	3.3 V	• Output controlled via GP_LVL register bit 16. • TTL driver output
GPO[17]	Output Only	GNT[B]# or GNT[5]#	Core	3.3 V	• Output controlled via GP_LVL register bit 17. • TTL driver output
GPO[18]	Output Only	Unmuxed	Core	3.3 V	• Output controlled via GP_LVL register bits [18]. • TTL driver output
GPO[19]	Output Only	Unmuxed	Core	3.3 V	• Output controlled via GP_LVL register bits [19]. • TTL driver output
GPO[20]	Output Only	Unmuxed	Core	3.3 V	• Output controlled via GP_LVL register bit 20. • TTL driver output

GPIO	Type	Alternate Function (1)	Power Well	Tolerant	Notes
GPO[21]	Output Only	Unmuxed	Core	3.3 V	• This GPO defaults high. • Output controlled via GP_LVL register bit 21. • TTL driver output
GPO[22]	Output Only	Unmuxed	Core	3.3 V	• Output controlled via GP_LVL register bit [22]. • Open-drain output
GPIO[23	Output Only	Unmuxed	Core	3.3 V	• Output controlled via GP_LVL register bit [23]. • TTL driver output
GPIO[24]	I/O	Unmuxed	Resume	3.3 V	• Input active status read from GP_LVL register bit 24. • Output controlled via GP_LVL register bit 24. • TTL driver output
GPIO[25]	I/O	Unmuxed	Resume	3.3 V	• Blink enabled via GPO_BLINK register bit 25. • Input active status read from GP_LVL register bit 25 • Output controlled via GP_LVL register bit 25. • TTL driver output
GPIO[26]	N/A	N/A	N/A		• Not implemented
GPIO[27:28]	I/O	Unmuxed	Resume	3.3 V	• Input active status read from GP_LVL register bits [27:28] • Output controlled via GP_LVL register bits [27:28] • TTL driver output
GPIO[29:31]	N/A	N/A	N/A		• Not implemented
GPIO[32:43]	I/O	Unmuxed	Core	3.3 V	

3. TCO Timer

- Section 9.9.1 incorrectly lists TCO1_RLD as the register name for TCOBase+00h. This register is correctly named TCO_RLD - “TCO Timer Reload and Current Value Register”. This is an 8-bit register, thus the correct default value of this register is 00h.
- Section 9.9.2 incorrectly lists TCO1_TMR as the register name for TCOBase+01h. This register is correctly named TCO_TMR - “TCO Timer Initial Value Register”. This is an 8-bit register, thus the correct default value of this register is 04h. The description of bits 5:0 incorrectly indicates that “Values of 0-3 are ignored and should not be attempted”. Only values of 0-1 are actually ignored.
- Section 9.9.3 incorrectly lists TCO1_DAT_IN as the register name for TCOBase+02h. This register is correctly named TCO_DAT_IN - “TCO Data In Register”. This is an 8-bit register, thus the correct default value of this register is 00h. The last sentence of the description of this register is changed to: “Writes to this register will cause an SMI and set the SW_TCO_SMI bit in the TCO1_STS register.”
- Section 9.9.4 incorrectly lists TCO1_DAT_OUT as the register name for TCOBase+03h. This register is correctly named TCO_DAT_OUT - “TCO Data Out Register”. This is an 8-bit register, thus the correct default value is 00h.

4. USB PORTSC Correction

Section 11.2.7 describes the PORTSC[0,1] - Port Status and Control Register. Bit-9 (Port Reset) is incorrectly shown as being RO (Read Only) when it is actually R/W (Read/Write).

5. GPIO[22]

Table 3-4 incorrectly lists GPIO[22] as High-Z Immediately after PCIRST#/RSMRST#. This pin is actually driven low after reset.

6. Frequency Strap Correction

Section 5.11.3, Table 5-33 indicates that FREQ_STRAP is at D31:F0;D4h when it is actually at D5h (BACK_CNTL). Additionally, the sentence “The ICH4 will hold these signals for 120 ns after CPURST# is deasserted by the Host Controller.” is removed.

7. Prefetch Flush Enable

Section 8.1.27,CNF ICH4 Configuration Register, bit-13 is defined as follows:

13	**Prefetch Flush Enable** — R/W. When set, this bit causes CPU to PCI logic to only deliver “Demand” data for a delayed transaction if a CPU to PCI write has occurred since the delayed transaction was initiated. This bit must be set by system BIOS.

8. TCO_STS Bit Correction

Section 9.8.3.13 describes the TCO_STS, bit-13 of PMBASE+34h (SMI Status Register). It is incorrectly shown as RO (Read Only). It is actually R/WC (Read/Write Clear). The following note is added to TCO_STS bit.

Note: This bit is cleared by writing a 1 to this bit position.

9. Power Sequencing

Table 17-19, *Power Sequencing and Reset Signal Timings* has the following corrections:

The parameter of t173 is changed to read: “VccSus Supplies active to LAN_RST# high, RSMRST# high”

The parameter of t176 is changed to read: “Vcc3_3, Vcc1_5, VccHI supplies active to PWROK, VRMPWRGD active”

The parameter of t184 is changed to read: “V_CPU_IO active to STPCLK# and CPUSLP# inactive, and processor Frequency Strap signals high”.

10. IDE Section Corrections

Section 5.15.1.2 incorrectly refers to Table 5-53 in two places. This reference is changed to Table 5-52.1. Table 5-52.1, *IDE Legacy I/O Ports: Control Block Registers (CS3x# Chip Select*, is now defined below:

I/O Offset	Register Function (Read)	Register Function (Write)
00h	Reserved	Reserved
01h	Reserved	Reserved
02h	Alt Status	Device Control
03h	Forward to LPC - Not claimed by IDE	Forward to LPC - Not claimed by IDE

11. IDE Interrupt Status bit

Section 10.2.2 describes the BMIS[P,S] - Bus Master IDE Status Register. Bit-7 is now defined as follows:

Bit	Description
7	**Interrupt Status - R/WC** 0 =This bit is cleared by software writing "1" to the bit position. If this bit is cleared while the interrupt is still active, this bit will remain clear until another assertion edge is detected on the interrupt line. 1 = This bit is set when the host controller executes a PRD that has its PRD_INT bit set. When this bit is cleared by software, the interrupt is cleared.

12. Section 9.7.5 Correction

Section 9.7.5 Reset Control Register, bit-1 incorrectly refers to the term "EDS" which is replaced with the term "datasheet."

13. USB Overcurrent Correction

The first bullet of section 5.16 incorrectly indicates that unused overcurrent signals can be used as GPI's. This first bullet is replaced as follows:

"Overcurrent detection on all six USB ports is supported. The overcurrent inputs are 5 V tolerant."

14. Figure 2-2 (RTC Circuit) Correction

The following note is added to the list of notes inside of Figure 2-2 to be consistent with requirements: Note 10. Diodes are Schottky.

15. PME Wake Doc Change

The following changes are made to Section 5.12.6.3, Table 5-41:

Note 1 is changed to "This is a wake event from S5 only if the sleep state was entered by setting the SLP_EN and SLP_TYP bits via software or from a power failure."

Note 4 is added: "This is a wake event from S5 only if the sleep state was entered by setting the SLP_EN and SLP_TYP bits via software."

The note associated with GPI:[0:n] is changed from Note 1 to Note 4.

The following changes are made to Section 5.12.6.4:

The last sentence of the third paragraph is changed to read: "There are four possible events that will wake the system after a power failure."

Add a fourth item: PME: PME_STS or PME_B0_STS, if enabled, will wake the system from S5 if S5 is entered from an AC power failure or if entered by a write to the SLP_TYP and SLP_EN registers.

The following changes are made to Section 9.8.3.7:

The third sentence of the description for PME_B0_STS is changed to: “If the PME_B0_STS bit is set, and the system is in an S1-S4 state (or S5 state due to SLP_TYP and SLP_EN or due to return from AC power failure), then the setting of the PME_B0_STS will generate a wake event, and an SCI (or SMI# if SCI_EN is not set) will be generated.”

The third sentence of the description for PME_STS is changed to: “If the PME_STS bit is set, and the system is in an S1-S4 state (or S5 state due to SLP_TYP and SLP_EN or due to return from AC power failure), then the setting of the PME_STS will generate a wake event, and an SCI will be generated.”

The following changes are made to Section 9.8.3.8:

The second sentence of the description for PME_EN is changed to: “PME can be a wake event from the S1-S4 state or from S5 (if entered via SLP_EN or from AC power recovery, but not power button override).

16. APM I/O Decode Correction

The second sentence of Section 9.8.2 (APM I/O Decode) is changed to read “This register space cannot be moved (fixed I/O location).”

17. Memory Map Table Change

The last row of the table (Table 6-4 of Section 6.4 Memory Map) is being replaced as follows:

Memory Range	Target	Dependency/Comments
All other	PCI	Any memory range access that makes it to the ICH4’s PCI bus and is not specified in one of the D31:F0; 0xE0-0xEF registers or below 16M will be master aborted on PCI.

18. SMBus Host_Busy Correction

Section 12.2.1 HST_STS - Host Status Register is being corrected. Specifically, bit-0 Host_Busy is corrected to read as follows:

0 = Cleared by the ICH4 when the current transaction is completed.

1 = Indicates that the ICH4 is running a command from the host interface. No SMB registers should be accessed while this bit is set, except the BLOCK DATA BYTE or LAST BYTE registers. The BLOCK DATA BYTE and LAST BYTE registers can be accessed when this bit is set only when the SMB_CMD bit in the Host Control Register are programmed for Block command or I^2C Read command. This is necessary in order to check the DONE_STS bit.

19. GEN2_DEC Correction

The description for Generic I/O Decode Range 2 Base Address (GEN2_DEC) in section 9.1.33, changes to “This address is aligned on a 16-byte boundary and must have address lines 31:16 as ‘0’. The note remains unchanged.

20. THRMTRIP# Timing Correction

The THRMTRIP# active to SLP_S3#, SLP_S4#, SLP_S5# active time ($t220_{MAX}$) is corrected from 2 PCICLK periods to 3 PCICLK periods.

21. USB Port Number Documentation Corrections

In section 5.17.10.1.3, the description of bits 20:23 of the EHCI Host Controller Structural Parameters register indicates an incorrect value for these bits. The sentence is changed to:

"This 4-bit field represents the numeric value assigned to the debug port (i.e., 0001 = port 0)."

The PWAKE_CAP.Port Wake Up Capability Mask (section 12.1.25) bit description is changed to the following:

Bit	Description
6:1	**Port Wake Up Capability Mask** — R/W. Bit positions 1 through 6 correspond to a physical port implemented on this host controller. For example, bit position 1 corresponds to port 0, bit position 2 corresponds to port 1, etc.

22. GPIO[13:11] & GPIO[8:0] Documentation Clarification

In section 5.14.2, the reference to GP_LVL register for selecting GPIO[1:15] active level is incorrect. The paragraph is changed to the following:

"GPIO[13:11] & GPIO[8:0] have "sticky" bits on the input. Refer to the GPE0_STS register. As long as the signal goes active for at least two clocks, the ICH4 will keep the sticky status bit active. The active status of these GPIOs can be read from the corresponding bits in the GPE0_STS register."