Intel® 815EM Chipset: 82815EM Graphics and Memory Controller Hub (GMCH2-M)

Datasheet

April 2003

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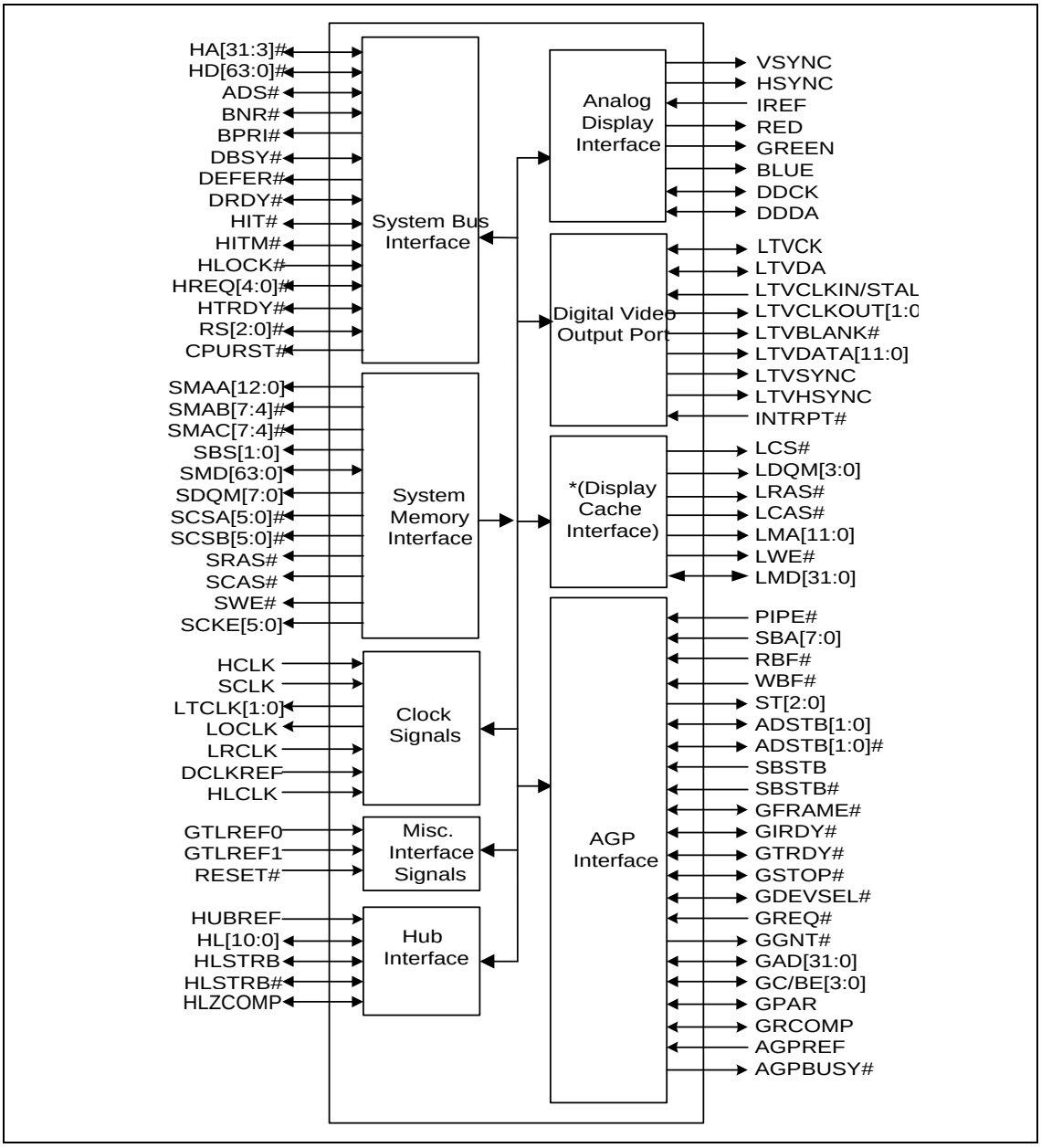
Revision History

Rev.	Description	Date
-001	Initial Release	January 2000
-002	Updates include: • Removed XOR chain testing information • Added component ID information	April 2003

Intel® 82815EM GMCH2-M Features

- Processor/Host Bus Support
  - Optimized for the mobile Intel® Pentium® III processor and mobile Intel® Celeron™ processors.
  - Supports 32-Bit System Bus Addressing
  - 4 deep in-order queue; 4 or 1 deep request queue
  - Supports Uni-processor systems only
  - In-order and Dynamic Deferred Transaction Support
  - 100MHz System Bus Frequency
  - GTL+ I/O Buffer
- Integrated SDRAM Controller
  - 32 to 512MB using 16/64/128/256 Mbit technology
  - Supports up to 3 double sided SO-DIMMs @ 100Mhz
  - 64-bit data interface
  - 100MHz system memory bus frequency
  - Support for Asymmetrical SDRAM addressing only
  - Support for x8 and x16 SDRAM device width
  - Unbuffered, Non-ECC SDRAM only supported
  - Refresh Mechanism: CBR supported
  - Enhanced Open page Arbitration SDRAM paging scheme
  - Suspend to RAM support
- Accelerated Graphics Port (AGP) Interface Multiplexed with Internal Graphics
  - Supports a **single** AGP device
  - Supports AGP 2.0 including 4x AGP data transfers
  - AGP 2.0 support via dual mode buffers to allow 3.3v or 1.5v signaling
  - AGP PIPE# or SBA initiated accesses to SDRAM are **not** snooped
  - AGP FRAME# initiated accesses to SDRAM are snooped
  - High priority access support
  - Hierarchical PCI configuration mechanism
  - Delayed transaction support for AGP-to-SDRAM reads that can not be serviced immediately
- Arbitration Scheme and Concurrency
  - Intelligent Centralized Arbitration Model for Optimum Concurrency Support
  - Concurrent operations of processor and System busses supported via dedicated arbitration and data buffering
- Data Buffering
  - Distributed Data Buffering Model for optimum concurrency
  - SDRAM Write Buffer with read-around-write capability
  - Dedicated processor-SDRAM, hub interface-SDRAM and Graphics-SDRAM Read Buffers
- Power Management Functions
  - SMRAM space remapping to A0000h (128 KB)
  - Optional Extended SMRAM space above 256 MB, additional 512K/1MB TSEG from Top of Memory, cacheable
  - Stop Clock Grant and Halt special cycle translation from the host to the hub interface
  - ACPI Compliant power management
  - Dynamic (independent) SCKE support
  - AGPBUSY# support
  - APIC Buffer Management
- Integrated Graphics Controller Multiplexed with AGP Controller
  - 3D Hyper Pipelined Architecture
  - Parallel Data Processing (PDP)
  - Precise Pixel Interpolation (PPI)
  - Full 2D H/W Acceleration
  - Motion Video Acceleration
- 3D Graphics Visual Enhancements
  - Flat & Gouraud Shading
  - Mip Maps with Trilinear and Anisotropic Filtering
  - Full Color Specular
  - Fogging Atmospheric Effects
  - Z Buffering
  - 3D Pipe 2D Clipping
  - Backface Culling
- 3D Graphics Texturing Enhancements
  - Per Pixel Perspective Correction Texture Mapping
  - Texture Compositing
  - Texture Color Keying/Chroma Keying
- Digital Video Output Port (DVO)
  - Support for an external TV encoder
  - Video Controller Hub (VCH) Interface
  - 196 Pin mini-BGA package
- Display
  - Integrated 24-bit 230MHz RAMDAC
  - Gamma Corrected Video
  - DDC2B Compliant
- 2D Graphics
  - Up to 1600x1200 in 8-bit Color at 75 Hz Refresh
  - Hardware Accelerated Functions
  - 3 Operand Raster BitBLTs
  - 64x64x3 Color Transparent Cursor
  - Hardware Cursor and Popup window support
- Arithmetic Stretch Blitter Video
  - H/W Assisted Motion Compensation for MPEG2 Decode
  - H/W assisted DVD playback at 30fps
  - H/W Overlay Engine with Bilinear Filtering
  - Independent gamma correction, saturation, brightness & contrast for overlay
- Integrated Graphics Memory Controller
  - Intel® D.V.M. Technology
- Display Cache Interface
  - 32-bit data interface
  - 100/133MHz SDRAM interface
  - Support for 2 1Mx16, or 1 2Mx32 SDRAM
  - 4MB max addressable
- Supporting I/O Bridge
  - 360 Pin eBGA I/O Controller Hub (ICH2-M)
- Packaging/Power
  - 544 BGA
  - 1.8V core with 3.3V CMOS I/O

Intel® 815EM Chipset GMCH2-M Simplified Block Diagram



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1. Overview

The Intel® 815EM chipset is a high-flexibility chipset designed to extend from the basic graphics / multimedia mobile PC platform up to the mainstream performance mobile PC platform. The Intel® 815EM chipset consists of a Graphics and Memory Controller Hub (GMCH2-M) Bridge and an I/O Controller Hub (ICH2-M) Bridge for the I/O subsystem.

The GMCH2-M integrates a Display Cache SDRAM controller that supports a 32-bit 100MHz SDRAM array for enhanced integrated 3D graphics performance. Multiplexed with the display cache interface is an AGP controller interface to enable graphics configuration and upgrade flexibility with the Intel® 815EM chipset. The AGP interface and the internal graphics device are mutually exclusive. When the AGP port is populated with an AGP graphics device, the integrated graphics is disabled and thus the display cache interface is not needed.

In this document the terms "GMCH2-M" and "Intel® 815EM chipset" refer to the Intel® 815EM chipset Graphics and Memory Controller Hub interchangeably, unless otherwise specified. Also the term GFX and internal graphics device refers to the Intel® 815EM chipset internal graphics device, unless otherwise specified.

The Intel® 815EM chipset may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata are available on request.

1.1. Component Identification via Programming Interface

The Intel® 815EM Chipset may be identified by the following register contents:

Stepping	Vendor ID[1]	Device ID[2]	Revision Number[3]
A0	8086h	1130h	10h
A1	8086h	1130h	11h

NOTES:

1. The Vendor ID corresponds to bits 15-0 of the Vendor ID Register located at offset 00-01h in the PCI function 0 configuration space.
2. The Device ID corresponds to bits 15-0 of the Device ID Register located at offset 02-03h in the PCI function 0 configuration space.
3. The Revision Number correspond to bits 7-0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space.

1.2. Component Marking Information

The Intel® 815EM Chipset may be identified by the following component markings:

Stepping	Q-Spec	S-Spec	Top Marking	Notes
A0	QA38	N/A	FW82815EM	
A1	QA75	SL4MP	FW82815EM	

1.3. The Intel® 815EM Chipset System

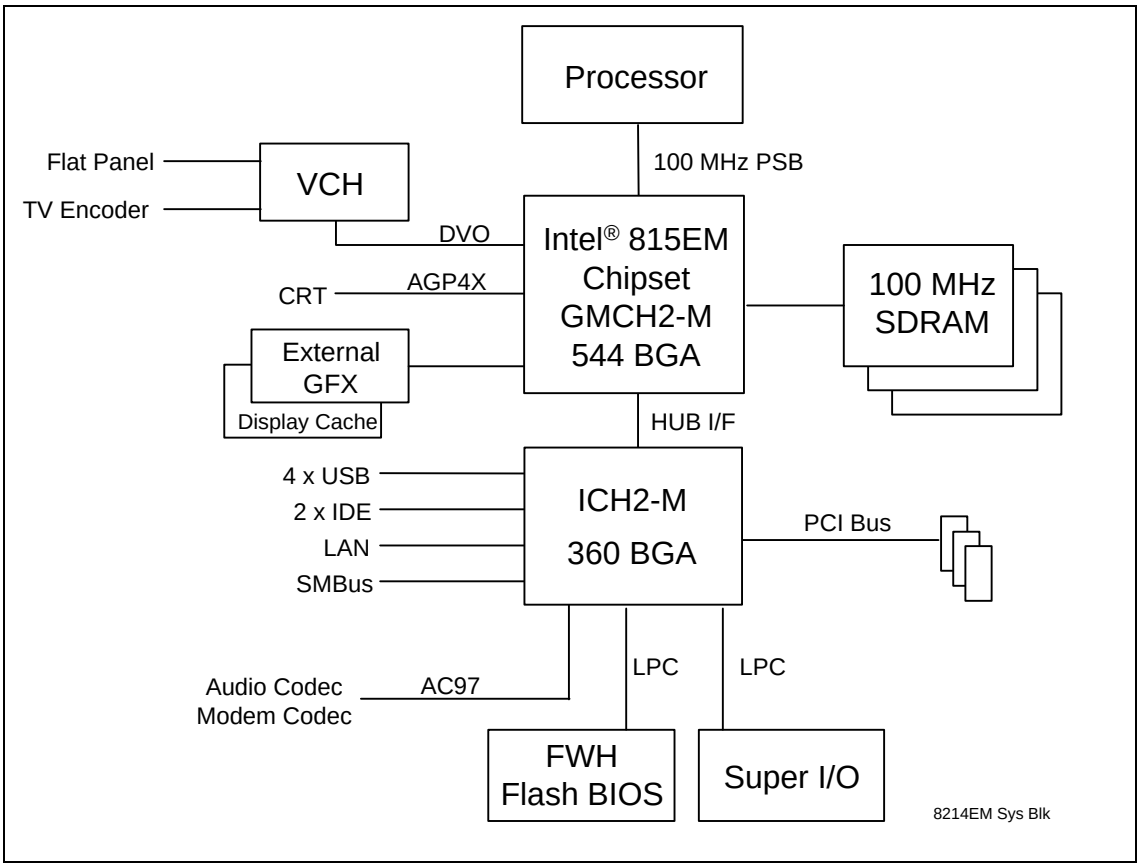
The Intel® 815EM chipset uses a hub architecture with the GMCH2-M as the host bridge hub and the I/O Controller Hub (ICH2-M) as the I/O hub. The ICH2-M is a highly integrated multifunctional I/O Controller Hub that provides the interface to the PCI Bus and integrates many of the functions needed in today's PC platforms. The Intel® 815EM chipset GMCH2-M and ICH2-M communicate over a dedicated hub interface.

ICH2-M functions and capabilities include:

- PCI Rev 2.2 compliant with support for 33 MHz PCI operations
- ICH2-M supports up to 6 Req/Gnt pairs (PCI bus)
- Power Management Logic Support
- Enhanced DMA Controller, Interrupt Controller & Timer Functions
- Integrated IDE controller; ICH2-M supports Ultra ATA/66/100
- USB host interface with support for four USB ports
- System Management Bus (SMBus) compatible with most I2C devices
- AC'97 2.1 Compliant Link for Audio and Telephony CODECs
- Low Pin Count (LPC) interface
- Firmware Hub (FWH) interface support
- Alert On LAN*

The following figure shows a block diagram of the typical mobile platform based on the Intel® 815EM chipset. The GMCH2-M supports processor bus frequencies of 100MHz. The ICH2-M provides extensive I/O support. The ICH2-M provides support for 6 PCI bus Req/Gnt pairs, increased IDE capability from Ultra ATA/33 to Ultra ATA/100, and Alert On LAN*.

Figure 1. Intel® 815EM Chipset System Block Diagram



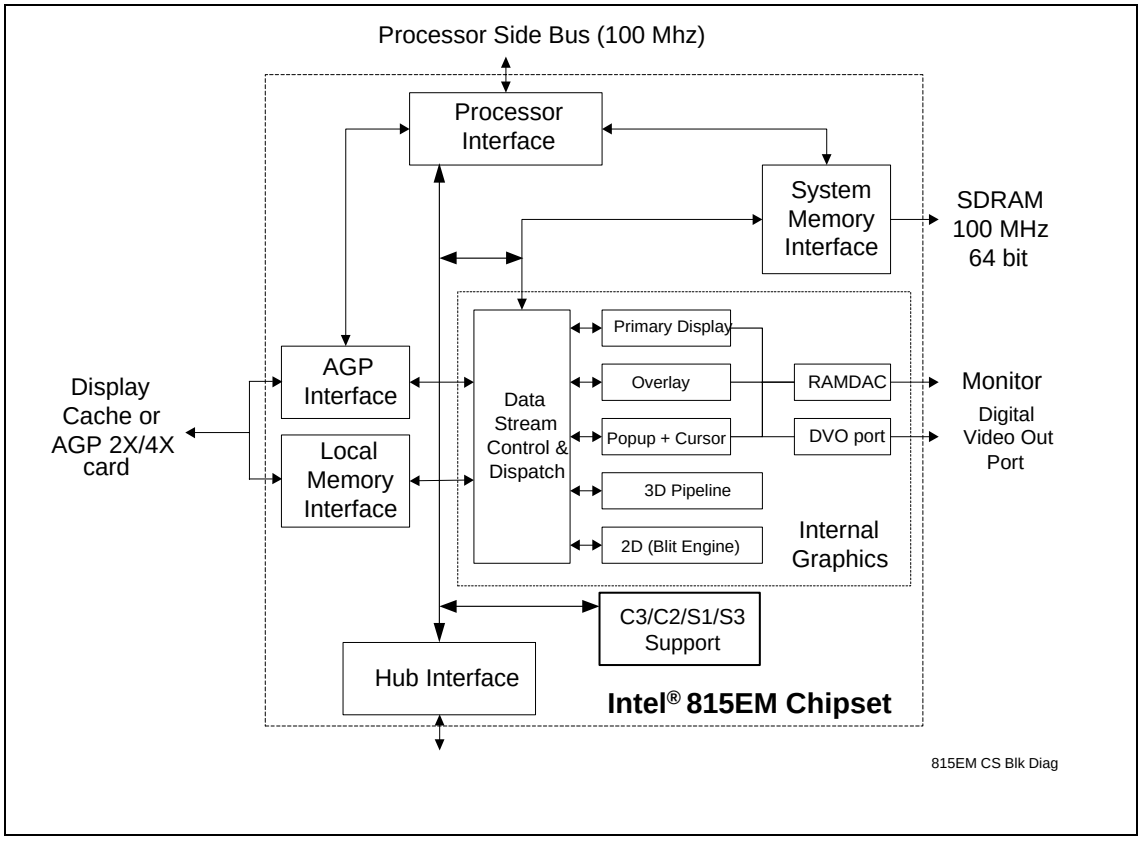
1.4. Intel® 815EM Chipset GMCH2-M Overview

Figure 1 is a block diagram of the Intel® 815EM chipset. The Intel® 815EM chipset GMCH2-M functions and capabilities include:

Support for a single processor configuration

- 64-bit GTL+ based Processor Side Bus Interface at 100 MHz
- 32-bit Host Address Support
- 64-bit System Memory Interface with optimized support for SDRAM at 100 MHz
- Integrated 2D & 3D Graphics Engines
- Integrated H/W Assisted Motion Compensation Engine
- Integrated 230 MHz DAC
- Digital Video Out (DVO) Interface Port to communicate to VCH for mobile LVDS flat panel interface support and TV encoder support
- Communicates to ICH2-M via Hub interface
- Local memory Display Cache at 100/133 MHz
- 2X/4X AGP Controller Port
- ACPI 1.0 power management

Figure 2. Intel® 815EM Chipset GMCH2-M Block Diagram



1.5. Host Interface

The host interface of the Intel® 815EM chipset GMCH2-M is optimized to support the mobile Intel® Pentium® III processor, and the mobile Intel® Celeron™ processor in uBGA and uPGA packages. The GMCH2-M implements the host address, control, and data bus interfaces within a single device. The GMCH2-M supports a 4-deep in-order queue (i.e., supports pipelining of up to four outstanding transaction requests on the host bus). Host bus addresses are decoded by the GMCH2-M for access to system memory, PCI memory, I/O (via hub interface), PCI configuration space and Graphics memory. The GMCH2-M takes advantage of the pipelined addressing capability of the processor to improve the overall system performance.

1.6. System Memory Interface

The Intel® 815EM chipset GMCH2-M integrates a system memory controller that supports a 64-bit, 100-MHz SDRAM array. The only DRAM type supported is industry standard Synchronous DRAM (SDRAM). The SDRAM controller interface is fully configurable through a set of control registers. Complete descriptions of these registers will be available in a future revision of this document.

The GMCH2-M supports industry standard 64-bit wide DIMMs for desktop platforms and SO-DIMMs for mobile platforms with SDRAM devices. The twelve multiplexed address lines, SMAA[12:0], along with the two bank select lines, SBS[1:0], allow the GMCH2-M to support 2M, 4M, 8M, and 16M x64 DIMMs. Only asymmetric addressing is supported. The GMCH2-M has 12 SCS# lines enabling the support of up to six 64-bit rows of SDRAM. The GMCH2-M targets SDRAM with CL2 and CL3 and supports both single and double-sided DIMMs for desktop and SO-DIMMs for mobile platforms. Additionally, the GMCH2-M also provides a seven deep refresh queue. The GMCH2-M can be configured to keep multiple pages open within the memory array. Pages can be kept open in any one bank of memory.

SCKE[5:0] is used in configurations requiring powerdown mode for the SDRAM. Each SCKE can be dynamically powerdown if not in use. This scheme will save significant amount of power since only one SO-DIMM at any given time will be functional and all the rest will be powered down.

1.7. Multiplexed AGP and Display Cache Interface

The Intel® 815EM chipset GMCH2-M multiplexes a display cache interface for internal graphics 3D performance improvement with an AGP controller interface. The Display Cache is used only in the internal graphics. When an AGP card is populated in the system, the Intel® 815EM chipset GMCH2-M internal graphics will be disabled and the AGP controller enabled.

1.8. AGP Interface

A single AGP port is supported by the GMCH2-M AGP interface. The AGP buffers operate in one of two selectable modes:

- 3.3V drive, **not** 5 volt safe - This mode is compliant to the AGP 1.0 and 2.0 specs.
- 1.5V drive, **not** 3.3 volt safe - This mode is compliant with the AGP 2.0 spec.

The following table shows the AGP Data Rate and the Signaling Levels supported by the GMCH2-M:

Table 1. AGP Data Rate and Signaling Levels

	Signaling Level	
Data Rate	1.5v	3.3v
1x AGP	Yes	Yes
2x AGP	Yes	Yes
4x AGP	Yes	No

The AGP interface supports 4x AGP signaling. AGP semantic (PIPE# or SBA[7:0]) cycles to SDRAM are not snooped on the host bus. AGP FRAME# cycles to SDRAM are snooped on the host bus. The GMCH2-M supports PIPE# or SBA[7:0] AGP address mechanisms, but not both simultaneously. Either the PIPE# or the SBA[7:0] mechanism must be selected during system initialization. High priority accesses are supported. Only memory writes from the hub interface to AGP are allowed. No transactions from AGP to the hub interface are allowed.

1.8.1. Display Cache Interface

The Intel® 815EM chipset integrates a Display Cache SDRAM controller for enhanced 3D performance. The maximum memory support is 4 MB. The Display Cache Interface is multiplexed with the AGP controller interface to provide options for both the value mobile segment and main stream performance platforms configuration with the Intel® 815EM chipset. When the AGP port is populated with an AGP graphics device the integrated graphics is disabled and thus the display cache interface is not needed.

The Intel® 815EM chipset GMCH2-M supports a Display Cache SDRAM controller with a 32-bit 133MHz SDRAM array. The DRAM type supported is industry standard Synchronous DRAM (SDRAM) like that of the system memory. The local memory SDRAM controller interface is fully configurable through a set of control registers. For more details on the registers, consult the *Extensions to the Pentium® Pro Processor BIOS Writer's Guide* Revision 3.6 and higher.

1.9. Hub Interface

The hub interface is a private interconnect between the GMCH2-M and the ICH2-M.

1.10. GMCH2-M Integrated Graphics (GFX) Support

The GMCH2-M includes a highly integrated 2D/3D graphics accelerator (GFX) and is PC99a compliant. Its architecture consists of dedicated multi-media engines executing in parallel to deliver high performance graphics and video capabilities which includes integrated 3D graphics engine, 2D graphics engine, video engine, display pipeline, and motion compensation HW accelerator.

The 3D and 2D engines are managed by a 3D/2D pipeline preprocessor allowing a sustained flow of graphics data to be rendered and displayed. The deeply pipelined 3D accelerator engine provides 3D graphics quality and performance via per-pixel 3D rendering and parallel data paths which allow each pipeline stage to simultaneously operate on different primitives or portions of the same primitive. The GMCH2-M graphics accelerator engine supports perspective-correct texture mapping, trilinear and anisotropic filtering, Mip-Mapping, Gouraud shading, alpha-blending, fogging and Z-buffering. A rich set of 3D instructions permit these features to be independently enabled or disabled.

The GMCH2-M integrated graphics accelerator's 2D capabilities include BLT and arithmetic STRBLT engines, a hardware cursor, a popup window and an extensive set of 2D registers and instructions. The high performance 64-bit BitBLT engine provides hardware acceleration for many common Windows operations.

In addition to its 2D/3D capabilities, the GMCH2-M integrated graphics accelerator also supports full MPEG-2 motion compensation for software-assisted DVD video playback, a VESA DDC2B compliant display interface and a digital video out port to interface to the VCH for panel support.

1.10.1. Intel® Dynamic Video Memory Technology (D.V.M.T.)

The internal graphics device on the GMCH2-M supports Intel® Dynamic Video Memory Technology. Intel® D.V.M.T. dynamically responds to application requirements by allocating the proper amount of display and texturing memory taken from system memory. For the GMCH2-M, a Display Cache (DC) can be used for Z-buffers (Textures and display buffer are located in system memory). If the display cache is not used, the Z-buffer is located in system memory.

1.10.2. Display

The GMCH2-M provides interfaces to a standard progressive scan monitor. This interface is only active when running in internal graphics mode. The Intel® 815EM chipset GMCH2-M directly drives a standard progressive scan monitor up to a resolution of 1600x1200 pixels.

1.10.3. Digital Video Out Port (DVO)

The GMCH2-M provides a Digital Video Out port to connect to the Video Controller Hub (VCH) to connect to CMOS or LVDS flat panel interfaces. The interface has 1.8V signaling to allow it to operate at higher frequencies. The VCH also has an interface to connect to a TV encoder. The TV encoder must support the DVO interface.

1.11. System Clocking

The GMCH2-M has a new type of clocking architecture. It has integrated SDRAM buffers that runs at 100 MHz, regardless of processor side bus frequency. The GMCH2-M uses a 48-MHz clock as the reference clock (DCLKREF) input for the graphics pixel clock PLL.

1.12. GMCH2-M Power Delivery

The GMCH2-M core voltage is 1.8V. System Memory runs off of a 3.3V supply. Display cache memory runs off of the AGP 3.3V supply. AGP 1X/2X I/O can run off of either a 3.3V or a 1.5V supply. AGP 4X I/O requires a 1.5V supply. The AGP interface voltage is determined by the VDDQ generation on the motherboard.

1.13. References

- GTL+ I/O Specification: Contained in the Pentium® II Processor Databook
- PCI Local *bus Specification 2.2*: Contact www.pcisig.com

2. Signal Description

This section provides a detailed description of the Intel® 815EM chipset GMCH2-M signals. The signals are arranged in functional groups according to their associated interface. The states of all of the signals during reset are provided in the System Reset section.

The "#" symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level. When "#" is not present after the signal name the signal is asserted when at the high voltage level.

The following notations are used to describe the signal type:

I	Input pin
O	Output pin
I/OD	Input / Open Drain Output pin. This pin requires a pullup 3.3V.
I/O	Bi-directional Input/Output pin
s/t/s	Sustained Tristate. This pin is driven to its inactive state prior to tri-stating.
as/t/s	Active Sustained Tristate. This applies to some of the hub interface signals. This pin is weakly driven to its last driven value.

The signal description also includes the type of buffer used for the particular signal:

GTL+	Open Drain GTL+ interface signal. Refer to the GTL+ I/O Specification for complete details. These signals will be actively driven high for a short period of time to assist timing when the Intel® 815EM chipset is configured for 100-MHz Host interface. GTL+ signals are inverted bus signals where a low voltage represents a logical "1".
AGP	AGP interface signals. These signals can be programmed to be compatible with AGP 2.0 3.3V or 1.5V Signaling Environment DC and AC Specifications. In 3.3V mode the buffers are not 5V tolerant. In 1.5V mode the buffers are not 3.3V tolerant.
CMOS	The CMOS buffers are Low Voltage TTL compatible signals. These are 3.3V only.
LVTTL	Low Voltage TTL compatible signals. There are 3.3V only.
1.8V	1.8V signals for the digital video interface
Analog	Analog CRT Signals

Note: That the processor address and data bus signals (Host Interface) are logically inverted signals (i.e., the actual values are inverted of what appears on the processor bus). This must be taken into account and the addresses and data bus signals must be inverted inside the Intel® 815EM chipset GMCH2-M. All processor control signals follow normal convention. A 0 indicates an active level (low voltage) if the

signal is followed by # symbol and a 1 indicates an active level (high voltage) if the signal has no # suffix.

The following table shows the Vtt/Vdd and Vref levels for the various interfaces:

Table 2. Voltage Levels for Each Interface

Interface	Vtt/Vdd (nominal)	Vref
GTL+	1.5v	2/3 * Vtt
AGP	1.5v 3.3v	1.5v: 0.5 * Vagpdd 3.3v: 0.4 * Vagpdd
Hub Interface	1.8v	0.5 * Vdd

2.1. Host Interface Signals

Signal Name	Type	Description
CPURST#	O GTL+	**CPU Reset:** The GMCH2-M asserts CPURST# while RESET# (PCIRST# from ICH2-M) is asserted and for approximately 1ms after RESET# is deasserted. The GMCH2-M also pulses CPURST# for approximately 1ms when requested via a hub interface special cycle. The CPURST# allows the processor to begin execution in a known state.
HA [31:3]#	I/O GTL+	**Host Address Bus:** HA[31:3]# connect to the processor address bus. During processor cycles, HA[31:3]# are inputs. The GMCH2-M drives HA[31:3]# during snoop cycles on behalf of Primary PCI. Note that the address bus is inverted on the processor bus. A low value on HA[15]# sampled at the rising edge of CPURST# informs the processor to support Quick-Start stop clock mode. If HA[15]# is sampled high at CPURST# rising edge, it informs the processor to support Stop-Grant mode.
HD [63:0]#	I/O GTL+	**Host Data:** These signals are connected to the processor data bus. Note that the data signals are inverted on the processor bus.
ADS#	I/O GTL+	**Address Strobe:** The processor bus owner asserts ADS# to indicate the first of two cycles of a *request phase*.
BNR#	I/O GTL+	**Block Next Request:** Used to block the current request bus owner from issuing a new request. This signal is used to dynamically control the processor bus pipeline depth.
BPRI#	O GTL+	**Priority Agent Bus Request:** The GMCH2-M is the only Priority Agent on the processor bus. It asserts this signal to obtain the ownership of the address bus. This signal has priority over symmetric bus requests and will cause the current symmetric owner to stop issuing new transactions unless the HLOCK# signal was asserted.
DBSY#	I/O GTL+	**Data Bus Busy:** Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
DEFER#	O GTL+	**Defer:** The GMCH2-M will generate a deferred response as defined by the rules of the GMCH2-M dynamic defer policy. The GMCH2-M will also use the DEFER# signal to indicate a processor retry response.
DRDY#	I/O GTL+	**Data Ready:** Asserted for each cycle that data is transferred.
HIT#	I/O GTL+	**Hit:** Indicates that a caching agent holds an unmodified version of the requested line. Also driven in conjunction with HITM# by the target to extend the snoop window.

Signal Name	Type	Description
HITM#	I/O GTL+	**Hit Modified:** Indicates that a caching agent holds a modified version of the requested line and that this agent assumes responsibility for providing the line. HITM# is also driven in conjunction with HIT# to extend the snoop window.
HLOCK#	I GTL+	**Host Lock:** All processor bus cycles sampled with the assertion of HLOCK# and ADS#, until the negation of HLOCK# must be atomic (i.e. no Hub interface or GMCH2-M graphics snoopable access to SDRAM is allowed when HLOCK# is asserted by the processor).
HREQ [4:0]#	I/O GTL+	**Host Request Command:** Asserted during both clocks of request phase. In the first clock, the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second clock, the signals carry additional information to define the complete transaction type. The transactions supported by the GMCH2-M are defined in the Host Interface section of this document.
HTRDY#	I/O GTL+	**Host Target Ready:** Indicates that the target of the processor transaction is able to enter the data transfer phase.
RS [2:0]#	I/O GTL+	**Response Signals:** Indicates type of response as shown below: **RS[2:0] Response type** 000 Idle state 001 Retry response 010 Deferred response 011 Reserved (not driven by the GMCH2-M) 100 Hard Failure (not driven by the GMCH2-M) 101 No data response 110 Implicit Writeback 111 Normal data response
GTLREF[1:0]	I	**GTL Reference:** Reference voltage input for the Host GTL+ interface. GTLREF is 2/3* VTT. VTT is nominally 1.5v.

2.2. System Memory Interface Signals

Signal Name	Type	Description
SMAA [12:0] SMAB [7:4]# SMAC [7:4]#	O CMOS	**Memory Address:** SMAA [12:0], SMAB [7:4]#, and SMAC [7:4]# are used to provide the multiplexed row and column address to SDRAM. SMAB[7:4]# and SMAC[7:4]# are inverted (180 degrees out of phase) versions of SMAA[7:4]. SMAC[5]# is default high when sampled for the 815EM to drive HA[15]# high at CPURST# deassertion time to indicate to the processor to support C2 Stop-Grant mode. When SMAC[5]# is sampled low, the 815EM will drive HA[15]# low at CPURST# deassertion time for the processor to support C2 Quick-Start mode.
SBS[1:0]	O CMOS	**Memory Bank Select:** These signals define the banks that are selected within each DRAM row. The SMAn and SBS signals combine to address every possible location within a DRAM device. SBS[1:0] may be heavily loaded and require 2 SDRAM clock cycles for setup time to the SDRAM's. For this reason, all chip select signals (SCSA[5:0]# and SCSB[5:0]#) must be deasserted on any SDRAM clock cycle that one of these signals change.
SMD [63:0]	I/O CMOS	**Memory Data:** These signals are used to interface to the SDRAM data bus.
SDQM [7:0]	O CMOS	**Input/Output Data Mask:** These pins act as synchronized output enables during read cycles and as a byte enables during write cycles.
SCSA [5:0]# SCSB [5:0]#	O CMOS	**Chip Select:** For the memory row configured with SDRAM, these pins perform the function of selecting the particular SDRAM components during the active state.
SRAS#	O CMOS	**SDRAM Row Address Strobe:** These signals drive the SDRAM array directly without any external buffers.
SCAS#	O CMOS	**SDRAM Column Address Strobe:** These signals drive the SDRAM array directly without any external buffers.
SWE#	O CMOS	**Write Enable Signal:** SWE# is asserted during writes to SDRAM.
SCKE [5:0]	O CMOS	**System Memory Clock Enable:** SCKE SDRAM Clock Enable is used to signal a self-refresh or power-down command to an SDRAM array when entering system suspend. SCKE is also used to dynamically power down inactive SDRAM rows.
SRCOMP	I/O	**System Memory RCOMP:** Used to calibrate the System memory I/O buffers.

2.3. AGP Interface Signals

For more details on the operation of these signals, refer to the AGP Interface Specification Revision 2.0. Some of the AGP interfaces are multiplexed with Display Cache interface signals. AGP interface signals only function as documented in this section when Intel® 815EM chipset AGP interface is enabled (Intel® 815EM chipset integrated graphics disabled). Refer to Section 2.12 for multiplexing map of AGP to Display Cache interface signals.

2.3.1. AGP Addressing Signals

There are two mechanisms by which the AGP master can enqueue AGP requests: PIPE# and SBA (side-band addressing). Upon initialization, one of the methods is chosen. The master may not switch methods

without a full reset of the system. When *PIPE#* is used to enqueue addresses, the master is not allowed to queue addresses using the SBA bus. For example, during configuration time, if the master indicates that it can use either mechanism, the configuration software will indicate which mechanism the master will use. Once this choice has been made, the master will continue to use the mechanism selected until the system is reset (and reprogrammed) to use the other mode. This change of modes is not a dynamic mechanism but rather a static decision when the device is first being configured after reset.

Signal Name	Type	Description
PIPE#	I AGP	**Pipeline Read** **During PIPE# Operation:** This signal is asserted by the AGP master to indicate a full-width address is to be enqueued on by the target using the AD bus. One address is placed in the AGP request queue on each rising clock edge while PIPE# is asserted. **During SBA Operation:** This signal is not used if SBA (Side Band Addressing) is selected. **During FRAME# Operation:** This signal is not used during AGP FRAME# operation.
SBA[7:0]	I AGP	**Side-band Addressing** **During PIPE# Operation:** These signals are not used during PIPE# operation. **During SBA Operation:** These signals (the SBA, or side-band addressing, bus) are used by the AGP master (graphics component) to place addresses into the AGP request queue. The SBA bus and AD bus operate independently. That is, transactions can proceed on the SBA bus and the AD bus simultaneously. **During FRAME# Operation:** These signals are not used during AGP FRAME# operation.

2.3.2. AGP Flow Control Signals

Signal Name	Type	Description
RBF#	I AGP	**Read Buffer Full** **During PIPE# and SBA Operation**: Read buffer full indicates if the master is ready to accept previously requested low priority read data. When RBF# is asserted the GMCH2-M is not allowed to initiate the return low priority read data. That is, the GMCH2-M can finish returning the data for the request currently being serviced, however it cannot begin returning data for the next request. RBF# is only sampled at the beginning of a cycle. If the AGP master is always ready to accept return read data then it is not required to implement this signal. **During FRAME# Operation:** This signal is not used during FRAME# operation.
WBF#	I AGP	**Write-Buffer Full** **During PIPE# and SBA Operation**: Write buffer full indicates if the master is ready to accept Fast Write data from the GMCH2-M. **Intel® 815EM chipset does not support the use of AGP Fast Writes.** If the AGP master is always ready to accept fast write data then it is not required to implement this signal. **During FRAME# Operation:** This signal is not used during FRAME# operation.
GMCK	I/OD CMOS	**GMBus**: When configured by register GMBUS[2:0], GMCK becomes a bidirectional clock signal between master GMCH2-M and slave VCH.

2.3.3. AGP Status Signals

Signal Name	Type	Description
ST[2:0]	O AGP	**Status Bus** **During PIPE# and SBA Operation:** Provides information from the arbiter to a AGP Master on what it may do. ST[2:0] only have meaning to the master when its GNT# is asserted. When GNT# is deasserted these signals have no meaning and must be ignored. Refer to the AGP Interface Specificaiton revision 2.0 for further explanation of the ST[2:0] values and their meanings. **During FRAME# Operation:** These signals are not used during FRAME# based operation; except that a '111' indicates that the master may begin a FRAME# transaction.

2.3.4. AGP Clocking Signals - Strobes

Signal Name	Type	Description
ADSTB0	I/O s/t/s AGP	**AD Bus Strobe-0** **During 2X Operation:** During 2X operation, this signal provides timing for the **GAD[15:0]** and **GCBE[1:0]#** signals. The agent that is providing the data will drive this signal. **During 4X Operation:** During 4X operation, this is one-half of a differential strobe pair that provides timing information for **GAD[15:0]** and **GCBE[1:0]#** signals.
ADSTB0#	I/O s/t/s AGP	**AD Bus Strobe-0 Compliment** **During 2X Operation:** During 2X operation, this signal is not used. **During 4X Operation:** During 4X operation, this is one-half of a differential strobe pair that provides timing information for **GAD[15:0]** and **GCBE[1:0]#** signals. The agent that is providing the data will drive this signal.
ADSTB1	I/O s/t/s AGP	**AD Bus Strobe-1** **During 2X Operation:** During 2X operation, this signal provides timing for **AD[16:31]** and **C/BE[2:3]#** signals. The agent that is providing the data will drive this signal. **During 4X Operation:** During 4X operation, this is one-half of a differential strobe pair that provides timing information for the **GAD[16:31]** and **GCBE[2:3]#** signals. The agent that is providing the data will drive this signal.
ADSTB1#	I/O s/t/s AGP	**AD Bus Strobe-1 Compliment** **During 2X Operation:** During 2X operation, this signal is not used **During 4X Operation:** During 4X operation, this is one-half of a differential strobe pair that provides timing information for the **GAD[16:31]** and **GCBE[2:3]#** signals. The agent that is providing the data will drive this signal.
SBSTB	I AGP	**SBA Bus Strobe** **During 2X Operation:** During 2X operation, this signal provides timing for the **SBA** bus signals. The agent that is driving the SBA bus will drive this signal. **During 4X Operation:** During 4X operation, this is one-half of a differential strobe pair that provides timing information for the **SBA** bus signals. The agent that is driving the SBA bus will drive this signal.
SBSTB#	I AGP	**SBA Bus Strobe Compliment** **During 2X Operation:** During 2X operation, this signal is not used. **During 4X Operation:** During 4X operation, this is one-half of a differential strobe pair that provides timing information for the SBA bus signals. The agent that is driving the SBA bus will drive this signal.
GRCOMP	I/O	**AGP RCOMP:** Used to calibrate AGP I/O buffers. This signal pin must be connected to a PCB trace representative of the AGP bus data signal traces but sufficiently long to present a long shelf before signal reflection occurs. The AGP buffers are calibrated based on the measured shelf voltage.
AGPREF	I	**AGP Reference:** Reference voltage input for the AGP interface. AGPREF should be 0.4*VDD_{AGP} when VDD is 3.3V, or 0.5* VDD_{AGP} when VDD is 1.5V.

2.3.5. AGP FRAME# Signals

Signal Name	Type	Description
GFRAME#	I/O s/t/s AGP	**FRAME:** **During PIPE# and SBA Operation:** Not used by AGP SBA and PIPE# operation. **During FRAME# Operation:** GFRAME# is an output when the GMCH2-M acts as an initiator on the AGP Interface. GFRAME# is asserted by the GMCH2-M to indicate the beginning and duration of an access. GFRAME# is an input when the GMCH2-M acts as a FRAME# based AGP target. As a FRAME# based AGP target, the GMCH2-M latches the C/BE[3:0]# and the AD[31:0] signals on the first clock edge on which it samples FRAME# active.
GIRDY#	I/O s/t/s AGP	***Initiator Ready:*** During PIPE# and SBA Operation: Not used while enqueueing requests via AGP SBA and PIPE#, but used during the data phase of PIPE# and SBA transactions. GIRDY# indicates the AGP compliant master is ready to provide *all* write data for the current transaction. Once IRDY# is asserted for a write operation, the master is not allowed to insert wait states. The assertion of IRDY# for reads indicates that the master is ready to transfer to a subsequent block (32 bytes) of read data. The master is *never* allowed to insert a wait state during the initial data transfer (32 bytes) of a read transaction. However, it may insert wait states after each 32 byte block is transferred. (There is no relationship between GFRAME# and GIRDY# for AGP transactions.)
GTRDY#	I/O s/t/s AGP	***Target Ready:*** During PIPE# and SBA Operation: Not used while enqueueing requests via AGP SBA and PIPE#, but used during the data phase of PIPE# and SBA transactions. GTRDY# indicates the AGP compliant target is ready to provide read data for the entire transaction (when the transfer size is less than or equal to 32 bytes). In write case, it is ready to transfer the initial or subsequent block (32 bytes) of data when the transfer size is greater than 32 bytes. The target is allowed to insert wait states at the end of each block data transfer(32 bytes). Each 32-byte block is transferred on both read and write transactions.
GSTOP#	I/O s/t/s AGP	***Stop****:* During PIPE# and SBA Operation:This signal is not used for PIPE# or SBA operation. During FRAME# Operation: STOP# is an input when the GMCH2-M acts as a FRAME# based AGP initiator and an output when the GMCH2-M acts as a FRAME# based AGP target. STOP# is used for disconnect, retry, and abort sequences on the AGP interface.
GDEVSEL#	I/O s/t/s AGP	***Device Select:*** During PIPE# and SBA Operation:This signal is not used during PIPE# or SBA operation. During FRAME# Operation: GDEVSEL#, when asserted, indicates that a FRAME# based AGP target device has decoded its address as the target of the current access. The GMCH2-M asserts GDEVSEL# based on the SDRAM address range being accessed by a PCI initiator. As an input it indicates whether any device on the bus has been selected.
GREQ#	I AGP	***Request****:* During SBA Operation: This signal is not used during SBA operation. During PIPE# and FRAME# Operation: GREQ#, when asserted, indicates that a FRAME# or PIPE# based AGP master is requesting use of the AGP interface.

Signal Name	Type	Description
GGNT#	O AGP	***Grant***: During SBA, PIPE# and FRAME# Operation: GGNT**#** along with the information on the ST[2:0] signals (status bus) indicates how the AGP interface will be used next. Refer to the AGP Interface Specificaiton revision 2.0 for further explanation of the ST[2:0] values and their meanings.
GMDA	I/OD CMOS	**GMBUS**: When configured by register GMBUS[2:0], GMDA becomes a bidirectional I/O data signal between master GMCH2-M and slave VCH.
GAD [31:0]	I/O AGP	***Address/Data Bus***: During PIPE# and FRAME# Operation: GAD[31:0] are used to transfer both address and data information on the AGP inteface. During SBA Operation: GAD[31:0] are used to transfer data on the AGP interface.
GCBE [3:0]#	I/O AGP	***Command/Byte Enable:*** During FRAME# Operation: During the address phase of a transaction, GCBE[3:0]# define the bus command. During the data phase GCBE[3:0]# are used as byte enables. The byte enables determine which byte lanes carry meaningful data. The commands issued on the GCBE# signals during FRAME# based AGP are the same GCBE# command described in the PCI 2.1 and 2.2 specifications. During PIPE# Operation: When an address is enqueued using PIPE#, the C/BE# signals carry command information. Refer to the AGP 2.0 Interface Specification Revision 2.0 for the definition of these commands. The command encoding used during PIPE# based AGP is **DIFFERENT** than the command encoding used during FRAME# based AGP cycles (or standard PCI cycles on a PCI bus). During SBA Operation: These signals are not used during SBA operation.
GPAR	I/O AGP	***Parity***: During FRAME# Operation: GPAR is driven by the GMCH2-M when it acts as a FRAME# based AGP initiator during address and data phases for a write cycle, and during the address phase for a read cycle. GPAR is driven by the GMCH2-M when it acts as a FRAME# based AGP target during each data phase of a FRAME# based AGP memory read cycle. Even parity is generated across GAD[31:0] and GCBE[3:0]#. During SBA and PIPE# Operation: This signal is not used during SBA and PIPE# operation.

NOTES:
1. LOCK#, SERR#, and PERR# signals are not supported on the AGP Interface (even for PCI operations).
2. PCI signals described in this table behave according to PCI 2.1 specifications when used to perform PCI transactions on the AGP interface.

2.3.6. AGP C3 support Signals

The following pin is associated with ACPI C3 support.

Signal Name	Type	Description
AGPBUSY#	OD CMOS	**AGP Bus Busy:** This signal is generated either by the AGP Graphics Chip in AGP mode or by the GMCH2-M in graphics mode, but not by both. This is an input to the ICH2-M. In AGP mode, Asserted (active low): When asserted, AGPBUSY# indicates that the AGP device is currently busy and requests that the system not transition to the C3 state. However, assertion of AGPBUSY# does not guarantee that the system will not enter the C3 state or perform an Intel® SpeedStep™ technology transition. If system is in C3 state, then the assertion of AGPBUSY# is used to request that the system exit from the C3 state. The AGP GC must assert AGPBUSY# whenever the AGP GC has a pending request to use the AGP interface. The AGP GC must assert AGPBUSY# regardless of which protocol it intends to use on the AGP interface: SBA, PIPE#, or PCI. AGPBUSY# may only be asserted by the AGP GC when AGPBUSY# is in the D0 state and should not be asserted in the D1, D2, or D3 states. Deasserted (high): When deasserted, AGPBUSY# indicates that the AGP device is not busy and has no need to use the AGP interface. In Graphics mode, Asserted (active low): When asserted, AGPBUSY# indicates the internal graphics unit is requesting snoop or having interrupt request to be serviced. Therefore, it requests that the system not transition to the C3 state. However, assertion of AGPBUSY# does not guarantee that the system will not enter the C3 state or perform an Intel® SpeedStep™ technology transition. If system is in C3 state, then the assertion of AGPBUSY# is used to request that the system exit from the C3 state. Deasserted (high): When deasserted, AGPBUSY# indicates the internal graphics unit has no pending snoop request nor graphics interrupt request.

2.4. Display Cache Interface Signals

Some of the Display Cache interface signals are multiplexed with AGP interface signals. Display Cache interface signals only function as documented in this section when Intel® 815EM chipset integrated graphics is enabled (Intel® 815EM chipset AGP interface disabled). Refer to Section 2.12 for multiplexing map of AGP to Display Cache interface signals.

Signal Name	Type	Description
LCS#	O CMOS	**Chip Select:** For the memory row configured with SDRAM, this pin performs the function of selecting the particular SDRAM components during the active state.
LDQM[3:0]	O AGP	**Input/Output Data Mask:** These pins control the memory array and act as synchronized output enables during read cycles and as a byte enables during write cycles.
LRAS#	O CMOS	**SDRAM Row Address Strobe:** The LRAS# signal is used to generate SDRAM Command encoded on LRAS#/LCAS#/LWE# signals. When LRAS# is sampled active at the rising edge of the SDRAM clock, the row address is latched into the SDRAMs.
LCAS#	O CMOS	**SDRAM Column Address Strobe:** The LSCAS# signal is used to generate SDRAM Command encoded on LSRAS#/LSCAS#/LWE# signals. When LSCAS# is sampled active at the rising edge of the SDRAM clock, the column address is latched into the SDRAMs.
LMA[11:0]	O AGP	**Memory Address:** LMA[11:0] is used to provide the multiplexed row and column address to SDRAM.
LWE#	O CMOS	**Write Enable Signal:** LWE# is asserted during writes to SDRAM.
LMD[31:0]	I/O AGP	**Memory Data:** These signals are used to interface to the SDRAM data bus of SDRAM array.
L_FSEL	I CMOS	**Display Cache Frequency Select:** This signal indicates whether the display cache is to run at 100MHz or 133MHz. The value of this pin is sampled at de-assertion of CPURST# to determine display cache frequency. HIGH = 133MHz (Default) LOW = 100MHz Note: L_FSEL has a weak internal pull-up enabled during reset. Note: 100MHz display cache is a non-validated feature and should be implemented only if OEM performs validation specifically on this feature.

2.5. Hub Interface Signals

Signal Name	Type	Description
HL[10:0]	I/O	**Hub Interface Signals:** Signals used for the hub interface.
HLSTRB	I/O	**Packet Strobe:** One of two differential strobe signals used to transmit or receive packet data.
HLSTRB#	I/O	**Packet Strobe Compliment:** One of two differential strobe signals used to transmit or receive packet data.
HLREF	I Ref	**HUB reference:** Sets the differential voltage reference for the hub interface.

2.6. Display Interface Signals

Signal Name	Type	Description
VSYNC	O 3.3V	**CRT Vertical Synchronization:** This signal is used as the vertical sync (polarity is programmable) or " Vsync Interval".
HSYNC	O 3.3V	**CRT Horizontal Synchronization:** This signal is used as the horizontal sync (polarity is programmable) or " Hsync Interval".
IWASTE	I Ref	**Waste Reference:** This signal must be tied to ground.
IREF	I Ref	**Set pointer resistor for the internal color palette DAC.** A 174 ohm 1% resistor is recommended
RED	O Analog	**CRT Analog video output from the internal color palette DAC:** The DAC is designed for a 37.5 ohms equivalent load on each pin (e.g. 75 ohms resistor on the board, in parallel with the 75 ohms CRT load)
GREEN	O Analog	**CRT Analog video output from the internal color palette DAC:** The DAC is designed for a 37.5 ohms equivalent load on each pin (e.g. 75 ohms resistor on the board, in parallel with the 75 ohms CRT load)
BLUE	O Analog	**CRT Analog video output from the internal color palette DAC:** The DAC is designed for a 37.5 ohms equivalent load on each pin (e.g., 75 ohms resistor on the board, in parallel with the 75 ohms CRT load)
DDCK	I/O CMOS	**CRT Monitor DDC Interface Clock:** (Also referred to as VESA™ "Display Data Channel", also referred to as the "Monitor Plug-n-Play" interface.) For DDC1, DDCK and DDDA provide a unidirectional channel for Extended Display ID. For DDC2, DDCK and DDDA can be used to establish a bi-directional channel based on I^2C protocol. The host can request Extended Display ID or Video Display Interface information over the DDC2 channel.
DDDA	I/O CMOS	**CRT Monitor DDC Interface Data:** See DDCK Description

2.7. Digital Video Output Signals/TV-Out Pins

Signal Name	Type	Description
LTVCLKIN/STALL (DVOCLKIN)	I 1.8V	**Low Voltage TV Clock In (TV-Out Mode):** In 1.8V TV-Out usage, the TVCLKIN pin functions as a pixel clock input to the GMCH2-M from the TV encoder. The TVCLKIN frequency ranges from 20MHz to 40MHz depending on the mode (e.g., NTSC or PAL) and the overscan compensation values in the TV Encoder. CLKIN has a worse case duty cycle of 60%/40% coming in to the GMCH2-M. **Flat Panel Interrupt (LCD Mode):** STALL flow control: This signal comes from the external VCH chip. This signal is asserted when VCH is not ready to take in display data from Intel® 815EM chipset.
LTVCLKOUT[1:0] (DVOCLKOUT[1:0])	O 1.8V	**LCD/TV Port Clock Out:** These pins provide a differential pair reference clock that can run up to 85MHz.
LTVBLANK# (DVOBLANK)	O 1.8V	**Flicker Blank or Border Period Indication:** BLANK# is a programmable output pin driven by the graphics control. When programmed as a blank period indication, this pin indicates active pixels excluding the border. When programmed as a border period indication, this pin indicates active pixel including the border pixels.
LTVDATA[11:0] (DVODATA[11:0])	O 1.8V	**LCD/TV Data:** These signals are used to interface to the LCD/TV-out data bus.
LTVVSYNC (DVOVSYNC)	O 1.8V	**Vertical Sync:** VSYNC signal for the LTV interface. The active polarity of the signal is programmable.
LTVHSYNC (DVOHSYNC)	O 1.8V	**Horizontal Sync:** HSYNC signal for the LTV interface. The active polarity of the signal is programmable.
LTVCK (DVOI2CCLK)	I/OD CMOS	**LCD/TV Clock:** Clock pin for 2-wire interface.
LTVDA (DVOI2CDATA)	I/OD CMOS	**LCD/TV Data:** Data pin for 2-wire interface.
INTRPT# (DVOINT#)	I CMOS	**INTRPT#:** This dedicated pin indicates an interrupt when low. This is used to support display device hot plug.

2.8. Power Signals

Signal Name	Type	Description
V_1.8	Power	Core Power (1.8V)
VDDQ	Power	AGP I/O and Display Cache Buffer Supply Power
VSUS_3.3	Power	System Memory Buffer Power (Separate 3.3V power plane for power down modes)
VCCDA	Power	Display Power Signal (Connect to an isolated 1.8V plane with VCCDACA1 and VCCDACA2)
VCCDACA1	Power	Display Power Signal (Connect to an isolated 1.8V plane with VCCDA and VCCDACA2)
VCCBA	Power	AGP/Hub I/F Power (1.8V)
VCCDACA2	Power	Display Power Signal (Connect to an isolated 1.8V plane with VCCDA and VCCDACA1)
VCCDPLL	Power	System Memory PLL Power (1.8V)
VSSDA	Power	Display Ground Signal
VSSDACA	Power	Display Ground Signal
VSS	Power	Core Ground
VSSDPLL	Power	System Memory PLL Ground
VSSBA	Power	AGP/Hub I/F Ground

2.9. Clock Signals

Signal Name	Type	Description
HCLK	I CMOS	**Host Clock Input:** Clock used on the host interface. This pin receives a buffered host clock from the external clock synthesizer. Externally generated 100MHz clock. This clock goes to Intel® 815EM chipset PSB logic. This clock is also the reference for System Memory, Local Memory, and internal graphics core clocks. The clock synthesizer drives this to 2.5V.
SCLK	I CMOS	**System Memory Clock:** Clock used on the output buffers of system memory. Externally generated 100MHz clock.
LTCLK[1:0]	O CMOS	**Display Cache Transmit Clocks:** LTCLK[1:0] are internally generated display cache clocks used to clock the input buffers of the SDRAM devices.
LOCLK	O CMOS	**Output Clock:** LOCLK is an internally generated clock used to drive LRCLK.
LRCLK	I CMOS	**Receive Clock:** LRCLK is a display cache clock used to clock the input buffers of the GMCH2-M.
DCLKREF	I CMOS	**Display Interface Clock:** DCLKREF is a 48MHz clock generated by an external clock synthesizer to the GMCH2-M.
HLCLK	I CMOS	**Hub Interface Clock:** 66MHz hub interface clock generated by an external clock synthesizer.

2.10. Miscellaneous Interface Signals

Signal Name	Type	Description
RESET#	I	**Global Reset:** Driven by the ICH/ICH0 when PCIRST# is active.
Reserved		**Reserved for future use,** Needs to be connected to V_1.8 for backward compatiblity to GMCH2-M.
NC		**No Connect**

2.11. GMCH2-M Power-Up/Reset Strap Options

Pin Name	Strap Description	Configuration	Interface Type	Buffer Type
SBA[7]	Local Memory Frequency Select	High = 133MHz (default) Low = 100MHz	AGP/LM	Input
SCAS#	Host Frequency	High = Reserved Low = 100MHz	System Memory	Bi-directional
SMAA [11]	IOQ Depth	High = 4 (default) Low = 1	System Memory	Bi-directional
SMAA [10]	ALL Z	High = Normal Active Low	System Memory	Bi-directional
SMAA [9]	FSB P-MOS Kicker Enable	High = Reserved Low = Pentium® III processor and Celeron™ processor support	System Memory	Bi-directional
SMAC[5]#	Enable Quick Start Support	High = Stop-Grant Support (default) Low = Quick-Start Support	System Memory	Bi-directional

NOTES:
1. External reset signal used to sample the straps is Reset#.
2. All system memory reset straps have internal 50K ohm pull-ups during reset.

2.12. Multiplexed Display Cache and AGP Signal Mapping

Table 3. Display Cache and AGP signal Mapping

Local Memory Signal Name	AGP Signal Name
LCAS#	G_AD26
LCKE	G_AD24
LCS#	G_STOP#
LDQM0	G_AD0
LDQM1	G_AD10
LDQM2	SBA2
LDQM3	ST1
L_FSEL	SBA7
LMA0	G_GAD22
LMA1	G_AD15
LMA10	G_FRAME#
LMA11/LBA	G_AD18
LMA2	G_AD11
LMA3	G_BE0#
LMA4	G_AD9
LMA5	G_AD13
LMA6	G_PAR
LMA7	G_TRDY#
LMA8	G_AD16
LMA9	G_AD20
LMD0	G_AD8
LMD1	G_AD7
LMD10	G_BE1#
LMD11	G_DEVSEL#
LMD12	G_IRDY#
LMD13	G_BE2#
LMD14	G_AD17
LMD15	G_AD19

Local Memory Signal Name	AGP Signal Name
LMD16	G_AD21
LMD17	G_AD23
LMD18	G_AD25
LMD19	G_AD27
LMD2	G_AD5
LMD20	G_AD29
LMD21	G_AD31
LMD22	SBA6
LMD23	SBA4
LMD24	PIPE#
LMD25	SBA1
LMD26	SBA3
LMD27	G_REQ#
LMD28	ST0
LMD29	ST2
LMD3	G_AD3
LMD30	RBF#
LMD31	SBA0
LMD4	G_AD1
LMD5	G_AD6
LMD6	G_AD4
LMD7	G_AD2
LMD8	G_AD12
LMD9	G_AD14
LRAS#	G_BE3#
LTCLK0	G_AD30
LTCLK1	G_AD28
LWE#	SBA5

3. PCI Configuration Registers

This section describes the PCI Configuration Register set.

The GMCH2-M contains PCI configuration registers for Device 0 (Host-hub interface Bridge/DRAM Controller), Device 1 (AGP Bridge), and Device 2 (GMCH2-M internal graphics device).

The GMCH2-M also contains an extensive set of registers and instructions for controlling its graphics operations. Intel® graphics drivers provide the software interface at this architectural level. The register/instruction interface is transparent at the Application Programmers Interface (API) level and thus, beyond the scope of this document.

3.1. Register Nomenclature and Access Attributes

RO	**Read Only**. If a register is read only, writes to this register have no effect.
R/w	**Read/Write**. A register with this attribute can be read and written
R/WC	**Read/Write Clear**. A register bit with this attribute can be read and written. However, a write of a 1 clears (sets to 0) the corresponding bit and a write of a 0 has no effect.
R/WO	**Read/Write Once**. A register bit with this attribute can be written to only once after power up. After the first write, the bit becomes read only.
Reserved Bits	Some of the GMCH2-M registers described in this section contain reserved bits. These bits are labeled "Reserved" or "Intel® Reserved". Software must deal correctly with fields that are reserved. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions and then written back. Note the software does not need to perform read, merge, write operation for the configuration address register.
Reserved Registers	In addition to reserved bits within a register, the GMCH2-M contains address locations in the configuration space of the Host-hub interface Bridge/DRAM Controller and the internal graphics device entities that are marked either "Reserved" or Intel® Reserved". When a "Reserved" register location is read, a random value can be returned. ("Reserved" registers can be 8-, 16-, or 32-bit in size). Registers that are marked as "Reserved" must not be modified by system software. Writes to "Reserved" registers may cause system failure.
Default Value Upon Reset	Upon a Full Reset, the GMCH2-M sets all of its internal configuration registers to predetermined **default** states. Some register values at reset are determined by external strapping options. The default state represents the minimum functionality feature set required to successfully bring up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of the system initialization software (usually BIOS) to properly determine the DRAM configurations, operating parameters and optional system features that are applicable, and to program the GMCH2-M registers accordingly.

3.2. GMCH2-M Register Introduction

The GMCH2-M contains two sets of software accessible registers, accessed via the Host I/O address space:

- I/O mapped Control registers in the host I/O space: These register controls the access to PCI configuration space (see section entitled I/O Mapped Registers)
- Internal GMCH2-M configuration registers: These are partitioned into three logical device register sets (“logical” since they reside within a single physical device).
  - Device #0: Host-hub interface Bridge/DRAM Controller functionality controls PCI bus 0 such as PCI registers, DRAM configuration, other chip-set operating parameters and optional features.
  - Device #1: The second register block is dedicated to the AGP interface.
  - Device #2: The third block is dedicated to the internal graphics device (GFX) in the GMCH2-M.

The GMCH2-M supports PCI configuration space accesses using the mechanism denoted as Configuration Mechanism #1 in the PCI specification. The GMCH2-M internal registers (both I/O Mapped and Configuration registers) are accessible by the host. The registers can be accessed as Byte, Word (16-bit), or Dword (32-bit) quantities, with the exception of CONFIG_ADDRESS, which can only be accessed as a Dword. All multi-byte numeric fields use "little-endian" ordering (i.e., lower addresses contain the least significant parts of the field).

3.3. I/O Mapped Registers

The GMCH2-M contains two registers that reside in the processor I/O address space

- Configuration Address Register (CONFIG_ADDRESS):

  CONFIG_ADDRESS is a 32 bit register accessed only when referenced as a Dword. A Byte or Word reference will "pass through" the Configuration Address Register onto the PCI0 bus as an I/O cycle. The CONFIG_ADDRESS register contains the PCI Bus Number, PCI Device Number, PCI Function Number, and PCI Register Number for which a subsequent configuration access is intended. The register numbers, bit 7:2 in CONFIG_ADDRESS, is the upper 6 bits of the dword-aligned byte offset address of the selected dword.

- Configuration Data Register (CONFIG_DATA):

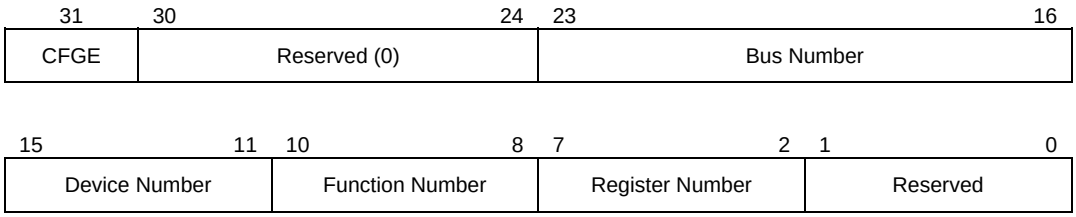
  CONFIG_DATA is a 32 bit Read/Write window into the specified dword of the pCI configuration space selected by CONFIG_ADDRESS. The portion of configuration space that is referenced by CONFIG_DATA is determined by the contents of CONFIG_ADDRESS. Reads and writes to the PCI Configuration space can be byte, word, or dword, via I/O read or write instructions to the CONFIG_DATA port.

The Configuration Address Register enables/disables the configuration space and determines what portion of configuration space is visible through the Configuration Data window.

3.3.1. CONFIG_ADDRESS—Configuration Address Register

I/O Address: 0CF8h Accessed as a DWord
Default Value: 00000000h
Access: Read/Write
Size: 32 bits

The CONFIG_ADDRESS register contains the Bus Number, Device Number, Function Number, and Register Number for which a subsequent configuration access is intended.



Bit	Descriptions
31	**Configuration Enable (CFGE).** When this bit is set to 1 accesses to PCI configuration space are enabled. If this bit is reset to 0 accesses to PCI configuration space are disabled.
30:24	**Reserved.** These bits are read only and have a value of 0.
23:16	**Bus Number.** When the Bus Number is programmed to 00h the target of the Configuration Cycle is one of the three devices in the GMCH2-M or the PCI Bus (the hub interface is logically a PCI bus) that is directly connected to the GMCH2-M, depending on the Device Number field. A Type 0 configuration cycle is generated on the hub interface if the Bus Number is programmed to 00h and the GMCH2-M is not the target. A Type 1 configuration cycle is generated on the hub interface if the Bus Number is non-zero, and is less than the value programmed into the SECONDARY BUS NUMBER or is greater than the value programmed into the SUBORDINATE BUS NUMBER Register. A Type 0 PCI configuration cycle is generated on the AGP bridge if the Bus Number is non-zero and matches the value programmed into the SECONDARY BUS NUMBER Register. A Type 1 PCI configuration cycle is generated on the AGP bridge if the Bus Number is non-zero, greater than the value in the SECONDARY BUS NUMBER register and less than or equal to the value programmed into the SUBORDINATE BUS NUMBER Register.

Bit	Descriptions
15:11	**Device Number.** This field selects one agent on the PCI bus selected by the Bus Number. During a Type 1 Configuration cycle this field is mapped to AD[15:11]. During a Type 0 Configuration Cycle this field is decoded and one bit among AD[31:11] is driven to a 1. The GMCH2-M is always Device Number 0 for the Host bridge (GMCH2-M) entity, The AGP bridge entity is always Device Number 1 and, The Internal Graphics Device entity is always Device number 2. If the Bus Number is non-zero and matches the value programmed into the SECONDARY BUS NUMBER Register a Type 0 PCI configuration cycle will be generated on the AGP bridge. The Device Number field is decoded and the GMCH2-M asserts one and only one GADxx signal as an IDSEL. GAD16 is asserted to access Device #0, GAD17 for Device #1, GAD18 for Device #2 and so forth up to Device #15 which will assert AD31. All device numbers higher than 15 cause a type 0 configuration access with no IDSEL asserted, which will result in a Master Abort reported in the GMCH2-M's "virtual" PCI-PCI bridge registers. For Bus Numbers resulting in hub interface configuration cycles the GMCH2-M propagates the Device Number field as A[15:11]. For Bus Numbers resulting in AGP bridge Type 1 Configuration cycles the Device Number is propagated as GAD[15:11].
10:8	**Function Number.** This field is mapped to AD[10:8] during PCIx configuration cycles. This allows the configuration registers of a particular function in a multi-function device to be accessed. The GMCH2-M only responds to configuration cycles with a function number of 000b; all other function number values attempting access to the GMCH2-M (Device Number = 0, 1 or 2, Bus Number = 0) will generate a master abort.
7:2	**Register Number.** This field selects one register within a particular Bus, Device, and Function as specified by the other fields in the Configuration Address Register. This field is mapped to AD[7:2] during PCI configuration cycles.
1:0	**Reserved.**

3.3.2. CONFIG_DATA—Configuration Data Register

I/O Address: 0CFCh
Default Value: 00000000h
Access: Read/Write
Size: 32 bits

CONFIG_DATA is a 32 bit Read/Write window into configuration space. The portion of configuration space that is referenced by CONFIG_DATA is determined by the contents of CONFIG_ADDRESS.

Bit	Descriptions
31:0	Configuration Data Window (CDW). If bit 31 of CONFIG_ADDRESS is 1 any I/O reference that falls in the CONFIG_DATA I/O space will be mapped to configuration space using the contents of CONFIG_ADDRESS.

3.4. PCI Bus Configuration Mechanism

The PCI Bus defines a slot based "configuration space" that allows each device to contain up to 8 functions with each function containing up to 256 8-bit configuration registers. The PCI specification defines two bus cycles to access the PCI configuration space: Configuration Read and Configuration Write. Memory and I/O spaces are supported directly by the processor. Configuration space is supported by a mapping mechanism implemented within the GMCH2-M.

The PCI specification defines two mechanisms to access configuration space, Mechanism #1 and Mechanism #2. The GMCH2-M supports only Mechanism #1. The configuration access mechanism makes use of the CONFIG_ADDRESS Register and CONFIG_DATA Register. To reference a configuration register a Dword I/O write cycle is used to place a value into CONFIG_ADDRESS that specifies the PCI bus, the device on that bus, the function within the device, and a specific configuration register of the device function being accessed. CONFIG_ADDRESS[31] must be 1 to enable a configuration cycle. CONFIG_DATA then becomes a window into the four bytes of configuration space specified by the contents of CONFIG_ADDRESS. Any read or write to CONFIG_DATA will result in the GMCH2-M translating the CONFIG_ADDRESS into the appropriate configuration cycle.

The GMCH2-M is responsible for translating and routing the processor I/O accesses to the CONFIG_ADDRESS and CONFIG_DATA registers to internal GMCH2-M configuration registers, the internal graphic device, or the hub interface.

3.5. PCI Configuration Space Access

The GMCH2-M and the ICH2-M are physically connected via the hub interface. From a configuration standpoint, the hub interface connecting the GMCH2-M and the ICH2-M is **logically PCI bus #0**. All devices internal to the GMCH2-M and ICH2-M appear to be on PCI bus #0. The system primary PCI expansion bus is physically attached to the ICH2-M and, from a configuration standpoint appears as a hierarchical PCI bus behind a PCI-to-PCI bridge. The primary PCI expansion bus connected to the ICH2-M has a programmable PCI Bus number.

The GMCH2-M contains three PCI devices within a single physical component. The configuration registers for both Devices 0, 1 and 2 are mapped as devices residing on PCI bus #0.

- Device 0: Host-hub interface Bridge/DRAM Controller.
- Device 1: AGP Bridge supporting 1X/2X/4X transactions.
- Device 2: GMCH2-M internal graphics device (GFX).

Note: Even though the primary PCI expansion bus is referred to as PCI0 in this document it is not PCI bus #0 from a configuration standpoint. Note that a physical PCI bus #0 does not exist. The hub interface and the internal devices in the GMCH2-M and ICH2-M logically constitute PCI Bus #0 to configuration software.

3.5.1. Logical PCI Bus #0 Configuration Mechanism

The GMCH2-M decodes the Bus Number (bits 23:16) and the Device Number fields of the CONFIG_ ADDRESS register. If the Bus Number field of CONFIG_ADDRESS is 0 the configuration cycle is targeting a PCI Bus #0 device.

Device #0: The Host-hub Bridge/DRAM Controller entity is hardwired as Device #0 on PCI Bus #0.

Device #1: The AGP interface entity is hardwired as Device #1 on PCI Bus #0.

Device #2: The internal graphics device (GFX) entity is hardwired as Device #2 on PCI Bus #0.

Configuration cycles to one of the GMCH2-M internal devices are confined to the GMCH2-M and not sent over the Hub interface. Accesses to devices #3 to #31 on PCI Bus #0 will be forwarded over the Hub interface.

3.5.2. Primary PCI (PCI0) and Downstream Configuration Mechanism

If the Bus Number in the CONFIG_ADDRESS is non-zero the GMCH2-M will generate a configuration cycle over the hub interface. The ICH2-M compares the non-zero Bus Number with the SECONDARY BUS NUMBER and SUBORDINATE BUS NUMBER registers of its P2P bridges to determine if the configuration cycle is meant for Primary PCI expansion bus (PCI0), or a downstream PCI bus.

3.5.3. Internal Graphics Device (GFX) Configuration Mechanism

From the chipset configuration perspective the internal graphics device is seen as a PCI device (device #2) on PCI Bus #0. Configuration cycles that target device #2 on PCI Bus #0 will be claimed by the internal graphics device and will not be forwarded via hub interface to the ICH2-M.

3.6. Host-Hub Interface Bridge/DRAM Controller Device Registers (Device #0)

Device #0 registers come in two categories

- Those visible in both **GFX mode** and **AGP mode**.
- Those visible only in **AGP mode**. These are always appended with the message **AGP Mode Only**.

When GMCH2-M is in internal graphics (GFX) mode most of the configuration bits needed to configure Device #0 are needed in AGP mode as well. The few exceptions are don't care situations in AGP. In AGP mode, a number of bits to control the AGP port are made visible only in AGP mode. They will read back 0s in GFX mode. The following table shows the GMCH2-M configuration space for device #0.

Table 4. GMCH2-M PCI Configuration Space (Device #0)

Address Offset	Register Symbol	Register Name	Default Value	Access
00–01h	VID	Vendor Identification	8086h	RO
02–03h	DID	Device Identification (Device 0)	1130h	RO
04–05h	PCICMD	PCI Command Register	0006h	**Read/Write**
06–07h	PCISTS	PCI Status Register	0090h	**Read/Write**, RO
08h	RID (A0)	Revision Identification for A0-step	10h	RO
08h	RID (A1)	Revision Identification for A1-step	11h	RO
09h	—	Reserved	—	—
0Ah	SUBC	Sub-Class Code	00h	RO
0Bh	BCC	Base Class Code	06h	RO
0Ch	—	Reserved	—	—
0Dh	MLT	Master Latency Timer	00h	RO
0Eh	HDR	Header Type	00h	RO
0Fh	—	Reserved	—	—
10-13h	APBASE	Aperture Base Configuration	00000008h (AGP) 00000000h (GFX)	**Read/Write**, RO
14-2Bh	—	Reserved	—	—
2C–2Dh	SVID	Subsystem Vendor Identification	0000h	**Read/Write**
2E–2Fh	SID	Subsystem Identification	0000h	**Read/Write**
30–33h	—	Reserved	—	—
34h	CAPPTR	Capabilities Pointer	88h	RO
35–4Fh	—	Reserved	—	—
50h	GMCHCFG	GMCH2-M Configuration	01ss 0s00b	**Read/Write**
51h	APCONT	Aperture Control	00h	**Read/Write**, RO
52h	DRP	DRAM Row Population	00h	**Read/Write**
53h	DRAMT	DRAM Timing Register	00h	**Read/Write**
54h	DRP2	DRAM Row Population Register 2	00h	**Read/Write**
55–57h	—	Reserved	—	—
58h	FDHC	Fixed DRAM Hole Control	00h	**Read/Write**
59-5Fh	PAM	Programmable Attributes Map	00h	**Read/Write**
60h	C3STAT	C3 control and status	00h	**Read/Write**, RO
61–6Fh	—	Reserved	—	—

Address Offset	Register Symbol	Register Name	Default Value	Access
70h	SMRAM	System Management RAM Control	00h	**Read/Write**, RO
71h	—	Reserved	—	—
72-73h	MISCC	Miscellaneous Control Register	0000h	**Read/Write**, RO
74–87h	—	Reserved	—	—
88-8Bh	CAPID	Capability Identification	F104 A009h	RO
8C–91h	—	Reserved	—	—
92–93h	BUFF_SC	Buffer Strength Control	FFFFh	**Read/Write**
94–95h	BUFF_SC2	Buffer Strength Control 2	FFFFh	**Read/Write**
96–9Fh	—	Reserved	—	—
A0-A3h	ACAPID	AGP Capability Identifier	0020 0002h	RO (AGP only)
A4-A7h	AGPSTAT	AGP Status	1F00 0207h	RO (AGP only)
A8-ABh	AGPCMD	AGP Command	0000 0000h	**Read/Write** (AGP only)
AC-AFh	—	Reserved	—	—
B0-B3h	AGPCTRL	AGP Control	0000 0000h	**Read/Write** (AGP only)
B4h	APSIZE	Aperture Size	00h	**Read/Write** (AGP only)
B5-B7h	—	Reserved	—	—
B8-BBh	ATTBASE	Aperture Translation Table Base	0000 0000h	**Read/Write** (AGP only)
BCh	AMTT	AGP Multi-Transaction Timer	00h	**Read/Write** (AGP only)
BDh	LPTT	Low Priority Transaction Timer	00h	**Read/Write** (AGP only)
BEh	MCHCFG	MCH Configuration	0000 x000b	**Read/Write**, RO
BF-CAh	—	Reserced	—	—
CBh	ERRCMD	Error Command	00h	**Read/Write** (AGP only)
CC-FFh	—	Reserved	—	—

3.6.1. VID—Vendor Identification Register (Device 0)

Address Offset: 00 - 01h
Default Value: 8086h
Attribute: Read Only
Size: 16 bits

The VID Register contains the vendor identification number. This 16-bit register combined with the Device Identification Register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Description
15:0	**Vendor Identification Number**. This is a 16-bit value assigned to Intel®. Intel® VID = 8086h.

3.6.2. DID—Device Identification Register (Device 0)

Address Offset: 02 - 03h
Default Value: 1130h
Attribute: Read Only
Size: 16 bits

This 16-bit register combined with the Vendor Identification register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Description
15:0	**Device Identification Number.** This is a 16 bit value assigned to the GMCH2-M Host-Hub Interface Bridge / DRAM Controller Device 0. 1130h = Device ID for Device 0.

3.6.3. PCICMD—PCI Command Register (Device 0)

Address Offset: 04-05h
Default: 0006h
Access: Read/Write
Size: 16 bits

The PCICMD Register enables and disables the SERR# signal.

15	10	9	8
Reserved (0)		(HW=0)	SERR En

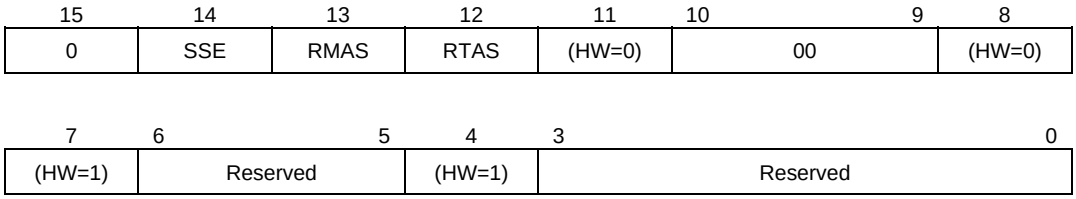
7	6	5	4	3	2	1	0
(HW=0)	(HW=0)	(HW=0)	(HW=0)	(HW=0)	(HW=1)	(HW=1)	(HW=0)

Bit	Descriptions
15:10	**Reserved**.
9	**Fast Back-to-Back.** Not implemented by GMCH2-M; hardwired to 0.
8	**SERR Enable (SERRE)**. This bit is a global enable bit for Device 0 SERR messaging. The GMCH2-M does not have an SERR# signal. The GMCH2-M communicates the SERR# condition by sending an SERR message to the ICH. If this bit is set to a 1, the GMCH2-M is enabled to generate SERR messages over the Hub interface for specific Device 0 error conditions If SERRE is reset to 0, then the SERR message is not generated by the GMCH2-M for Device 0. **NOTE: This bit only controls SERR messaging for the Device 0. Device 1 has its own SERRE bit to control error reporting for error conditions occurring on Device 1. The two control bits are used in a logical OR manner to enable the SERR hub interface message mechanism.**
7	**Address/Data Stepping.** Not implemented by GMCH2-M; hardwired to 0
6	**Parity Error Enable (PERRE).** Not implemented by GMCH2-M;hardwired to 0. Writes to this bit position have no affect.
5	**VGA Palette Snoop.** Not implemented by GMCH2-M; hardwired to 0. Writes to this bit position have no affect.
4	**Memory Write and Invalidate Enable.** Not implemented, is hardwired to 0. Writes to this bit position have no affects.
3	**Special Cycle Enable. (Not implemented by GMCH2-M; hardwired to 0).** GMCH2-M ignores all special cycles generated on the PCI.
2	**Bus Master Enable (BME)**. **(Not implemented by GMCH2-M; hardwired to 1).** GMCH2-M is always allowed to be a Bus Master. . Writes to this bit position have no affect.
1	**Memory Access Enable (MAE)**. **(Not implemented by GMCH2-M; hardwired to 1).** GMCH2-M always allows access to main memory. Writes to this bit position have no affect.
0	**I/O Access Enable (IOAE)**. **(Not implemented; hardwired to 0).** Writes to this bit position have no affect.

3.6.4. PCISTS—PCI Status Register (Device 0)

Address Offset: 06-07h
Default Value: 0090h
Access: Read Only, Read/Write Clear
Size: 16 bits

PCISTS is a 16-bit status register that reports the occurrence of a PCI master abort and PCI target abort on the PCI0 bus. PCISTS also indicates the DEVSEL# timing that has been set by the GMCH2-M hardware for target responses on the PCI0 bus. Bits [15:12] and bit 8 are Read/Write clear and bits [10:9] are read only.



Bit	Descriptions
15	**Detected Parity Error (DPE)**. This bit is hardwired to a 0. Writes to this bit position have no affect.
14	**Signaled System Error (SSE)**. This bit is set to 1 when GMCH2-M Device 0 generates an SERR message over the hub interface for any enabled Device 0 error condition. Device 0 error conditions are enabled in the PCICMD register. Device 0 error flags are read/reset from the PCISTS register. Software sets SSE to 0 by writing a 1 to this bit.
13	**Received Master Abort Status (RMAS)**. This bit is set when the GMCH2-M generates a hub interface request that receives a Master Abort completion packet. Software clears this bit by writing a 1 to it.
12	**Received Target Abort Status (RTAS)**. This bit is set when the GMCH2-M generates a hub interface request that receives a Target Abort completion packet. Software clears this bit by writing a 1 to it.
11	**Signaled Target Abort Status (STAS).** (Not implemented in GMCH2-M; is hardwired to a 0). Writes to this bit position have no affect.
10:9	**DEVSEL# Timing (DEVT)**. These bits are hardwired to 00. Writes to these bit positions have no affect. Device 0 does not physically connect to PCI0. These bits are set to 00 (fast decode) so that optimum DEVSEL timing for PCI0 is not limited by GMCH2-M.
8	**Data Parity Detected (DPD).** This bit is hardwired to a 0. Writes to this bit position have no affect.
7	**Fast Back-to-Back (FB2B).** This bit is hardwired to 1. Writes to these bit positions have no affect. Device 0 does not physically connect to PCI. This bit is set to 1 (indicating fast back-to-back capability) so that the optimum setting for PCI is not limited by GMCH2-M.
6:5	**Reserved**.
4	**Capability List (CLIST).** This bit is hardwired to '1' to indicate that GMCH2-M always has a capability list. The list of capabilities is accessed via register CAPPTR at configuration address offset 34h. Register CAPPTR contains an offset pointing to the address of the first of a linked list of capability registers. Writes to this bit position have no affect.
3:0	**Reserved**.

3.6.5. RID—Revision Identification Register (Device 0)

Address Offset: 08h

Default Value: 10h for A0-step silicon
11h for A1-step silicon
Access: Read Only
Size: 8 bits

This register contains the revision number of the Device 0. These bits are read only and writes to this register have no effect.

Bit	Description
7:0	**Revision Identification Number**. **-RO**- This is an 8-bit value that indicates the revision identification number for Device 0. This value is 10h.

3.6.6. SUBC—Sub-Class Code Register (Device 0)

Address Offset: 0Ah
Default Value: 00h
Access: Read Only
Size: 8 bits

This register contains the Sub-Class Code for the GMCH2-M Function #0. This code is 00h indicating a Host Bridge device. The register is read only.

Bit	Description
7:0	**Sub-Class Code (SUBC)**. –**RO**- This is an 8-bit value that indicates the category of Bridge into which GMCH2-M falls. The code is 00h indicating a Host Bridge.

3.6.7. BCC—Base Class Code Register (Device 0)

Address Offset: 0Bh
Default Value: 06h
Access: Read Only
Size: 8 bits

This register contains the Base Class Code of the GMCH2-M Function #0. This code is 06h indicating a Bridge device. This register is read only.

Bit	Description
7:0	**Base Class Code (BASEC)**. This is an 8-bit value that indicates the Base Class Code for GMCH2-M. This code has the value 06h, indicating a Bridge device.

3.6.8. MLT—Master Latency Timer Register (Device 0)

Address Offset: 0Dh
Default Value: 00h
Access: Read Only
Size: 8 bits

Device 0 in GMCH2-M is not a PCI master. Therefore this register is not implemented.

Bit	Descriptions
7:0	**Master Latency Timer Value.** This read only field always returns 0 when read and writes have no affect.

3.6.9. HDR—Header Type Register (Device 0)

Address Offset: 0Eh
Default: 00h
Access: Read Only
Size: 8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

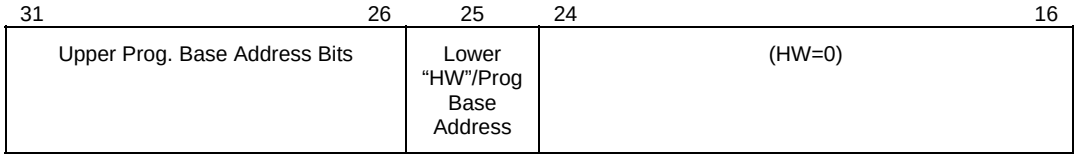
Bit	Descriptions
7:0	**Header Type.** This read only field always returns 0 when read and writes have no affect.

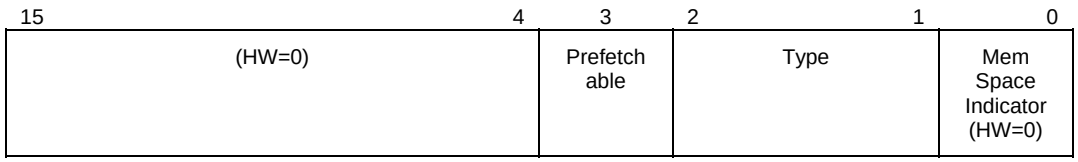
3.6.10. APBASE—Aperture Base Configuration Register (Device 0 - AGP MODE ONLY)

Address Offset:	10-13h
Default Value (AGP Mode):	00000008h
Default Value (GFX Mode):	00000000h
Access:	Read/Write, Read Only
Size:	32 bits

The APBASE is a standard PCI Base Address register that is used to set the base of the AGP Aperture. The standard PCI Configuration mechanism defines the base address configuration register such that only a fixed amount of space can be requested (dependent on which bits are hardwired to “0” or behave as hardwired to “0”). To allow for flexibility (of the aperture) an additional register called APSIZE is used as a “back-end” register to control which bits of the APBASE will behave as hardwired to “0”. This register will be programmed by the GMCH2-M specific BIOS code that will run before any of the generic configuration software is run.

Note that bit 1 of the APCONT register is used to prevent accesses to the aperture range before this register is initialized by the configuration software and the appropriate translation table structure has been established in the main memory.





Bit	Description
31:26	**Upper Programmable Base Address bits (Read/Write).** These bits are used to locate the range size selected via lower bits 25:4. Default = 0000
25	**Lower “Hardwired”/Programmable Base Address bit.** This bit behaves as a “hardwired” or as a programmable depending on the contents of the APSIZE register as defined below: Bit 25 is controlled by the bit 3 of the APSIZE register in the following manner: If APSIZE[3]=0 then APBASE[25]=0 indicating 64 MB aperture size: **Aperture Size = 64 MB → 0 (default)** If APSIZE[3]=1 then APBASE[25] = (Read/Write) allowing 32 MB aperture size: **Aperture Size = 32 MB → Read/Write** Default for APSIZE[3]=0b forces default APBASE[25] = 0b (bit responds as “hardwired” to 0). This provides a default to the maximum aperture size of 64 MB. The GMCH2-M specific BIOS is responsible for selecting smaller size (if required) before PCI configuration software runs and establishes the system address map.

Bit	Description
24:4	**Hardwired to "0".** This forces minimum aperture size selected by this register to be 32 MB.
3	**Prefetchable (RO).** This bit is hardwired to "1" to identify the Graphics Aperture range as a prefetchable, i.e.: *There are no side effects on reads, the device returns all bytes on reads regardless of the byte enables, and the GMCH2-M may merge processor writes into this range without causing errors.*
2:1	**Type (RO).** These bits determine addressing type and they are hardwired to "00" to indicate that address range defined by the upper bits of this register can be located anywhere in the 32-bit address space.
0	**Memory Space Indicator (RO).** Hardwired to "0" to identify aperture range as a memory range.

3.6.11. SVID—Subsystem Vendor Identification Register (Device 0)

Address Offset: 2C-2Dh
Default: 0000h
Access: Read/Write Once
Size: 16 bits

Bit	Description
15:0	**Subsystem Vendor ID (Read/WriteO).** This value is used to identify the vendor of the subsystem. The default value is 0000h. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read Only. This Register can only be cleared by a Reset.

3.6.12. SID—Subsystem Identification Register (Device 0)

Address Offset: 2E-2Fh
Default: 0000h
Access: Read/Write Once
Size: 16 bits

Bit	Description
15:0	**Subsystem ID (Read/WriteO).** This value is used to identify a particular subsystem. The default value is 0000h. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read Only. This Register can only be cleared by a Reset.

3.6.13. CAPPTR—Capabilities Pointer (Device 0)

Address Offset: 34h
Default Value: 88h
Access: Read Only
Size: 8 bits

The CAPPTR provides the offset that is the pointer to the location where the capability identification register is located.

Bit	Description
7:0	**Pointer to the start of the CAPPTR linked list.** The 88h value points to the CAPID register that provides capability information regarding the GMCH2-M.

3.6.14. GMCHCFG—GMCH2-M Configuration Register (Device 0)

Address Offset: 50h
Default: 01ss0s00
Access: Read/Write, Read Only
Size: 8 bits

7	6	5	4	3	2	1 0
Mem Arb Gnt Win Enable	CPU Latency Timer	Reserved	Local Memory Frequency Select	DRAM Page Closing Policy	System Memory Frequency Select	Reserved

Bit	Description
7	**Memory Arbiter Grant Window Enable (MAGWE).** This bit controls the Host vs Low Priority Graphics timeslice regulation in the arbiter for the System DRAM. **At pre-arbitration (aka, stage 1)** 0 = Disabled. Enforce fixed priority. 1 = Limit grant to host-to-graphics stream to 6 consecutive packets. **At main-arbitration (aka, stage 2)** 0 = Disabled. Enforce fixed priority. 1 = 24 clocks limiting host, 24 clocks guaranteed to low priority graphics stream. In fixed mode arbitration, MAGWE=0, the host stream always has higher priority over the low priority graphics stream for accesses to system memory. In timeslice mode, the host stream and the low priority graphics stream are both regulated by a time window to provide fairness to the graphics stream. Fixed priority mode where the host stream is always favored is the recommended mode of operation, as this setting gives highest system performance without adversely affecting graphics performance under real life applications workload.

Bit	Description
6	**CPU Latency Timer (CLT).** 0 = Deferrable processor cycle will be Deferred immediately after receiving another ADS# 1 = Deferrable processor cycle will be Deferred after it has been held in a “Snoop Stall” for 31 clocks and another ADS# has arrived (default).
5	**Reserved**
4	**Local Memory Frequency Select (LMFS).** This bit selects the operating frequency for the Local Memory Controller. Default is set by sampling LM_FREQ_SEL strap (AGP SBA[7] pin) at reset. It has a weak internal pull-up enabled during reset. 0 = 100MHz. This is a reflection of LM_FREQ_SEL strap being pulled down. 1 = 133MHz, (default). This is a reflection of LM_FREQ_SEL strap being pulled up (default). **Note: This bit has meaning only when operating in Internal graphics modes w/ display cache.** **Note: The value of this bit should only be changed when the Internal Graphics device is disabled (i.e., GMS = 00).**
3	**DRAM Page Closing Policy (DPCP).** When this bit is a 0 GMCH2-M will tend to leave the DRAM pages open. In this mode the only times that GMCH2-M will close memory pages are: 0 = Precharge Bank during service of a “Page Miss” access. Precharge All when changing from one Row to another if any Pages are open. Precharge All at leadin to a Refresh operation When this bit is a 1 GMCH2-M will tend to leave the DRAM pages closed. In this mode GMCH2-M will: 1 = Precharge All during the service of any “Page Miss” access. Precharge All when changing from one Row to another if any Pages are open. Precharge All at leadin to a Refresh operation.
2	**System Memory Frequency Select (SMFS).** This bit selects the operating frequency for the main system memory. Default is set by sampling SBS0# pin at reset. When GMCH2-M is in Graphics mode, this bit is hardwired to ‘0’ (100MHz) and read only. 0 = 100MHz. 1 = 133MHz.
1:0	**Reserved.**

3.6.15. APCONT—Aperture Control (Device 0)

Address Offset: 51h
Default Value: 00h
Access: Read/Write, Write Once, Read Only
Size: 8 bits

The Aperture Control Register controls selection and access to aperture space.

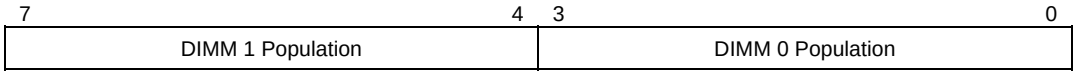
7	3	2	1	0
Reserved		AGP Select Lock	Aperture Access Global EN	AGP Select

Bit	Description
7:3	**Reserved**
2	**GFX AGP Select Lock (WO).** This GFX AGP Select (bit 0) can be made read only by this bit. This is a write once bit, after it is written to it cannot be changed without a system reset. 0 = GFX AGP Select remains writeable. 1 = GFX AGP Select is read only.
1	**Aperture Access Global Enable (Read/Write).** This bit is used to prevent access to the aperture from any port (processor, PCI0 or AGP/PCI1) before the aperture range is established by the configuration software and appropriate translation table in the main DRAM has been initialized. **Default is "0"**. It must be set after system is fully configured for aperture accesses.
0	**GFX AGP Select. Read/Write, RO if GFX AGP Select Lock (bit 2 =1)** This field selects the graphics device to be either AGP or Internal Graphics (GFX). 0 = AGP Mode. AGP interface device is enabled. All registers in device 0 and device 1 are visible. No device 2 registers are visible, reads from those addresses will return 1's. 1 = GFX Mode. Internal Graphics device is enabled. All non-AGP related device 0 registers and all device 2 registers are visible. No device 1 registers are visible, reads from those addresses will return 1's. Reads from AGP related device 0 registers will return 0's. The internal graphics device will not respond to any configuration cycles unless SMRAM[7:6] @ 70h are NOT 00 AND APCONT[0] @ is 1. **GFX AGP Select** must be programmed before any other access is made to the configuration space. The two possible modes are mutually exclusive. This bit determines whether other configuration registers are enabled or disabled.This bit must be set as part of the initialization sequence.

3.6.16. DRP—DRAM Row Population Register (Device 0)

Address Offset: 52h
Default Value: 00h
Access: Read/Write (Read_Only if D_LCK = 1)
Size: 8 bits

The DRAM Row Population Register defines the population of each side of each SO-DIMM. Note that this entire register becomes RO when the D_LCK bit (SMRAM register Device 0, address offset 70h) is set.



Bit	Description
7:4	**DIMM 1 Population.** This field indicates the population of DIMM 1. (See table below)
3:0	**DIMM 0 Population.** This field indicates the population of DIMM 0. (See table below)

Table 5. Supported System Memory DIMM Configurations

GMCH2-M Register Code	DIMM Capacity	# of Devices / DIMM	# of Sides	DRAM Technology	Front Side Population		Back Side Population		Row	Bank	Column
					Count	Config	Count	Config			
0	0			N/A	Empty		Empty		N/A	N/A	N/A
1	32 MB	16	DS	16 Mb	8 -	2 Mb x 8	8 -	2 Mb x 8	11	1	9
2	32 MB	4	SS	64 Mb	4 -	4 Mb x 16			12	2	8
3	48 MB	12	DS	64/16 Mb	4 -	4 Mb x 16	8 -	2 Mb x 8	12	2/1	8
4	64 MB	8	DS	64 Mb	4 -	4 Mb x 16	4 -	4 Mb x 16	12	2	8
5	64 MB	8	SS	64 Mb	8 -	8 Mb x 8			12	2	9
5	64 MB	4	SS	128 Mb	4 -	8 Mb x 16			12	2	9
6	96 MB	12	DS	64 Mb	8 -	8 Mb x 8	4 -	4 Mb x 16	12	2	9/8
6	96 MB	8	DS	128/64 Mb	4 -	8 Mb x 16	4 -	4 Mb x 16	12	2	9/8
7	128 MB	16	DS	64 Mb	8 -	8 Mb x 8	8 -	8 Mb x 8	12	2	9
7	128 MB	8	DS	128 Mb	4 -	8 Mb x 16	4 -	8 Mb x 16	12	2	9
9	128 MB	8	SS	128 Mb	8 -	16 Mb x 8			12	2	10
A	128 MB	4	SS	256 Mb	4 -	16 Mb x 16			13	2	9
B	192 MB	12	DS	128 Mb	8 -	16 Mb x 8	4 -	8 Mb x 16	12	2	10/9
B	192 MB	16	DS	128/64 Mb	8 -	16 Mb x 8	8 -	8 Mb x 8	12	2	10/9
C	256 MB	16	DS	128 Mb	8 -	16 Mb x 8	8 -	16 Mb x 8	12	2	10
D	256 MB	8	DS	256 Mb	4 -	16 Mb x 16	4 -	16 Mb x 16	13	2	9
E	256 MB	8	SS	256 Mb	8 -	32 Mb x 8			13	2	10
F	512 MB	16	DS	256 Mb	8 -	32 Mb x 8	8 -	32 Mb x 8	13	2	10

3.6.17. DRAMT—DRAM Timing Register (Device 0)

Address Offset: 53h
Default Value: 00h
Access: Read/Write
Size: 8 bits

This register controls the operating mode and the timing of the DRAM Controller.

7 5	4	3	2	1	0
SDRAM Mode Select	DRAM Cycle Time	Reserved	CAS# Latency	SDRAM RAS# to CAS# Dly	SDRAM RAS# Precharge

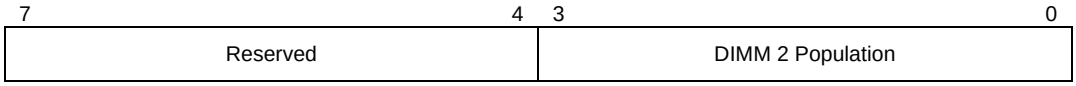
Bit	Description
7:5	**SDRAM Mode Select (SMS).** These bits select the operational mode of the GMCH2-M DRAM interface. The special modes are intended for initialization at power up. 000 = **DRAM in Self-Refresh Mode**, Refresh Disabled (Default) 001 = **Normal Operation**, 100Mhz System memory - Refresh interval 15.6 uSec 010 = **Normal Operation**, 100Mhz System memory - Refresh interval 7.8 011 = **Normal Operation**, 100Mhz System memory - Refresh interval 1.28 uSec 100 = **NOP Command Enable.** In this mode all processor cycles to SDRAM result in a NOP Command. 101 = **All Banks Precharge Enable.** In this mode all processor cycles to SDRAM result in an All Banks Precharge Command on the SDRAM interface. 110 = **Mode Register Set Enable.** In this mode all processor cycles to SDRAM result in a mode register set command on the SDRAM interface. The Command is driven on the MA[12:0] lines. MA[2:0] must always be driven to 010 for burst of 4 mode. MA3 must be driven to 1 for interleave wrap type. MA4 needs to be driven to the value programmed in the CAS# Latency bit. MA[6:5] should always be driven to 01. MA[12:7] must be driven to 00000. BIOS must calculate and drive the correct host address for each row of memory such that the correct command is driven on the MA[12:0] lines. **Note** that MAB[7:4]# are inverted from MAA[7:4]; BIOS must account for this. 111 = **CBR Enable.** In this mode all processor cycles to SDRAM result in a CBR cycle on the SDRAM interface.
4	**DRAM Cycle Time (DCT).** This bit controls the number of SCLKs for an access cycle. 0 = Tras = 5 SCLKs & Trc = 7 SCLKs (Default) 1 = Tras = 7 SCLKs & Trc = 9 SCLKs.
3	**Intel® Reserved.**
2	**CAS# Latency (CL).** This bit controls the number of CLKs between when a read command is sampled by the SDRAMs and when GMCH2-M samples read data from the SDRAMs. 0 = CAS# latency is 3 SCLKs. 1 = CAS# latency is 2 SCLKs.
1	**SDRAM RAS# to CAS# Delay (SRCD).** This bit controls the number of SCLKs from a Row Activate command to a read or write command. 0 = 3 clocks will be inserted between a row activate command and either a read or write command. 1 = 2 clocks will be inserted between a row activate and either a read or write command.

Bit	Description
0	**SDRAM RAS# Precharge (SRP).** This bit controls the number of SCLKs for RAS# precharge. 0 = 3 clocks of RAS# precharge are provided. 1 = 2 clocks of RAS# precharge are provided

3.6.18. DRP2—DRAM Row Population Register 2 (Device 0)

Address Offset: 54h
Default Value: 00h
Access: Read/Write (Read_Only if D_LCK = 1)
Size: 8 bits

This second DRAM Row Population Register (DRP2) defines the population of each side of DIMM 2.

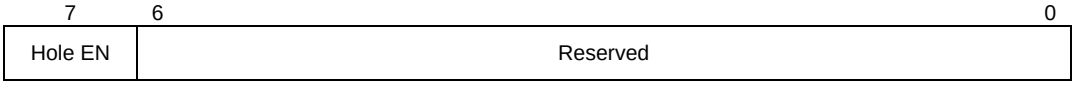


Bit	Description
7:4	**Reserved.**
3:0	**DIMM 2 Population.** This field indicates the population of DIMM 2. Please refer to Supported System Memory DIMM Configurations table located with the DRP register definition. Note that not some of the larger capacity DIMMs may not be supported in DIMM 2 based on the capacities of DIMM 0 and DIMM 1. The max supported main memory capacity is 512 MB.

3.6.19. FDHC — Fixed DRAM Hole Control Register (Device 0)

Address Offset: 58h
Default Value: 00h
Access: Read/Write
Size: 8 bits

This 8-bit register controls a single fixed DRAM hole: 15-16 MB.



Bit	Description
7	**Hole Enable (HEN).** This field enables a memory hole in DRAM space. Host cycles matching an enabled hole are passed on to ICH through the hub interface. Hub interface and PCI cycles matching an enabled hole will be ignored by the GMCH2-M. Note that a selected hole is not re-mapped. 0 = No Hole Enabled 1 = 15 MB-16 MB (1MB) Hole Enabled
6:0	**Reserved.**

3.6.20. PAM—Programmable Attributes Map Registers (Device 0)

Address Offset: 59 - 5Fh
Default Value: 00h
Attribute: Read/Write
Size: 4 bits/register

The GMCH2-M allows programmable memory attributes on 13 *Legacy* memory segments of various sizes in the 768 KB to 1 MB address range. Seven Programmable Attribute Map (PAM) Registers are used to support these features. Cacheability of these areas is controlled via the MTRR registers in the mobile Intel® Pentium® III processor. Two bits are used to specify memory attributes for each memory segment. These bits apply to both host, AGP/PCI and hub interface initiator accesses to the PAM areas. These attributes are:

- RE - Read Enable. When RE = 1, the processor read accesses to the corresponding memory segment are claimed by the GMCH2-M and directed to main memory. Conversely, when RE = 0, the host read accesses are directed to the hub interface/PCI0.
- WE - Write Enable. When WE = 1, the host write accesses to the corresponding memory segment are claimed by the GMCH2-M and directed to main memory. Conversely, when WE = 0, the host write accesses are directed to the hub interface/PCI0.

The RE and WE attributes permit a memory segment to be Read Only, Write Only, Read/Write, or disabled. For example, if a memory segment has RE = 1 and WE = 0, the segment is Read Only.

Each PAM Register controls two regions, typically 16 KB in size. Each of these regions has a 4-bit field. The four bits that control each region have the same encoding and are defined in the following table.

Table 6. Attribute Bit Assignments

7	6	5	4	3	2	1	0	Description
R	R	0	0	R	R	0	0	**Disabled.** DRAM is disabled and all accesses are directed to the hub interface. The GMCH2-M does not respond as a AGP/PCI or hub interface target for any read or write access to this area.
R	R	0	1	R	R	0	1	**Read Only**. Reads are forwarded to DRAM and writes are forwarded to the hub interface for termination. This write protects the corresponding memory segment. The GMCH2-M will respond as a AGP/PCI or hub interface target for read accesses but not for any write accesses.
R	R	1	0	R	R	1	0	**Write Only**. Writes are forwarded to DRAM and reads are forwarded to the hub interface for termination. The GMCH2-M will respond as a AGP/PCI or hub interface target for write accesses but not for any read accesses.
R	R	1	1	R	R	1	1	**Read/Write**. This is the normal operating mode of main memory. Both read and write cycles from the host are claimed by the GMCH2-M and forwarded to DRAM. The GMCH2-M will respond as a AGP/PCI or hub interface target for both read and write accesses.

As an example, consider a BIOS that is implemented on the expansion bus. During the initialization process, the BIOS can be shadowed in main memory to increase the system performance. When BIOS is shadowed in main memory, it should be copied to the same address location. To shadow the BIOS, the attributes for that address range should be set to write only. The BIOS is shadowed by first doing a read of that address. This read is forwarded to the expansion bus. The host then does a write of the same address, which is directed to main memory. After the BIOS is shadowed, the attributes for that memory area are set to read only so that all writes are forwarded to the expansion bus. The table above and the figure below show the PAM registers and the associated attribute bits:

Figure 3. PAM Registers

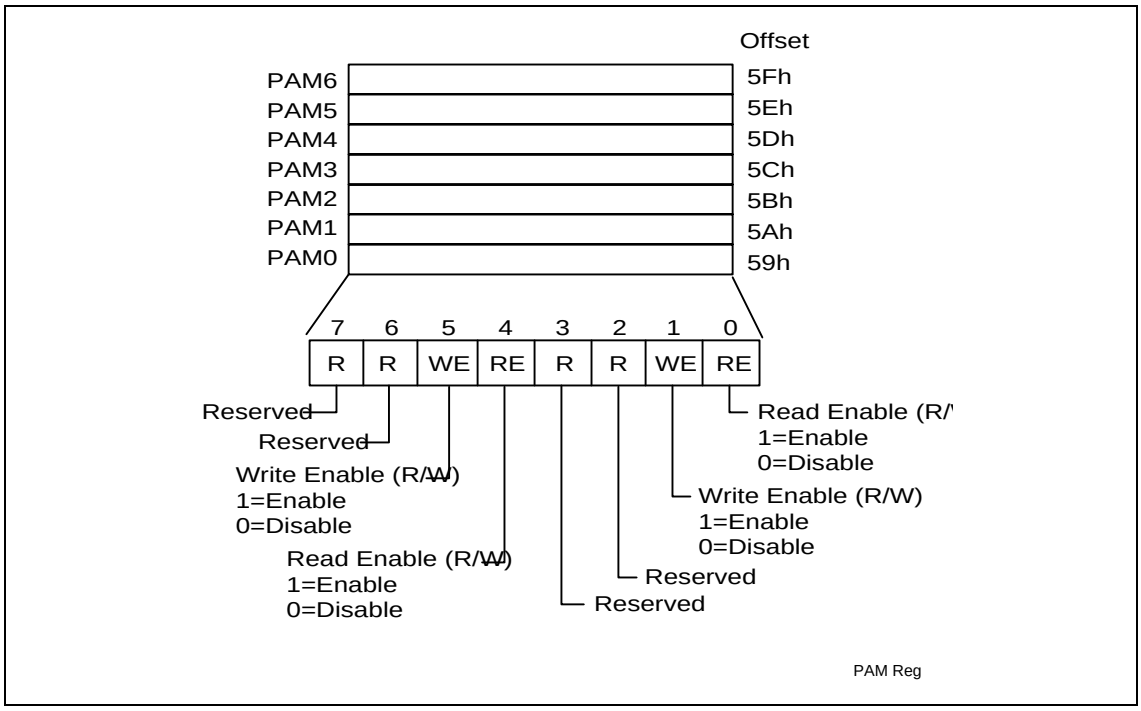


Table 7. PAM Registers and Associated Memory Segments

PAM Reg	Attribute Bits				Memory Segment	Comments	Offset
PAM0[3:0]	Reserved						59h
PAM0[7:4]	R	R	WE	RE	0F0000h - 0FFFFFh	BIOS Area	59h
PAM1[3:0]	R	R	WE	RE	0C0000h - 0C3FFFh	ISA Add-on BIOS	5Ah
PAM1[7:4]	R	R	WE	RE	0C4000h - 0C7FFFh	ISA Add-on BIOS	5Ah
PAM2[3:0]	R	R	WE	RE	0C8000h - 0CBFFFh	ISA Add-on BIOS	5Bh
PAM2[7:4]	R	R	WE	RE	0CC000h- 0CFFFFh	ISA Add-on BIOS	5Bh
PAM3[3:0]	R	R	WE	RE	0D0000h- 0D3FFFh	ISA Add-on BIOS	5Ch
PAM3[7:4]	R	R	WE	RE	0D4000h- 0D7FFFh	ISA Add-on BIOS	5Ch
PAM4[3:0]	R	R	WE	RE	0D8000h- 0DBFFFh	ISA Add-on BIOS	5Dh
PAM4[7:4]	R	R	WE	RE	0DC000h- 0DFFFFh	ISA Add-on BIOS	5Dh
PAM5[3:0]	R	R	WE	RE	0E0000h- 0E3FFFh	BIOS Extension	5Eh
PAM5[7:4]	R	R	WE	RE	0E4000h- 0E7FFFh	BIOS Extension	5Eh
PAM6[3:0]	R	R	WE	RE	0E8000h- 0EBFFFh	BIOS Extension	5Fh
PAM6[7:4]	R	R	WE	RE	0EC000h- 0EFFFFh	BIOS Extension	5Fh

Expansion Area (C0000h-DFFFFh)

This 128 KByte ISA Expansion region is divided into eight 16 KByte segments. Each segment can be assigned one of four Read/Write states: read-only, write-only, Read/Write, or disabled. Typically, these blocks are mapped through GMCH2-M and are subtractively decoded to ISA space. Memory that is disabled is not remapped.

Note: That GMCH2-M has support for more PAM regions than Intel® 810 chipset.

Extended System BIOS Area (E0000h-EFFFFh)

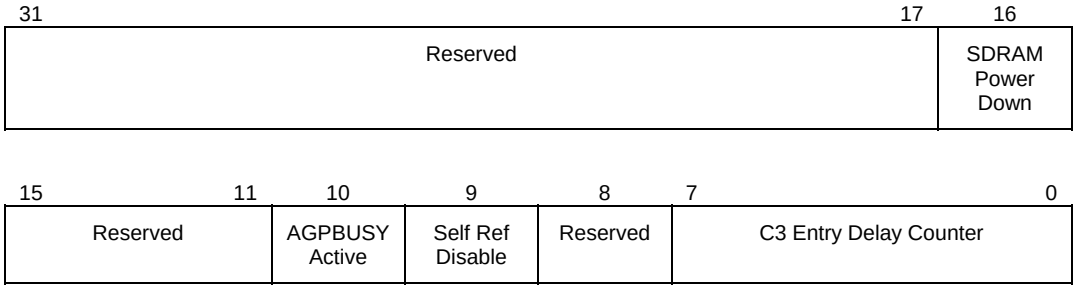
This 64 KByte area is divided into four 16 KByte segments. Each segment can be assigned independent read and write attributes so it can be mapped either to main DRAM or to the hub interface. Typically, this area is used for RAM or ROM. Memory segments that are disabled are not remapped elsewhere.

System BIOS Area (F0000h-FFFFFh)

This area is a single 64 KByte segment. This segment can be assigned read and write attributes. It is by default (after reset) Read/Write disabled and cycles are forwarded to the hub interface. By manipulating the Read/Write attributes, the GMCH2-M can "shadow" BIOS into the main DRAM. When disabled, this segment is not remapped.

3.6.21. C3STATUS —C3 Control and Status Register (Device #0)

Address Offset: 60h
Default Value: (see table)
Access: Read/Write (some bits Read Only)
Size: 32 bits



Bit	Description
31:17	Reserved
16	SDRAM Power Down Feature 0 = SDRAM allowed to enter power down via CKE# 1 = SDRAM not allowed to enter power down (Default)
15:11	Reserved
10	Force AGPBUSY# active. 0 = AGPBUSY# operates normally (Default) 1 = AGPBUSY# asserted (low) continuously.

Bit	Description
9	Self-Refresh Disable. 0 = Self-Refresh enabled during C3 state. (Default) 1 = Self-Refresh disabled.
8	Reserved: need to be programmed as '0'
7:0	C3 entry delay counter. Adjusts the delay for entering the C3 state. 40h = Optimal setting

3.6.22. SMRAM - System Management RAM Control Register (Device 0)

Address Offset: 70h
Default Value: 00h
Access: Read/Write, Read Only
Size: 8 bits

The SMRAM register controls how accesses to Compatible and Extended SMRAM spaces are treated, and how much (if any) memory is used from the System to support both SMRAM and Graphics Local Memory needs.

7 6	5 4	3 2	1	0
Graphics Mode Select	Upper SMM Select	Lower SMM Select	SMM Space Locked	E_ SMRAM_ ERR

Bit	Description
7:6	**Graphics Mode Select (GMS).** This field is used to enable/disable the Internal Graphics device (GFX) and select the amount of Main Memory that is "Stolen" to support the Internal Graphics device in VGA (non-linear) mode only. These 2 bits only have meaning if we are not in AGP mode. 00 = Internal Graphics Device Disabled, No memory "Stolen" 01 = Internal Graphics Device Enabled, No memory "Stolen" 10 = Internal Graphics Device Enabled, 512K of memory "Stolen" for frame buffer. 11 = Internal Graphics Device Enabled, 1M of memory "Stolen" for frame buffer. **Note:** When the Internal Graphics Device is Disabled (00) the Graphics Device and all of its memory and I/O functions are disabled and the clocks to this logic are turned off, memory accesses to the VGA range (A0000-BFFFF) will be forwarded on to the hub interface, and the Graphics Local Memory space is NOT "stolen" from main memory. Any change to the SMRAM register will not affect AGP mode or cause the controller to go into AGP mode. When this field is non-0 the Internal Graphics Device and all of its memory and I/O functions are enabled, all non-SMM memory accesses to the VGA range will be handled internally and the selected amount of Graphics Local Memory space (0, 512K or 1M) is "stolen" from the main memory. Graphics Memory is "stolen" AFTER TSEG Memory is "stolen". Once D_LCK is set, these bits becomes read only. GMCH2-M does not support VGA on local memory. Software must not use the 01 mode for VGA

Bit	Description
5:4	**Upper SMM Select (USMM).** This field is used to enable/disable the various SMM memory ranges above 1 MB. TSEG is a block of memory (“Stolen” from Main Memory at [TOM-Size]: [TOM]) that is only accessable by the processor and only while operating in SMM mode. HSEG is a Remap of the AB segment at FEEA0000: FEEBFFFF. Both of these areas, when enabled, are usable as SMM RAM. 00 = TSEG and HSEG are both Disabled 01 = TSEG is Disabled, HSEG is Conditionally Enabled 10 = TSEG is Enabled as 512 KB and HSEG is Conditionally Enabled 11 = TSEG is Enabled as 1 MB and HSEG is Conditionally Enabled **Note:** Non-SMM Operations (SMM processor accesses and all other access) that use these address ranges are forwarded to the hub interface. Once D_LCK is set, these bits becomes read only. HSEG is ONLY enabled if LSMM = 00.
3:2	**Lower SMM Select (LSMM).** This field controls the definition of the A&B segment SMM space 00 = AB segment Disabled (no one can write to it). 01 = AB segment Enabled as General System RAM (anyone can write to it). 10 = AB segment Enabled as SMM Code RAM Shadow. Only SMM Code Reads can access DRAM in the AB segment (processor code reads only). SMM Data operations and all Non-SMM Operations go to either the internal graphics device or are broadcast on the hub interface. 11 = AB segment Enabled as SMM RAM. All SMM operations to the AB segment are serviced by DRAM, all Non-SMM Operations go to either the internal Graphics Device or are broadcast on the hub interface (processor SMM Read/Write can access SMM space). When D_LCK is set bit 3 becomes Read Only, and bit 2 is Writable ONLY if bit 3 is a “1”. When bit 3 is set only the processor can access it.
1	**SMM Space Locked (D_LCK):** When D_LCK is set to 1 then D_LCK, GMS, USMM, and the most significant bit of LSMM become read only. D_LCK can be set to 1 via a normal configuration space write but can only be cleared by a reset. The combination of D_LCK and LSMM provide convenience with security. The BIOS can use LSMM=01 to initialize SMM space and then use D_LCK to “lock down” SMM space in the future so that no application software (or BIOS itself) can violate the integrity of SMM space, even if the program has knowledge of the LSMM function. This bit also Locks the DRP and DRP2 registers.
0	**E_SMRAM_ERR (E_SMERR):** This bit is set when processor accesses the defined memory ranges in Extended SMRAM (HSEG or TSEG) while not in SMM mode. It is software’s responsibility to clear this bit. The software must write a 1 to this bit to clear it This bit is Not set for the case of an Explicit Write Back operation.

3.6.23. MISCC—Miscellaneous Control Register (Device 0)

Address Offset: 72-73h
Default Value: 0000h
Access: Read/Write, Read Only
Size: 16 bits

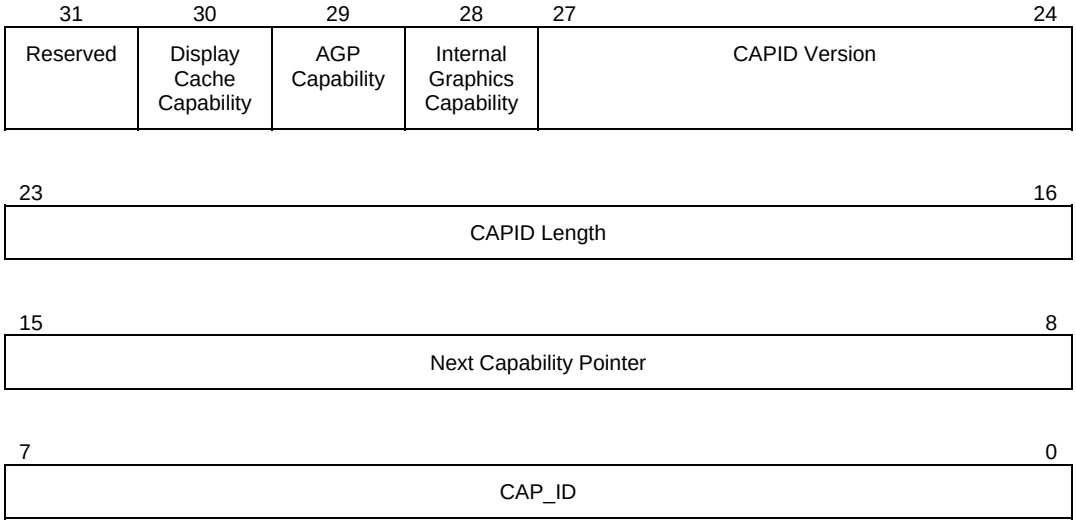
This register holds all of the miscellaneous control bits for GMCH2-M.

Bit	Description
15:8	**Reserved.**
7:6	**Read Power Throttle Control. Read/Write,RO if Throttle Lock (bit 3=1). These bits are locked (RO) when bit 3 (Throttle Lock) is set to 1.**These bits select the Power Throttle Bandwidth Limits for Read operations to System Memory. 00 = No Limit (800 MB/Sec) (Default Value) 01 = Limit at 87 ½ % (700 MB/Sec) 10 = Limit at 75 % (600 MB/Sec) 11 = Limit at 62 ½ % (500 MB/Sec)
5:4	**Write Power Throttle Control. Read/Write,RO if Throttle Lock (bit 3=1). These bits are locked (RO) when bit 3 (Throttle Lock) is set to 1.** These bits select the Power Throttle Bandwidth Limits for Write operations to System Memory. 00 = No Limit (800 MB/Sec) (Default Value) 01 = Limit at 62 ½ % (500 MB/Sec) 10 = Limit at 50 % (400 MB/Sec) 11 = Limit at 37 ½ % (300 MB/Sec)
3	**Throttle Lock**. **Read/Write, RO if Throttle Lock (bit 3 =1). Once this bit is set, it can only be cleared by a reset.** 0 = Bits [7:3] remain writeable 1 = Block writes to bits [7:3]
2	**Reserved** (RO)
1	**BNR Lookahead (Read/Write).** This enables the HT unit to look further up the data path in order to optimize the BNR (Block New Requests) signal in order to increase our effective IOQ (In Order Queue) depth. 0 = Normal Behavior (default) 1 = BNR Lookahead Enable

Bit	Description
0	**Graphics Translation Window Size Select (GTWSS).** (Read/Write) In GFX mode this would be the size of the GTT (Graphics Translation Table). Not a valid bit in AGP mode. 0 = 64 MB (default) 1 = 32 MB.

3.6.24. CAPID—Capability Identification (Device 0 - AGP MODE ONLY)

Address Offset: 88-8Bh
Default Value: 1 F205 A009h – 1 1205 0009h
Access: Read Only
Size: 64 bits (40 bits implemented)



Bit	Description
39-33	**Reserved**
32	**Mobile Capable** 0 = Not mobile capable 1= Mobile capable (bit hard wired internally)
31	**Reserved** Default = 0.
30	**Display Cache Capability (R/O)** 0 = Only supports UMA mode (no Local Memory). 1 = Component is Local Memory (Display Cache) and UMA capable.
29	**AGP Capability (R/O)** 0 = AGP mode not supported. 1 = AGP mode supported.

Bit	Description
28	**Internal Graphics Capability (R/O)** 0 = Internal graphic controller **not** supported. 1 = Internal graphic controller supported.
27-24	**CAPID Version (R/O)** This field has the value **0010b** to identify the first revision of the CAPID register definition.
23-16	**CAPID Length (R/O)** This field has the value 05h to indicate the structure length.
15-8	**Next Capability Pointer (R/O)** This field has two possible values base on (APCONT[0] at offset 51h): A0h when APCONT[0] = 0 (AGP Mode) meaning the next capability pointer is ACAPID. 00h when APCONT[0] = 1 (GFX Mode) meaning that this was the last capability pointer in the list.
7-0	**CAP_ID (R/O)** This field has the value **1001b** to identify the CAP_ID assigned by the PCI SIG for vendor dependent capability pointers.

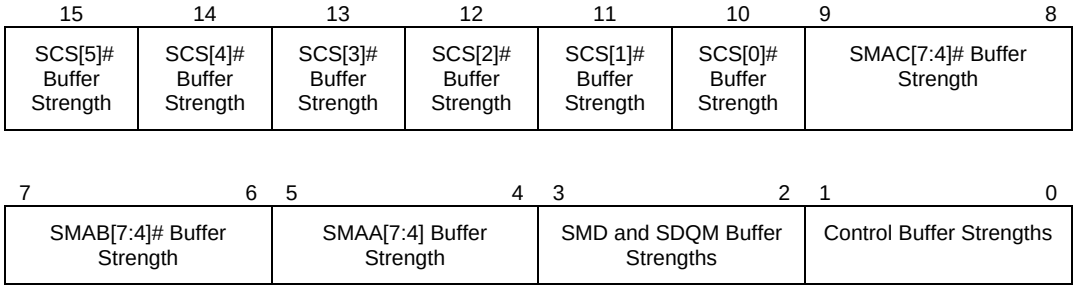
3.6.25. BUFF_SC—System Memory Buffer Strength Control Register (Device 0)

Address Offset: 92-93h
Default Value: FFFFh
Access: Read/Write
Size: 16 bits

This register programs the system memory DRAM interface signal buffer strengths, with the exception of the CKEs. The programming of these bits should be based on DRAM density (x8 or x16), DRAM technology (16Mb, 64Mb, 128Mb or 256 Mb), rows populated, etc. Note that x4 & x32 DRAMs are not supported. Registered DIMMs and DIMMS with ECC are also not supported and BIOS upon detection of ECC via SPD, should report to the user that ECC DIMM timings are not supported by the GMCH2-M. Note SO-DIMM only support x16 DRAM density.

In the descriptions below, the term “Row” is equivalent to one side of one DIMM. In other words, a “single-sided” DIMM contains one populated row (always an odd numbered), and one empty row (even numbered). A “double-sided” DIMM contains two populated rows.

All buffer strengths are based on the number of “loads” connected to each pin of a given signal group. A “load” represents one pin of one SDRAM Device. The GMCH2-M pin is implied and not counted in the load equations. The number of loads on a given signal for a given configuration can be determined entirely from the width of the SDRAM devices that populate each row in the configuration. This information is readily available for each row via the Serial Presence Detect mechanism.



Bit	Description
15	**SCS[5]# Buffer Strength (Row 5).** 0 = 1.7x 4 loads 1 = 1.0x 0 or 2 loads Each Row is actually selected by a pair of Chip Select signals (SCSA[n]# and SCSB[n]#). The number of SCS# loads for a given Row can be determined from SPD data using the following equation: Loads = 32 / (width of SDRAM devices in row)
14	**SCS[4]# Buffer Strength (Row 4).** 0 = 1.7x 4 loads 1 = 1.0x 0 or 2 loads

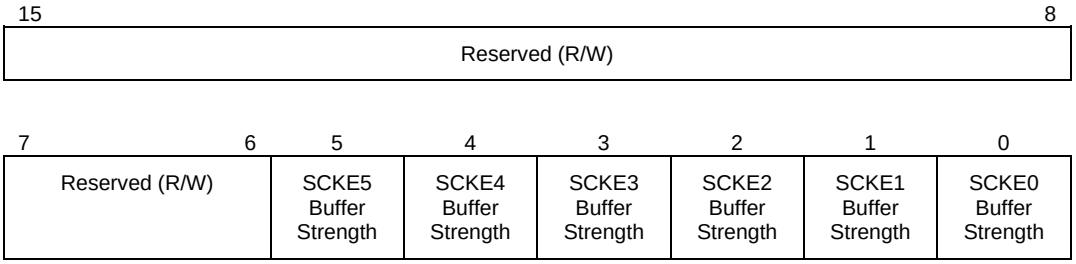
Bit	Description
13	**SCS[3]# Buffer Strength (Row 3).** 0 = 1.7x 4 loads 1 = 1.0x 0 or 2 loads
12	**SCS[2]# Buffer Strength (Row 2).** 0 = 1.7x 4 loads 1 = 1.0x 0 or 2 loads
11	**SCS[1]# Buffer Strength (Row 1).** 0 = 1.7x 4 loads 1 = 1.0x 0 or 2 loads
10	**SCS[0]# Buffer Strength (Row 0).** 0 = 1.7x 4 loads 1 = 1.0x 0 or 2 loads
9:8	**SMAC[7:4]# Buffer Strength (Rows 4/5).** 00 = 2.7x > 8 loads 01 = 1.7x 8 loads 10 = 1.0x 0 or 4 loads 11 = 1.0x 0 or 4 loads Separate copies of these SMA*[7:4] “Command-Per-Clock” signals are provided for each DIMM. So the loads for each copy are determined by the number of SDRAM devices on the corresponding DIMM (4, 8, 12, or 16 loads). The number of loads for each SMA*[7:4] signal group can be determined from SPD data using the following equation: Loads = (64 / (SDRAM Device Width for 1st row)) + (64 / (SDRAM Device Width for 2nd row))
7:6	**SMAB[7:4]# Buffer Strength (Rows 2/3).** 00 = 2.7x 16 loads 01 = 1.7x 8 loads 10 = 1.0x 0 or 4 loads 11 = 1.0x 0 or 4 loads
5:4	**SMAA[7:4] Buffer Strength (Rows 0/1).** 00 = 2.7x 16 loads 01 = 1.7x 8 loads 10 = 1.0x 0 or 4 loads 11 = 1.0x 0 or 4 loads

Bit	Description
3:2	**SMD[63:0] and SDQM[7:0] Buffer Strengths (All Rows).** 00 = 1.7x > 2 loads 01 = 0.7x Reserved 10 = 1.0x 0-2 loads 11 = 1.0x 0-2 loads The load on the SMD and SDQM signals is a function only of the number of populated rows in the system (range 1 to 6 loads): Loads = Number of populated Rows.
1:0	**SWE#, SCAS#, SRAS#, SMAA[11:8, 3:0], SBS[1:0] Control Buffer Strengths (All Rows)** 00 = 1.7x > 16 loads 01 = 0.7x < 8 loads 10 = 1.0x 8-16 loads 11 = 1.0x 8-16 loads The load on the Address and Control signals (other than SMA*[7:4] above) is simply the number of devices populated in ALL rows (range from 4 to 48 loads!). Loads = (64 / Row 0 Device Width) + (64 / Row 1 Device Width) + (64 / Row 2 Device Width) + (64 / Row 3 Device Width) + (64 / Row 4 Device Width) + (64 / Row 5 Device Width)

3.6.26. BUFF_SC2-System Memory Buffer Strength Control Register 2 (Device 0)

Address Offset: 94-95h
Default Value: FFFFh
Access: Read/Write
Size: 16 bits

This register programs the system memory DRAM interface CKE signal buffer strengths. See BUFF_SC register for remainder of buffer strength controls.



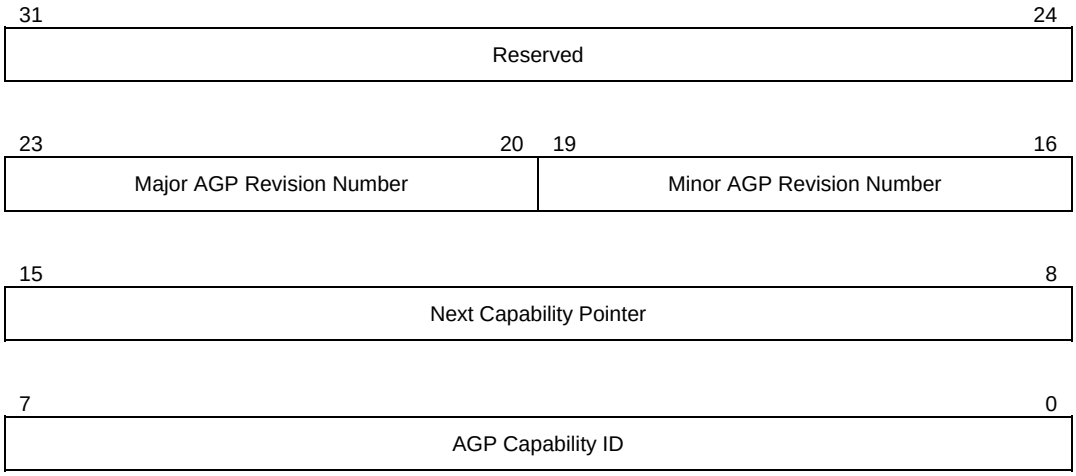
Bit	Description
15:6	**Reserved**. Generic Read/Write bits with flops for future use.
5	**SCKE[5] Buffer Strength (Row 5).** 0 = 2.7x 8 loads 1 = 1.7x 0 or 4 loads The load on a given SCKE signal is equal to the number of SDRAM devices for that particular Row (either 4 or 8 loads). Loads = (64 / SDRAM Device Width for this row)
4	**SCKE[4] Buffer Strength (Row 4).** 0 = 2.7x 8 loads 1 = 1.7x 0 or 4 loads
3	**SCKE[3] Buffer Strength (Row 3).** 0 = 2.7x 8 loads 1 = 1.7x 0 or 4 loads
2	**SCKE[2] Buffer Strength (Row 2).** 0 = 2.7x 8 loads 1 = 1.7x 0 or 4 loads
1	**SCKE[1] Buffer Strength (Row 1).** 0 = 2.7x 8 loads 1 = 1.7x 0 or 4 loads

Bit	Description
0	**SCKE[0] Buffer Strength (Row 0).** 0 = 2.7x 8 loads 1 = 1.7x 0 or 4 loads

3.6.27. ACAPID—AGP Capability Identifier Register (Device 0)

Address Offset: A0-A3h
Default Value: 00200002h
Access: Read Only
Size: 32 bits

This register provides standard identifier for AGP capability. **(AGP MODE ONLY)**

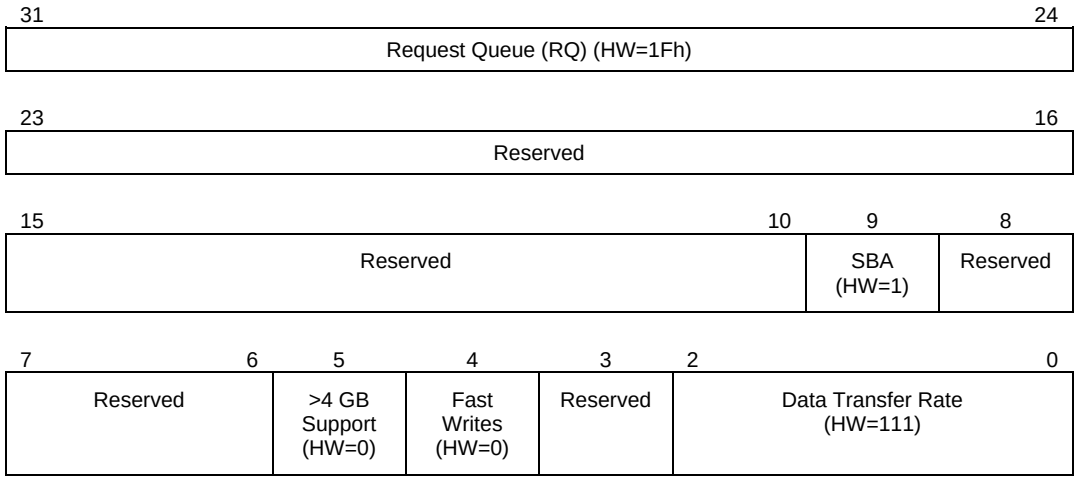


Bit	Description
31:24	**Reserved**
23:20	**Major AGP Revision Number**: These bits provide a major revision number of AGP specification to which this version of GMCH2-M conforms. These bits are set to the value 0010b to indicate AGP Rev. 2.x.
19:16	**Minor AGP Revision Number**: These bits provide a minor revision number of AGP specification to which this version of GMCH2-M conforms. This number is hardwired to value of “0000” (i.e. implying Rev x.0) *Together with major revision number this field identifies GMCH2-M as an AGP REV 2.0 compliant device.*
15:8	**Next Capability Pointer**: AGP capability is the first and the last capability described via the capability pointer mechanism and therefore these bits are hardwired to “0” to indicate the end of the capability linked list.
7:0	**AGP Capability ID**: This field identifies the linked list item as containing AGP registers. This field has the value 0000_0010b as assigned by the PCI SIG.

3.6.28. AGPSTAT—AGP Status Register (Device 0)

Address Offset: A4-A7h
Default Value: 1F000207h
Access: Read Only
Size: 32 bits

This register reports AGP device capability/status. **(AGP MODE ONLY)**

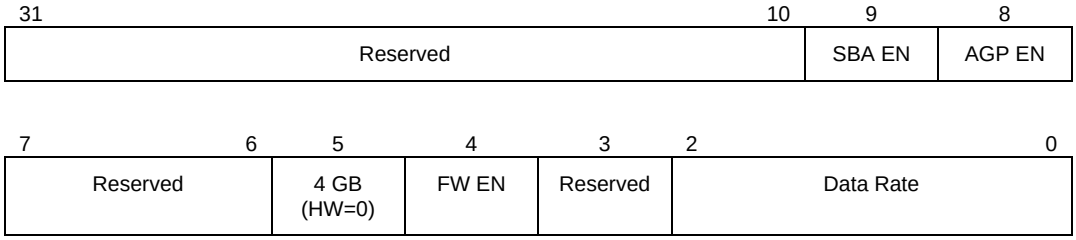


Bit	Description
31:24	**RQ.** This field contains the maximum number of AGP command requests the GMCH2-M is configured to manage. The lower 6 bits of this field reflect the value programmed in AGPCTRL[12:10]. Only discrete values of 32, 16, 8, 4 , 2 and 1 can be selected via AGPCTRL. Upper bits are hardwired to “0”. Default =1Fh to allow a maximum of 32 outstanding AGP command requests.
23:10	**Reserved**
9	**SBA.** This bit indicates that the GMCH2-M supports side band addressing. It is hardwired to 1.
8:6	**Reserved**
5	**4G.** This bit indicate that the GMCH2-M does **not** support addresses greater than 4 gigabytes. It is hardwired to 0.
4	**FW.**This bit indicate that the GMCH2-M does **not** support fast writes from the processor-to-AGP master. It is hardwired to 0.
3	**Reserved**
2:0	**Rat**e. After reset the GMCH2-M reports its data transfer rate capability. **Default Value = 111.** **Note that the selected data transfer mode applies to both AD bus and SBA bus.** Bit 0 (high) = AGP device supports 1x data transfer mode Bit 1 (high) = AGP device supports 2x data transfer mode Bit 2 (high) = AGP device supports 4x data transfer mode. This bit can be masked by the AGPCTRL register bit 0 (See PCI Configuration Space Table 3-1).

3.6.29. AGPCMD—AGP Command Register (Device 0)

Address Offset: A8-ABh
Default Value: 00000000h
Access: Read/Write
Size: 32 bits

This register provides control of the AGP operational parameters. (AGP mode only.)

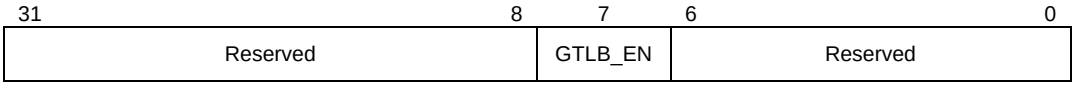


Bit	Description
31:10	**Reserved.**
9	**SBA Enable.** 1 = Side Band Addressing mechanism is enabled. 0= Side Band Addressing mechanism is disabled
8	**AGP Enable.** Any AGP operations received while this bit is set to 1 will be serviced even if this bit is reset to 0. If this bit transitions from a 1 to a 0 on a clock edge in the middle of an SBA command being delivered in 1X mode the command will be issued. 0 = GMCH2-M will ignore all AGP operations, including the sync cycle. 1 = GMCH2-M will respond to AGP operations delivered via PIPE#, or to operations delivered via SBA if the *AGP Side Band Enable* bit is also set to 1.
7:6	**Reserved.**
5	**4G.** The GMCH2-M as an AGP target does not support addressing greater than 4 gigabytes. This bit is hardwired to 0.
4	**FW Enable.** This bit must always be programmed to '0'. The chip-set will behave unpredictably if this bit is programmed with '1'.
3	**Reserved.**
2:0	**Data Rate:** The settings of these bits determines the AGP data transfer rate. One (*and only one*) bit in this field must be set to indicate the desired data transfer rate. The same bit must be set on both master and target. Bit 0: 1X, Bit 1: 2X, Bit 2: 4x. Configuration software will update this field by setting only one bit that corresponds to the capability of AGP master (after that capability has been verified by accessing the same functional register within the AGP master's configuration space.) Bit 2 becomes reserved (but will still read 4x, erroneously) when the 4x Override bit in the AGPCTRL register is set to 1 because this bit will not be updated in 4x Override mode. When the 4x Override bit is set writes to Data Rate[2] have no functional impact. **Note: This field applies to AD and SBA buses.**

3.6.30. AGPCTRL—AGP Control Register (Device 0)

Address Offset: B0-B3h
Default Value: 00000000h
Access: Read/Write
Size: 32 bits

This register provides for additional control of the AGP interface. (AGP mode only.)

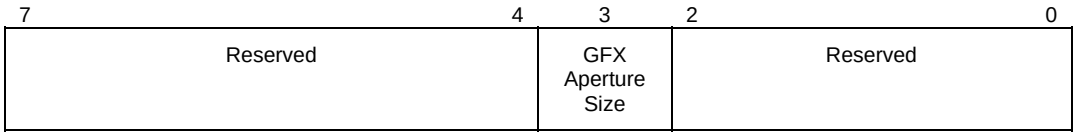


Bit	Description
31:8	**Reserved**
7	**GTLB Enable (and GTLB Flush Control) (Read/Write):** 1 = enables normal operations of the Graphics Translation Lookaside Buffer. 0 = the GTLB is flushed by clearing the valid bits associated with each entry. In this mode of operation all accesses that require translation bypass the GTLB. All requests that are positively decoded to the graphics aperture force the GMCH2-M to access the translation table in main memory before completing the request. Translation table entry fetches will not be cached in the GTLB. **(default)** When an invalid translation table entry is read, this entry will still be cached in the GTLB (ejecting the least recently used entry). The GMCH2-M will flush the GWB whenever software sets or clears this bit to ensure coherency between the GTLB and main memory. **NOTE:** This bit can be changed dynamically (i.e. while an access to GTLB occurs).
6:0	**Reserved**

3.6.31. APSIZE—Aperture Size (Device 0)

Address Offset: B4h
Default Value: 00h
Access: Read/Write
Size: 8 bits

This register determines the effective size of the Graphics Aperture used for a particular GMCH2-M configuration. This register can be updated by the GMCH2-M-specific BIOS configuration sequence before the PCI standard bus enumeration sequence takes place. If the register is not updated then a default value will select an aperture of maximum size (i.e. 64 MB). (AGP mode only.)



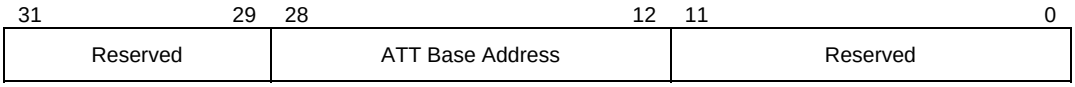
Bit	Description
7:4	**Reserved.**
3	**Graphics Aperture Size.** Bit 3 operates on bit 25 of the Aperture Base (APBASE) configuration register. When this bit is a “0” it forces bit 25 in APBASE to behave as “hardwired” to 0. When this bit is a “1” it forces bit 25 in APBASE to be Read/Write accessible. Only the following combinations are allowed: 0 = 64 MB Aperture Size 1 = 32 MB Aperture Size Default for APSIZE[3]=0b forces default APBASE[25] =0b (responds as “hardwired” to 0). This provides maximum aperture size of 64 MB. Programming APSIZE[3]=1b enables APBASE[25] as Read/Write programmable.
2:0	Reserved.

3.6.32. ATTBASE-Aperture Translation Table Base Register (Device 0)

Address Offset: B8-BBh
Default Value: 00000000h
Access: Read/Write
Size: 32 bits

This register provides the starting address of the Graphics Aperture Translation Table Base located in the main DRAM. This value is used by the GMCH2-M's Graphics Aperture address translation logic (including the GTLB logic) to obtain the appropriate address translation entry required during the translation of the aperture address into a corresponding physical DRAM address. The ATTBASE register may be dynamically changed. (AGP mode only.)

Note: The address provided via ATTBASE is 4KB aligned.



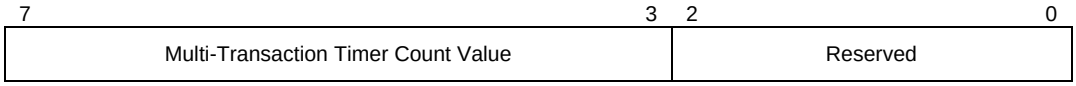
Bit	Description
31:29	**Reserved.**
28:12	**ATT Base Address**. This field contains a pointer to the base of the translation table used to map memory space addresses in the aperture range to addresses in main memory.
11:0	**Reserved.**

3.6.33. AMTT—AGP Multi-Transaction Timer (Device 0)

Address Offset: BCh
Default Value: 00h
Access: Read/Write
Size: 8 bits

AMTT is an 8-bit register that controls the amount of time that the GMCH2-M's arbiter allows AGP/PCI master to perform multiple back-to-back transactions. The GMCH2-M's AMTT mechanism is used to optimize the performance of the AGP master (using PCI semantics) that performs multiple back-to-back transactions to fragmented memory ranges (and as a consequence it can not use long burst transfers). The AMTT mechanism applies to the processor-AGP/PCI transactions as well and it guarantees to the processor a fair share of the AGP/PCI interface bandwidth.

The number of clocks programmed in the AMTT represents the guaranteed time slice (measured in 66MHz clocks) allotted to the current agent (either AGP/PCI master or Host bridge) after which the AGP arbiter will grant the bus to another agent. The default value of AMTT is 00h and disables this function. The AMTT value can be programmed with 8 clock granularity. For example, if the AMTT is programmed to 18h, then the selected value corresponds to the time period of 24 AGP (66-MHz) clocks. (AGP mode only.)

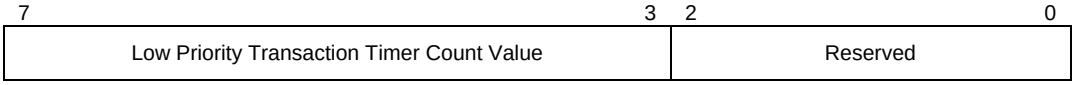


Bit	Description
7:3	**Multi-Transaction Timer Count Value.** The number programmed in these bits represents the guaranteed time slice (measured in eight 66MHz clock granularity) allotted to the current agent (either AGP/PCI master or Host bridge) after which the AGP arbiter will grant the bus to another agent.
2:0	**Reserved.**

3.6.34. LPTT—AGP Low Priority Transaction Timer Register (Device 0)

Address Offset: BDh
Default Value: 00h
Access: Read/Write
Size: 8 bits

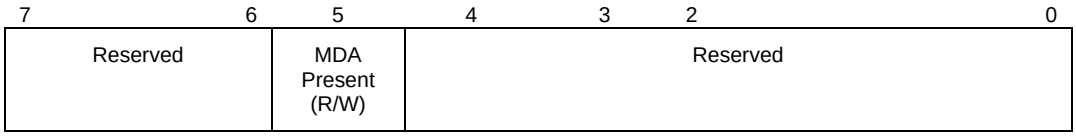
LPTT is an 8-bit register similar in a function to AMTT. This register is used to control the minimum tenure on the AGP for low priority data transaction (both reads and writes) issued using PIPE# or SB mechanisms. The number of clocks programmed in the LPTT represents the guaranteed time slice (measured in 66MHz clocks) allotted to the current low priority AGP transaction data transfer state. This does not necessarily apply to a single transaction but it can span over multiple low-priority transactions of the same type. After this time expires the AGP arbiter may grant the bus to another agent if there is a pending request. The LPTT does not apply in the case of high-priority request where ownership is transferred directly to high-priority requesting queue. The default value of LPTT is 00h and disables this function. The LPTT value can be programmed with 8 clock granularity. For example, if the LPTT is programmed to 10h, then the selected value corresponds to the time period of 16 AGP (66-MHz) clocks. (AGP mode only.)



Bit	Description
7:3	**Low Priority Transaction Timer Count Value.** The number of clocks programmed in these bits represents the guaranteed time slice (measured in eight 66MHz clock granularity) allotted to the current low priority AGP transaction data transfer state.
2:0	**Reserved.**

3.6.35. GMCHCFG—GMCH2-M Configuration Register (Device 0)

Address Offset: BEh
Default: 0000 X000b
Access: Read/Write, Read Only
Size: 8 bits



Bit	Description
7:6	**Reserved.**
5	**MDA Present (MDAP) (Read/Write). This bit should not be set when the VGA Enable bit is not set**. This bit works with the VGA Enable bit in the BCTRL register (3Eh, bit 3) of device 1 to control the routing of processor initiated transactions targeting MDA compatible I/O and memory address ranges. If the VGA enable bit is set, then accesses to IO address range x3BCh - x3BFh are forwarded to hub interface. If the VGA enable bit is not set then accesses to IO address range x3BCh - x3BFh are treated just like any other IO accesses **i.e.** the cycles are forwarded to AGP if the address is within IOBASE and IOLIMIT and ISA enable bit is not set. MDA resources are defined as the following: **Memory:** 0B0000h - 0B7FFFh **I/O:** 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh, (including ISA address aliases, A[15:10] are not used in decode). Any I/O reference that includes the I/O locations listed above, or their aliases, will be forwarded to hub interface even if the reference includes I/O locations not listed above. The following table shows the behavior for all combinations of MDA and VGA: **VGA MDA Behavior** 0 0 All References to MDA and VGA go to hub interface 0 1 Illegal Combination (DO NOT USE) 1 0 All References to VGA go to AGP/PCI. MDA-only references 1 1 VGA References go to AGP/PCI; MDA References go to hub interface
4:0	**Reserved.**

3.6.36. ERRCMD—Error Command Register (Device 0)

Address Offset: CBh
Default Value: 00h
Access: Read/Write
Size: 8 bits

This register enables various errors to generate a SERR hub interface special cycle. Since the GMCH2-M does not have an SERR# signal, SERR messages are passed from the GMCH2-M to the ICH2-M over hub interface. The actual generation of the SERR message is globally enabled for Device 0 via the PCI Command register. (AGP mode only.)

Note: An error can generate one and only one hub interface error special cycle. It is software's responsibility to make sure that when an SERR error message is enabled for an error condition, SMI and SCI error messages are disabled for that same error condition.

7 6	5	4	3	2	1	0
Reserved	SRMMRO	SRTA	SLNDM	SAAOGA	SIAA	SAIGATTE

Bit	Description
7:6	**Reserved.**
5	**SERR on Receiving Main Memory Refresh Overrun.** Identical functionality in Device 2 memory mapped space @ 020B8h. This bit allows use of this same functionality in AGP Mode. 0 = reporting of this condition is disabled. 1 = the GMCH2-M generates an SERR hub interface special cycle when a main memory refresh overrun occurs.
4	**SERR on Receiving Target Abort on the hub interface.** 0 = reporting of this condition is disabled. 1 = the GMCH2-M generates an SERR hub interface special cycle when an GMCH2-M originated hub interface cycle is terminated with a Target Abort.
3	**SERR on LOCK to non-DRAM Memory.** 0 = reporting of this condition is disabled. 1= the GMCH2-M generates an SERR hub interface special cycle when a processor initiated LOCK transaction targeting non-DRAM memory space occurs.
2	**SERR on AGP Access Outside of Graphics Aperture.** 0 = reporting of this condition is disabled. 1 = the GMCH2-M generates an SERR hub interface special cycle when an AGP access occurs to an address outside of the graphics aperture.
1	**SERR on Invalid AGP Access.** 0 = reporting of this condition is disabled. 1 = GMCH2-M generates an SERR hub interface special cycle when an AGP access occurs to an address outside of the graphics aperture and either to the 640k - 1M range or above the top of memory.

Bit	Description
0	**SERR on Access to Invalid Graphics Aperture Translation Table Entry.** 0 = reporting of this condition via SERR messaging is disabled.When this bit is set to “ 1 = the GMCH2-M generates an SERR hub interface special cycle when an invalid translation table entry was returned in response to a AGP access to the graphics aperture.

3.7. AGP/PCI Bridge Registers – (Device #1 - Visible in AGP Mode Only)

These registers are accessible through the configuration mechanism defined in an earlier section of this document.

Table 8. GMCH2-M Configuration Space (Device #1)

Address Offset	Register Symbol	Register Name	Default Value	Access Type
00-01h	VID1	Vendor Identification	8086h	RO
02-03h	DID1	Device Identification	1131h	RO
04-05h	PCICMD1	PCI Command Register	0000h	RO, Read/Write
06-07h	PCISTS1	PCI Status Register	0020h	RO, Read/WriteC
08h	RID1 (A0)	Revision Identification for A0-step	10h	RO
08h	RID1 (A1)	Revision Identification for A1-step	11h	RO
09	—	Reserved	00h	—
0Ah	SUBC1	Sub-Class Code	04h	RO
0Bh	BCC1	Base Class Code	06h	RO
0Ch	—	Reserved	00h	—
0Dh	MLT1	Master Latency Timer	00h	Read/Write
0Eh	HDR1	Header Type	01h	RO
0F-17h	—	Reserved	00h	—
18h	PBUSN	Primary Bus Number	00h	RO
19h	SBUSN	Secondary Bus Number	00h	Read/Write
1Ah	SUBUSN	Subordinate Bus Number	00h	Read/Write
1Bh	SMLT	Secondary Bus Master Latency Timer	00h	Read/Write
1Ch	IOBASE	I/O Base Address Register	F0h	Read/Write
1Dh	IOLIMIT	I/O Limit Address Register	00h	Read/Write
1E-1Fh	SSTS	Secondary Status Register	02A0h	RO, Read/WriteC
20-21h	MBASE	Memory Base Address Register	FFF0h	Read/Write
22-23h	MLIMIT	Memory Limit Address Register	0000h	Read/Write

Address Offset	Register Symbol	Register Name	Default Value	Access Type
24-25h	PMBASE	Prefetchable Memory Base Address	FFF0h	Read/Write
26-27h	PMLIMIT	Prefetchable Memory Limit Address	0000h	Read/Write
28-3Dh	—	Reserved	00h	—
3Eh	BCTRL	Bridge Control Register	00h	Read/Write
3Fh	—	Reserved	00h	—
40h	ERRCMD1	Error Command	00h	Read/Write
41-FFh	—	Reserved	00h	—

3.7.1. VID1—Vendor Identification Register (Device 1)

Address Offset: 00 - 01h
Default Value: 8086h
Attribute: Read Only
Size: 16 bits

The VID Register contains the vendor identification number. This 16-bit register combined with the Device Identification Register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Description
15:0	**Vendor Identification Number**. This is a 16-bit value assigned to Intel®. Intel® VID = 8086h.

3.7.2. DID1—Device Identification Register (Device 1)

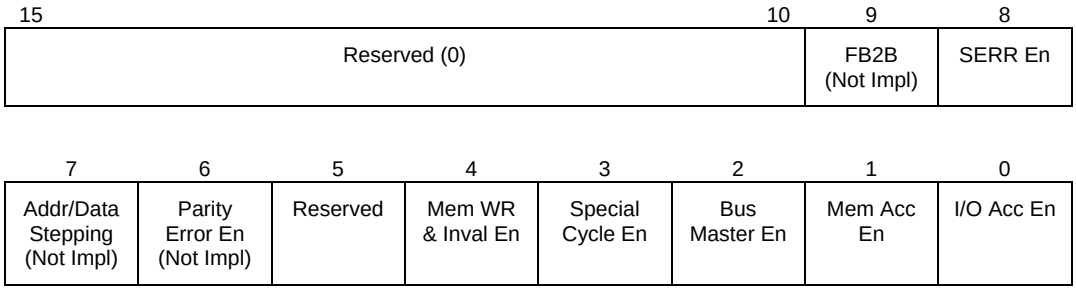
Address Offset: 02 - 03h
Default Value: 1131h
Attribute: Read Only
Size: 16 bits

This 16-bit register combined with the Vendor Identification register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Description
15:0	**Device Identification Number**. This is a 16 bit value assigned to the GMCH2-M AGP interface device. 1131h = Device ID for Device 1.

3.7.3. PCICMD1—PCI-PCI Command Register (Device 1)

Address Offset: 04-05h
Default: 0000h
Access: Read/Write, Read Only
Size 16 bits



Bit	Descriptions
15:10	**Reserved**.
9	**Fast Back-to-Back: Not Applicable-hardwired to "0".**
8	**SERR Message Enable (SERRE1)**. This bit is a global enable bit for Device 1 SERR messaging. The GMCH2-M does not have an SERR# signal. The GMCH2-M communicates the SERR# condition by sending an SERR message to the ICH2-M. 0 = the SERR message is not generated by the GMCH2-M for Device 1 1 = the GMCH2-M is enabled to generate SERR messages over hub interface for specific Device 1 error conditions that are individually enabled in the ERRCMD1 and BCTRL registers. The error status is reported in the PCISTS1 register. **NOTE: This bit only controls SERR messaging for the Device 1. Device 0 has its own SERRE bit to control error reporting for error conditions occurring on Device 0. The two control bits are used in a logical OR manner to enable the SERR hub interface message mechanism.**
7	**Address/Data Stepping: Not applicable. Hardwired to "0".**
6	**Parity Error Enable (PERRE1):** PERR# is not supported on AGP/PCI1. **Hardwired to "0".**
5	**Reserved.**
4	**Memory Write and Invalidate Enable: (RO)** This bit is implemented as RO and returns a value of "0" when read.
3	**Special Cycle Enable: (RO)** This bit is implemented as Read Only and returns a value of "0" when read.
2	**Bus Master Enable (BME1): (Read/Write)** 0 =(default) AGP Master initiated FRAME# cycles will be ignored by the GMCH2-M resulting in a Master Abort. Ignoring incoming cycles on the secondary side of the P2P bridge effectively disables the bus master on the primary side. 1 = AGP Master initiated FRAME# cycles will be accepted by the GMCH2-M if they hit a valid address decode range. This bit has no affect on AGP Master originated SBA or PIPE# cycles.

Bit	Descriptions
1	**Memory Access Enable (MAE1): (Read/Write)** 0 = all of Device #1's memory space is disabled. 1 = to enable the Memory and Prefetchable memory address ranges defined in the MBASE, MLIMIT, PMBASE, and PMLIMIT registers, as well as the VGA window.
0	**I/O Access Enable (IOAE1): (Read/Write)** 0 = all of Device 1's I/O space is disabled. 1 = to enable the I/O address range defined in the IOBASE, and IOLIMIT registers.

3.7.4. PCISTS1—PCI-PCI Status Register (Device 1)

Address Offset: 06-07h
Default Value: 0020h
Access: Read Only, Read/Write Clear
Size: 16 bits

PCISTS1 is a 16-bit status register that reports the occurrence of error conditions associated with primary side of the "virtual" PCI-PCI bridge embedded within the GMCH2-M. Since this device does not physically reside on PCI0 it reports the optimum operating conditions so that it does not restrict the capability of PCI0.

15	14	13	12	11	10 9	8
Detected Par Error (HW=0)	Sig Sys Error	Rec Mast Abort Sta (HW=0)	Rec Target Abort Sta (HW=0)	Sig Target Abort Sta (HW=0)	DEVSEL# Timing (HW=00)	Data Par Detected (HW=0)

7	6	5	4 3	0
FB2B (HW=0)	Reserved	66/60 MHz Cap (HW=0)	Reserved	

Bit	Descriptions
15	**Detected Parity Error (DPE1): Not Applicable - hardwired to "0".**
14	**Signaled System Error (SSE1).** This bit is set to 1 when Device 1 generates an SERR message over hub interface for any enabled Device 1 error condition. Device 1 error conditions are enabled in the PCICMD1, ERRCMD1 and BCTRL registers. Device 1 error flags are read/reset from the SSTS register. Software clears this bit by writing a 1 to it.
13	**Received Master Abort Status (RMAS1): Not Applicable – hardwired to "0".**
12	**Received Target Abort Status (RTAS1): Not Applicable – hardwired to "0".**
11	**Signaled Target Abort Status (STAS1): Not Applicable – hardwired to "0".**
10:9	**DEVSEL# Timing (DEVT1): Not Applicable - hardwired to "00b".**
8	**Data Parity Detected (DPD1): Not Applicable - hardwired to "0".**
7	**Fast Back-to-Back (FB2B1): Not Applicable - hardwired to "0".**

Bit	Descriptions
6	**Reserved**.
5	**66/60MHz Capability: Not Applicable - Hardwired to "1".**
4:0	**Reserved**.

3.7.5. RID1—Revision Identification Register (Device 1)

Address Offset: 08h
Default Value: 10h for A0-step silicon
11h for A1-step silicon
Access: Read Only
Size: 8 bits

This register contains the revision number of the GMCH2-M Device 1. These bits are read only and writes to this register have no effect. For the A-0 Stepping, this value is 10h.

Bit	Description
7:0	**Revision Identification Number**. This is an 8-bit value that indicates the revision identification number for the GMCH2-M Device 1. Default = 10h

3.7.6. SUBC1—Sub-Class Code Register (Device 1)

Address Offset: 0Ah
Default Value: 04h
Access: Read Only
Size: 8 bits

This register contains the Sub-Class Code for the GMCH2-M Device 1. This code is 04h indicating a PCI-PCI Bridge device. The register is read only.

Bit	Description
7:0	**Sub-Class Code (SUBC1)**. This is an 8-bit value that indicates the category of Bridge into which the GMCH2-M falls. The code is 04h indicating a Host Bridge.

3.7.7. BCC1—Base Class Code Register (Device 1)

Address Offset: 0Bh
Default Value: 06h
Access: Read Only
Size: 8 bits

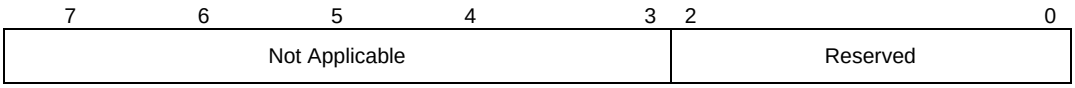
This register contains the Base Class Code of the GMCH2-M Device 1. This code is 06h indicating a Bridge device. This register is read only.

Bit	Description
7:0	**Base Class Code (BASEC)**. This is an 8-bit value that indicates the Base Class Code for the GMCH2-M Device 1. This code has the value 06h, indicating a Bridge device.

3.7.8. MLT1—Master Latency Timer Register (Device 1)

Address Offset: 0Dh
Default Value: 00h
Access: Read/Write
Size: 8 bits

This functionality is not applicable. It is described here since these bits should be implemented as a Read/Write to prevent standard PCI-PCI bridge configuration software from getting “confused”.



Bit	Description
7:3	**Not applicable but support Read/Write operations.** (Reads return previously written data.)
2:0	**Reserved.**

3.7.9. HDR1—Header Type Register (Device 1)

Address Offset: 0Eh
Default: 01h
Access: Read Only
Size: 8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

Bit	Descriptions
7:0	This read only field always returns 01h when read. Writes have no effect.

3.7.10. PBUSN—Primary Bus Number Register (Device 1)

Address Offset: 18h
Default: 00h
Access: Read Only
Size: 8 bits

This register identifies that “virtual” PCI-PCI bridge is connected to bus #0.

Bit	Descriptions
7:0	**Bus Number. Hardwired to “0”.**

3.7.11. SBUSN—Secondary Bus Number Register (Device 1)

Address Offset: 19h
Default: 00h
Access: Read/Write
Size: 8 bits

This register identifies the bus number assigned to the second bus side of the “virtual” PCI-PCI bridge i.e. to PCI1/AGP. This number is programmed by the PCI configuration software to allow mapping of configuration cycles to PCI1/AGP.

Bit	Descriptions
7:0	**Bus Number.** Programmable

3.7.12. SUBUSN—Subordinate Bus Number Register (Device 1)

Address Offset: 1Ah
Default: 00h
Access: Read/Write
Size: 8 bits

This register identifies the subordinate bus (if any) that resides at the level below PCI1/AGP. This number is programmed by the PCI configuration software to allow mapping of configuration cycles to PCI1/AGP.

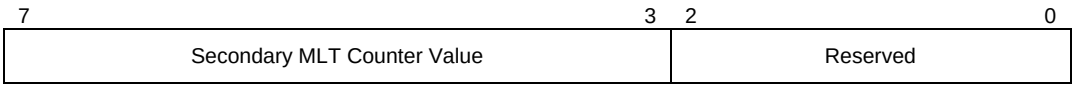
Bit	Descriptions
7:0	**Bus Number.** Programmable

3.7.13. SMLT—Secondary Master Latency Timer Register (Device 1)

Address Offset: 1Bh
Default Value: 00h
Access: Read/Write
Size: 8 bits

This register controls the bus tenure of the GMCH2-M on AGP/PCI. SMLT is an 8-bit register that controls the amount of time the GMCH2-M as an AGP/PCI bus master, can burst data on the AGP/PCI Bus. The Count Value is an 8 bit quantity, however SMLT[2:0] are reserved and assumed to be 0 when determining the Count Value. The GMCH2-M's SMLT is used to guarantee to the AGP master a minimum amount of the system resources. When the GMCH2-M begins the first PCI bus cycle after being granted the bus, the counter is loaded and enabled to count from the assertion of FRAME#. If the count expires while the GMCH2-M's grant is removed (due to AGP master request), then the GMCH2-M will lose the use of the bus, and the AGP master agent may be granted the bus. If GMCH2-M's bus grant is not removed, the GMCH2-M will continue to own the AGP/PCI bus regardless of the SMLT expiration or idle condition. Note that the GMCH2-M must always properly terminate an AGP/PCI transaction with FRAME# negation prior to the final data transfer.

The number of clocks programmed in the SMLT represents the guaranteed time slice (measured in 66Mhz PCI clocks) allotted to the GMCH2-M, after which it must complete the current data transfer phase and then surrender the bus as soon as its bus grant is removed. For example, if the SMLT is programmed to 18h, then the value is 24 AGP clocks. The default value of SMLT is 00h and disables this function. When the SMLT is disabled, the burst time for the GMCH2-M is unlimited (i.e. the GMCH2-M can burst forever).



Bit	Description
7:3	**Secondary MLT Counter Value.** Default=0 i.e. SMLT disabled
2:0	**Reserved.**

3.7.14. IOBASE—I/O Base Address Register (Device 1)

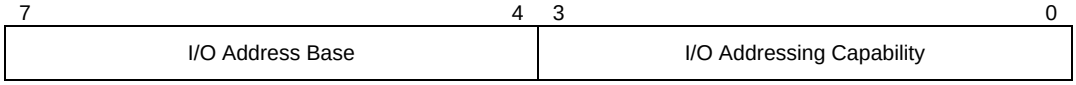
Address Offset: 1Ch
Default Value: F0h
Access: Read/Write
Size: 8 bits

This register control the processor to PCI1/AGP I/O access routing based on the following formula:

IO_BASE=< address =<IO_LIMIT

Only upper 4 bits are programmable. For the purpose of address decode, address bits A[11:0] are treated as 0. Thus the bottom of the defined I/O address range will be aligned to a 4KB boundary.

Note: BIOS must not set this register to 00h otherwise 0CF8h/0CFCh accesses will be forwarded to AGP



Bit	Description
7:4	**I/O Address Base.** Corresponds to A[15:12] of the I/O address. Default=Fh
3:0	**I/O Addressing Capability.** Hardwired to 0h indicating that only 16 bit I/O addressing is supported. Bits [31:16] of the I/O base address is assumed to be 0000h.

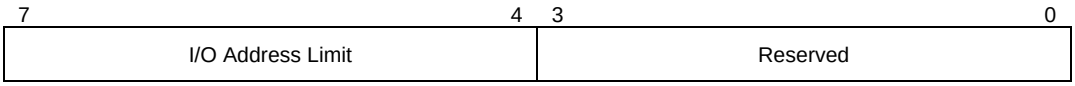
3.7.15. IOLIMIT—I/O Limit Address Register (Device 1)

Address Offset: 1Dh
Default Value: 00h
Access: Read/Write
Size: 8 bits

This register controls the processor to PCI1/AGP I/O access routing based on the following formula:

IO_BASE=< address =<IO_LIMIT

Only upper 4 bits are programmable. For the purpose of address decode address bits A[11:0] are assumed to be FFFh. Thus, the top of the defined I/O address range will be at the top of a 4KB aligned address block.

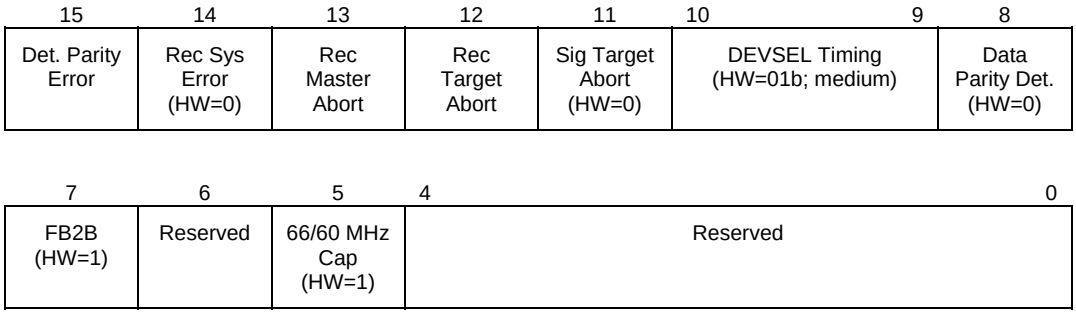


Bit	Description
7:4	**I/O Address Limit.** Corresponds to A[15:12] of the I/O address. Default=0
3:0	**Reserved.** (Only 16 bit addressing supported.)

3.7.16. SSTS—Secondary PCI-PCI Status Register (Device 1)

Address Offset: 1E-1Fh
Default Value: 02A0h
Access: Read Only, Read/Write Clear
Size: 16 bits

SSTS is a 16-bit status register that reports the occurrence of error conditions associated with secondary side (i.e. PCI1/AGP side) of the "virtual" PCI-PCI bridge embedded within GMCH2-M.



Bit	Descriptions
15	**Detected Parity Error (DPE1)**. This bit is set to a 1 to indicate GMCH2-M's detection of a parity error in the address or data phase of PCI1/AGP bus transactions. Software sets DPE1 to 0 by writing a 1 to this bit. **Note** that the function of this bit is not affected by the PERRE1 bit. Also note that PERR# is not implemented in the GMCH2-M.
14	**Received System Error (SSE1)**. This bit is hardwired to 0 since the GMCH2-M does not have an SERR# signal pin.
13	**Received Master Abort Status (RMAS1)**. This bit is set to 1 when the GMCH2-M terminates a Host-to-PCI1/AGP with an unexpected master abort. Software resets this bit to 0 by writing a 1 to it.
12	**Received Target Abort Status (RTAS1)**. When a GMCH2-M initiated transaction on PCI1/AGP is terminated with a target abort, RTAS1 is set to 1. Software resets RTAS1 to 0 by writing a 1 to it.
11	**Signaled Target Abort Status (STAS1).** STAS1 is hardwired to a 0, since the GMCH2-M does not generate target abort on PCI1/AGP.
10:9	**DEVSEL# Timing (DEVT1)**. This 2-bit field indicates the timing of the DEVSEL# signal when the GMCH2-M responds as a target on PCI1/AGP, and is hard-wired to the value **01b (medium)** to indicate the time when a valid DEVSEL# can be sampled by the initiator of the PCI cycle.
8	**Data Parity Detected (DPD1). Hardwired to 0.** GMCH2-M does not implement G_PERR# function. However, data parity errors are still detected and reported using SERR hub interface special cycles (if enabled by SERRE1 and the BCTRL register, bit 0).

Bit	Descriptions
7	**Fast Back-to-Back (FB2B1).** This bit is hardwired to 1, since GMCH2-M as a target supports fast back-to-back transactions on PCI1/AGP.
6	**Reserved**.
5	**66/60MHZ Capability: Hardwired to "1".**
4:0	**Reserved**.

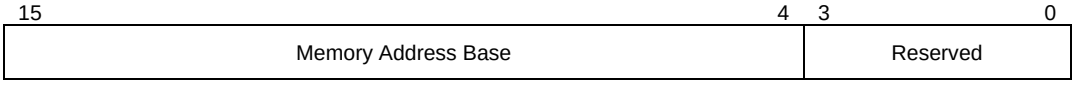
3.7.17. MBASE—Memory Base Address Register (Device 1)

Address Offset: 20-21h
Default Value: FFF0h
Access: Read/Write
Size: 16 bits

This register controls the processor to PCI1 non-prefetchable memory access routing based on the following formula:

MEMORY_BASE=< address =<MEMORY_LIMIT

The upper 12 bits of the register are Read/Write and correspond to the upper 12 address bits A[31:20] of the 32 bit address. The bottom 4 bits of this register are read-only and return zeroes when read. The configuration software must initialize this register. For the purpose of address decode address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1MB boundary.



Bit	Description
15:4	**Memory Address Base (MEM_BASE).** Corresponds to A[31:20] of the memory address.
3:0	**Reserved.**

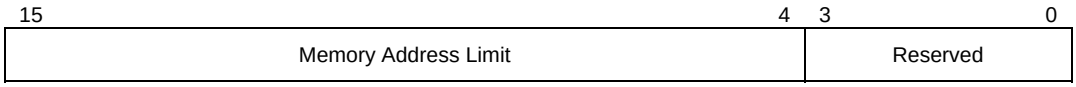
3.7.18. MLIMIT—Memory Limit Address Register (Device 1)

Address Offset: 22-23h
Default Value: 0000h
Access: Read/Write
Size: 16 bits

This register controls the processor to PCI1 non-prefetchable memory access routing based on the following formula:

MEMORY_BASE=< address =<MEMORY_LIMIT

The upper 12 bits of the register are Read/Write and correspond to the upper 12 address bits A[31:20] of the 32 bit address. The bottom 4 bits of this register are read-only and return zeroes when read. The configuration software must initialize this register. For the purpose of address decode, address bits A[19:0] are assumed to be FFFFFh. Thus, the top of the defined memory address range will be at the top of a 1MB aligned memory block.



Bit	Description
15: 4	**Memory Address Limit (MEM_LIMIT).** Corresponds to A[31:20] of the memory address. Default=0
3:0	**Reserved.**

Memory range covered by MBASE and MLIMIT registers are used to map non-prefetchable PCI1/AGP address ranges (typically where control/status memory-mapped I/O data structures of the graphics controller will reside) and PMBASE and PMLIMIT are used to map prefetchable address ranges (typically graphics local memory). This segregation allows application of USWC space attribute to be performed in a true plug-and-play manner to the prefetchable address range for improved processor-AGP memory access performance.

Configuration software is responsible for programming all address range registers (prefetchable, non-prefetchable) with the values that provide exclusive address ranges i.e. prevent overlap with each other and/or with the ranges covered with the main memory. There is no provision in the GMCH2-M hardware to enforce prevention of overlap and operations of the system in the case of overlap are not guaranteed.

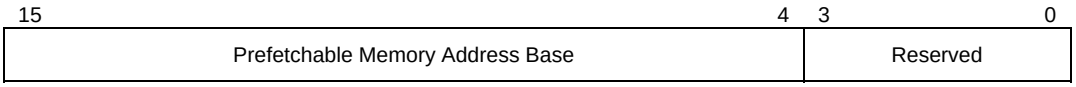
3.7.19. PMBASE—Prefetchable Memory Base Address Register (Device 1)

Address Offset: 24-25h
Default Value: FFF0h
Access: Read/Write
Size: 16 bits

This register controls the processor to PCI1 prefetchable memory accesses routing based on the following formula:

PREFETCHABLE_MEMORY_BASE=< address =<PREFETCHABLE_MEMORY_LIMIT

The upper 12 bits of the register are Read/Write and correspond to the upper 12 address bits A[31:20] of the 32 bit address. The bottom 4 bits of this register are read-only and return zeroes when read. The configuration software must initialize this register. For the purpose of address decode, address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1MB boundary.



Bit	Description
15: 4	**Prefetchable Memory Address Base (PMEM_BASE).** Corresponds to A[31:20] of the memory address. Default=FFF
3:0	**Reserved.**

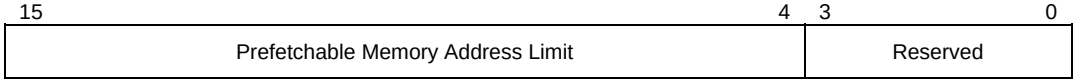
3.7.20. PMLIMIT—Prefetchable Memory Limit Address Register (Device 1)

Address Offset: 26-27h
Default Value: 0000h
Access: Read/Write
Size: 16 bits

This register controls the processor to PCI1 prefetchable memory accesses routing based on the following formula:

PREFETCHABLE_MEMORY_BASE=< address =<PREFETCHABLE_MEMORY_LIMIT

The upper 12 bits of the register are Read/Write and correspond to the upper 12 address bits A[31:20] of the 32 bit address. The bottom 4 bits of this register are read-only and return zeroes when read. The configuration software must initialize this register. For the purpose of address decode, address bits A[19:0] are assumed to be FFFFFh. Thus, the top of the defined memory address range will be at the top of a 1MB aligned memory block.



Bit	Description
15: 4	**Prefetchable Memory Address Limit (PMEM_LIMIT).**Corresponds to A[31:20] of the memory address. Default=0
3:0	**Reserved.**

Note: That prefetchable memory range is supported to allow segregation by the configuration software between the memory ranges that must be defined as UC and the ones that can be designated as a USWC (i.e. prefetchable) from the processor perspective.

3.7.21. BCTRL—PCI-PCI Bridge Control Register (Device 1)

Address Offset: 3Eh
Default: 00h
Access: Read/Write
Size 8 bits

This register provides extensions to the PCICMD1 register that are specific to PCI-PCI bridges. The BCTRL provides additional control for the secondary interface (PCI1/AGP) as well as some bits that affect the overall behavior of the "virtual" PCI-PCI bridge embedded within GMCH2-M, e.g. VGA compatible address ranges mapping.

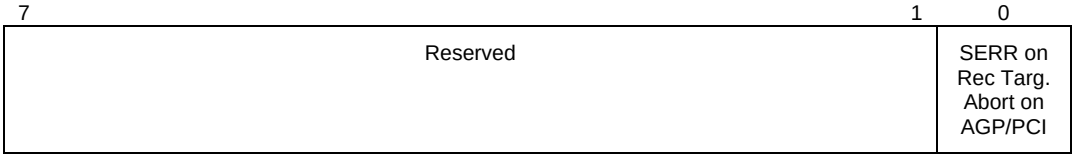
7	6	5	4	3	2	1	0
FB2B EN (HW=0)	Sec Bus Reset (HW=0)	Master Abort Mode (HW=0)	Reserved	VGA EN	ISA Enable	SERR# EN (HW=0)	Parity Err Response EN

Bit	Descriptions
7	**Fast Back to Back Enable.** Since there is only one target allowed on AGP this bit is meaningless. This bit is **hardwired to "0".**
6	**Secondary Bus Reset:** GMCH2-M does not support generation of reset via this bit on the AGP and therefore this bit is **hardwired to "0".** **Note that the only way to perform a hard reset of the AGP is via the system reset either initiated by software or hardware via ICH.**
5	**Master Abort Mode:** This bit is **hardwired to "0".** This means when acting as a master on AGP/PCI1 the GMCH2-M will drop writes on the "floor" and return all "1" during reads when a Master Abort occurs.
4	**Reserved.**

Bit	Descriptions
3	**VGA Enable.** This bit works with the MDA present bit , GMCHCFG[3], of device 0 to control the routing of processor initiated transactions targeting VGA compatible I/O and memory address ranges. When this bit is set , the GMCH2-M will forward the following processor accesses to the AGP: 1) memory accesses in the range 0A0000h to 0BFFFFh 2) I/O addresses where A[9:0] are in the ranges 3B0h to 3BBh and 3C0h to 3DFh (inclusive of ISA address aliases - A[15:10] are not decoded) When this bit is set , forwarding of these accesses issued by the processor is independent of the I/O address and memory address ranges defined by the previously defined base and limit registers. Forwarding of these accesses is also independent of the settings of the bit 2 (ISA Enable) of this register if this bit is “1”. If the VGA enable bit is set, then accesses to IO address range x3BCh - x3BFh are forwarded to hub interface. If the VGA enable bit is not set then accesses to IO address range x3BCh - x3BFh are treated just like any other IO accesses i.e. the cycles are forwarded to AGP if the address is within IOBASE and IOLIMIT and ISA enable bit is not set, otherwise they are forwarded to hub interface. If this bit is “0” (default) , then VGA compatible memory and I/O range accesses are not forwarded to AGP but rather they are mapped to primary PCI unless they are mapped to AGP via I/O and memory range registers defined above (IOBASE, IOLIMIT, MBASE, MLIMIT, PMBASE, PMLIMIT) The following table shows the behavior for all combinations of MDA and VGA: **VGA MDA Behavior** 0 0 All References to MDA and VGA Go To hub interface 0 1 Illegal Combination (DO NOT USE) 1 0 All References To VGA Go To AGP MDA-only references (I/O Address 3BF and aliases) will go to hub interface. 1 1 VGA References go to AGP/PCI; MDA References go to the hub interface
2	**ISA Enable:** Modifies the response by the GMCH2-M to an I/O access issued by the processor that target ISA I/O addresses. This applies only to I/O addresses that are enabled by the IOBASE and IOLIMIT registers. When this bit is set to 1 GMCH2-M will not forward to PCI1/AGP any I/O transactions addressing the last 768 bytes in each 1KB block even if the addresses are within the range defined by the IOBASE and IOLIMIT registers. Instead of going to PCI1/AGP these cycles will be forwarded to the hub interface where they can eventually be subtractively or positively claimed by the ISA bridge. If this bit is “0” (default) then all addresses defined by the IOBASE and IOLIMIT for processor I/O transactions will be mapped to PCI1/AGP.
1	**SERR# Enable.** This bit normally controls forwarding SERR# on the secondary interface to the primary interface. The GMCH2-M does not support the SERR# signal on the AGP/PCI1 bus. This bit is hardwired to a “0”.
0	**Parity Error Response Enable:** Controls GMCH2-M’s response to data phase parity errors on PCI1/AGP. G_PERR# is not implemented by the GMCH2-M. However, when this bit is set to 1, address and data parity errors on PCI1 are reported via SERR messaging, if enabled by SERRE1. If this bit is reset to 0, then address and data parity errors on PCI1/AGP are not reported via SERR messaging. Other types of error conditions can still be signaled via SERR messaging independent of this bit’s state.

3.7.22. ERRCMD1—Error Command Register (Device 1)

Address Offset: 40h
Default: 00h
Access: Read/Write
Size 8 bits



Bit	Descriptions
7:1	**Reserved.**
0	**SERR on Receiving Target Abort on AGP/PCI.** When this bit is set to “1” the GMCH2-M generates an SERR hub interface special cycle when an GMCH2-M originated AGP/PCI cycle is terminated with a Target Abort. If this bit is “0” then reporting of this condition is disabled.

3.8. Graphics Device Registers (Device 2 - VISIBLE IN GFX MODE ONLY)

These registers are accessible through the configuration mechanism defined in an earlier section of this document.

Table 9. Device 2 Configuration Space Address Map (Internal Graphics)

Address Offset	Register Symbol	Register Name	Default Value	Access Type
00-01h	VID2	Vendor Identification	8086h	RO
02-03h	DID2	Device Identification	1112h	RO
04-05h	PCICMD2	PCI Command Register	0004h	Read/Write
06-07h	PCISTS2	PCI Status Register	02B0h	RO
08h	RID2 (A0)	Revision Identification for A0-step	10h	RO
08h	RID2 (A1)	Revision Identification for A1-step	11h	RO
09h	PI	Programming Interface	00h	RO
0Ah	SUBC2	Sub-Class Code	00h	RO
0Bh	BCC2	Base Class Code	03h	RO
0Ch	CLS	Cache Line Size Register	00h	RO
0Dh	MLT2	Master Latency Timer	00h	RO
0Eh	HDR2	Header Type	01h	RO
0Fh	BIST	BIST Register	00h	RO
10-13h	GMADR	Graphics Memory Range Address	00000008h	Read/Write

Address Offset	Register Symbol	Register Name	Default Value	Access Type
14-17h	MMADR	Memory Mapped Range Address	00000000h	Read/Write
18-2Bh	—	Reserved	00h	—
2C-2Dh	SVID	Subsystem Vendor ID	0000h	Read/WriteO
2E-2Fh	SID	Subsystem ID	0000h	Read/WriteO
30-33h	ROMADR	Video Bios ROM Base Address	00000000h	RO
34h	CAPPOINT	Capabilities Pointer	DCh	RO
35-3Bh	—	Reserved	00h	—
3Ch	INTRLINE	Interrupt Line Register	00h	Read/Write
3Dh	INTRPIN	Interrupt Pin Register	01h	RO
3Eh	MINGNT	Minimum Grant Register	00h	RO
3Fh	MAXLAT	Maximum Latency Register	00h	RO
40-DBh	—	Reserved	00h	—
DC-DDh	PM_CAPID	Power Management Capabilities	0001h	RO
DE-DFh	PM_CAP	Power Management Capabilities	0022h	RO
E0-E1h	PM_CS	Power Management Control	0000h	Read/Write
E2-FFh	—	Reserved	00h	—

3.8.1. VID2—Vendor Identification Register (Device 2)

Address Offset: 00h–01h
Default Value: 8086h
Attribute: Read Only

The VID Register contains the vendor identification number. This 16-bit register combined with the Device Identification Register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Description
15:0	**Vendor Identification Number.** This is a 16-bit value assigned to Intel®.

3.8.2. DID2—Device Identification Register (Device 2)

Address Offset: 02h–03h
Default Value: 1132h
Attribute: Read Only

This 16-bit register combined with the Vendor Identification register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Description
15:0	**Device Identification Number.** This is a 16 bit value assigned to the internal graphics device of the GMCH2-M. 1132h = Device ID for Device 2.

3.8.3. PCICMD2—PCI Command Register (Device 2)

Address Offset: 04h–05h
Default: 0004h
Access: Read Only, Read/Write

This 16-bit register provides basic control over the GMCH2-M's ability to respond to PCI cycles. The PCICMD Register in GMCH2-M disables GMCH2-M PCI compliant master accesses to main memory.

15 … 10	9	8
Reserved (0)	FB2B (HW=0)	SERR En (HW=0)

7	6	5	4	3	2	1	0
Addr/Data Stepping (HW=0)	Parity Error En (HW=0)	VGA Pal Sn (HW=0)	Mem WR & Inval En (HW=0)	Special Cycle En (HW=0)	Bus Master En	Mem Acc En	I/O Acc En

Bits	Description
15:10	**Reserved**.
9	**Fast Back-to-Back (FB2B)—RO.** (Not Implemented). Hardwired to 0.
8	**SERR# Enable (SERRE) —RO.** (Not Implemented). Hardwired to 0.
7	**Address/Data Stepping—RO.** (Not Implemented). Hardwired to 0.
6	**Parity Error Enable (PERRE) —RO.** (Not Implemented). Hardwired to 0. Since GMCH2-M belongs to the category of devices that does not corrupt programs or data in system memory or hard drives, GMCH2-M ignores any parity error that it detects and continues with normal operation.
5	**Video Palette Snooping (VPS) —RO.** This bi is hardwired to 0 to disable snooping.
4	**Memory Write and Invalidate Enable (MWIE) —RO.** Hardwired to 0. GMCH2-M does not support memory write and invalidate commands.
3	**Special Cycle Enable (SCE) —RO.** This bit is hardwired to 0. GMCH2-M ignores Special cycles.

2	**Bus Master Enable (BME) —RO.** Hardwired to 1 to enable GMCH2-M to function as a PCI compliant master.
1	**Memory Access Enable (MAE) —Read/Write.** This bit controls GMCH2-M's response to memory space accesses. 0 = Disable (default). 1 = Enable.
0	**I/O Access Enable (IOAE) —Read/Write.** This bit controls GMCH2-M's response to I/O space accesses. 0 = Disable (default). 1 = Enable.

3.8.4. PCISTS2—PCI Status Register (Device 2)

Address Offset: 06h–07h
Default Value: 02B0h
Access: Read Only

PCISTS is a 16-bit status register that reports the occurrence of a PCI compliant master abort and PCI compliant target abort. PCISTS also indicates the DEVSEL# timing that has been set by the GMCH2-M hardware.

15	14	13	12	11	10 9	8
Detected Par Error (HW=0)	Sig Sys Error (HW=0)	Recog Mast Abort Sta (HW=0)	Rec Target Abort Sta (HW=0)	Sig Target Abort Sta (HW=0)	DEVSEL# Timing (HW=01)	Data Par Detected (HW=0)

7	6	5	4	3 0
FB2B (HW=1)	User Def Format (HW=0)	66 MHz PCI Cap (HW=1)	Cap List (HW=1)	Reserved

Bits	Description
15	**Detected Parity Error (DPE) —RO.** Since GMCH2-M does not detect parity, this bit is always set to 0.
14	**Signaled System Error (SSE) —RO.** The GMCH2-M Graphics device never asserts SERR#, therefore this bit is hardwired to 0.
13	**Received Master Abort Status (RMAS) —RO.** The GMCH2-M Graphics device never gets a Master Abort, therefore this bit is hardwired to 0.
12	**Received Target Abort Status (RTAS) —RO.** The GMCH2-M Graphics device never gets a Target Abort, therefore this bit is hardwired to 0.
11	**Signaled Target Abort Status (STAS).** Hardwired to 0. GMCH2-M does not use target abort semantics.
10:9	**DEVSEL# Timing (DEVT) —RO.** This 2-bit field indicates the timing of the DEVSEL# signal when GMCH2-M responds as a target. Hardwired to 01 to indicate that GMCH2-M is a medium decode device.
8	**Data Parity Detected (DPD) —Read/WriteC.** Since Parity Error Response is hardwired to disabled (and GMCH2-M does not do any parity detection), this bit is hardwired to 0**.**
7	**Fast Back-to-Back (FB2B).** Hardwired to 1. GMCH2-M accepts fast back-to-back when the transactions are not to the same agent.
6	**User Defined Format (UDF).** Hardwired to 0.
5	**66 MHz PCI Capable (66C).** Hardwired to 1 indicating that GMCH2-M is 66MHz PCI capable. Note that there is nothing in the design that prevents is 66MHz PCI from working, but we support on a subset of 66MHz PCI that is essentially equivalent to AGP. 66MHz PCI is not a feature we validate.
4	**CAP LIST—RO.** This bit is set to 1 to indicate that the register at 34h provides an offset into the function's PCI Configuration Space containing a pointer to the location of the first item in the list.
3:0	**Reserved.**

3.8.5. RID2—Revision Identification Register (Device 2)

Address Offset: 08h
Default Value: 10h for A0-step silicon
11h for A1-step silicon
Access: Read Only

This register contains the revision number of GMCH2-M. These bits are read only and writes to this register have no effect.

Bits	Description
7:0	**Revision Identification Number.** This is an 8-bit value that indicates the revision identification number for GMCH2-M. The four MSB's are for process differentiation and the four LSB's indicate stepping. Default = 10h

3.8.6. PI—Programming Interface Register (Device 2)

Address Offset: 09h
Default Value: 00h
Access: Read Only

This register contains the device-programming interface for GMCH2-M.

Bits	Description
7:0	**Programming Interface (PI).** 00h=Hardwired as a Display controller.

3.8.7. SUBC2—Sub-Class Code Register (Device 2)

Address Offset: 0Ah
Default Value: 00h
Access: Read Only
Size: 8 bits

This register contains the Sub-Class Code for the GMCH2-M Device 2.

Bit	Description
7:0	**Sub-Class Code (SUBC)**. This is an 8-bit value that indicates the category of Display controller into which GMCH2-M falls. The code is 00h indicating a VGA compatible device. Default = 00h

3.8.8. BCC2—Base Class Code Register (Device 2)

Address Offset: 0Bh
Default Value: 03h
Access: Read Only
Size: 8 bits

This register contains the Base Class Code of the GMCH2-M Function #1.

Bit	Description
7:0	**Base Class Code (BASEC)**. This is an 8-bit value that indicates the Base Class Code for GMCH2-M. This code has the value **03h**, indicating a Display controller.

3.8.9. CLS—Cache Line Size Register (Device 2)

Address Offset: 0Ch
Default Value: 00h
Access: Read only

GMCH2-M does not support this register as a PCI slave.

Bits	Description
7:0	**Cache Line Size (CLS). Hardwired to 0s**. GMCH2-M as a PCI compliant master does not use the Memory Write and Invalidate command and, in general, does not perform operations based on cache line size.

3.8.10. MLT2—Master Latency Timer Register (Device 2)

Address Offset: 0Dh
Default Value: 00h
Access: Read Only

Bits	Description
7:0	**Master Latency Timer Count Value. Hardwired to 0s**. GMCH2-M does not support the programmability of the master latency timer because it does not perform bursts.

3.8.11. HDR2—Header Type Register (Device 2)

Address Offset: 0Eh
Default Value: 00h
Access: Read Only

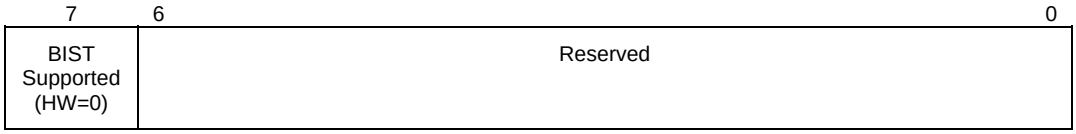
This register contains the Header Type of GMCH2-M.

Bits	Description
7:0	**Header Type (HTYPE).** This is an 8-bit value that indicates the Header Type for GMCH2-M. 00h = Indicating a basic (i.e., single function) configuration space format.

3.8.12. BIST—BIST Register (Device 2)

Address Offset: 0Fh
Default Value: 00h
Access: Read Only

This register is used for control and status of Built In Self Test (BIST).

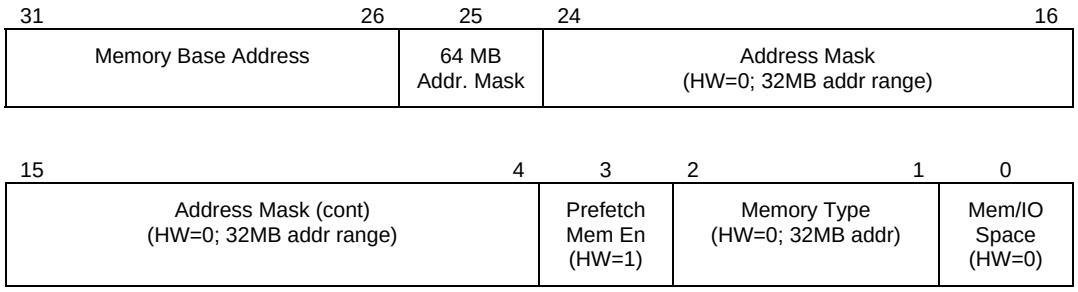


Bits	Description
7	**BIST Supported.** BIST is **not supported**. This bit is hardwired to 0.
6:0	**Reserved**.

3.8.13. GMADR-Graphics Memory Range Address Register (Device 2)

Address Offset: 10–13h
Default Value: 00000008h
Access: Read/Write, Read Only

This register requests allocation for internal Graphics memory. The allocation is for either 32 MB or 64 MB of memory space (selected by bit 0 of the Device 0 MISCC Reg) and the base address is defined by bits [31:25,24].

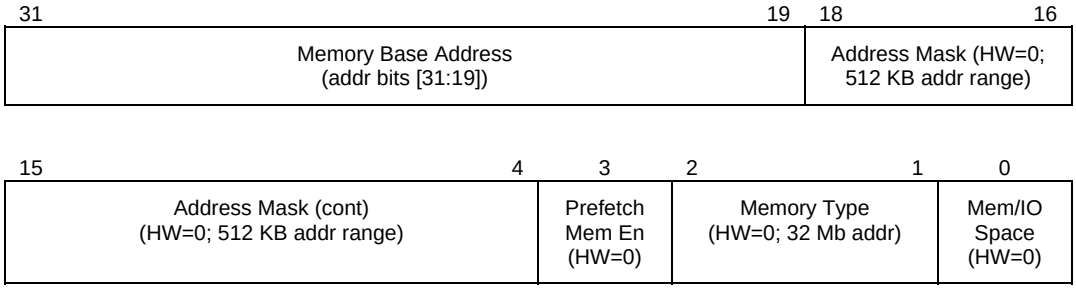


Bit	Descriptions
31:26	**Memory Base Address—Read/Write.** Set by the OS, these bits correspond to address signals [31:26].
25	**64 MB Address Mask—RO , Read/Write.** If Device 0 MISCC Reg bit 0 = 0, then this bit is RO with a value of 0, indicating a memory range of 64 MB. If Device 0 MISCC Reg bit 0 = 1, then this bit is Read/Write, indicating a memory range of 32 MB.
24:4	**Address Mask—RO.** Hardwired to 0s to indicate 32 MB address range.
3	**Prefetchable Memory—RO.** Hardwired to 1 to enable prefetching.
2:1	**Memory Type—RO.** Hardwired to 0 to indicate 32-bit address.
0	**Memory/IO Space—RO.** Hardwired to 0 to indicate memory space.

3.8.14. MMADR—Memory Mapped Range Address Register (Device 2)

Address Offset: 14–17h
Default Value: 00000000h
Access: Read/Write, Read Only

This register requests allocation for GMCH2-M registers and instruction ports. The allocation is for 512 KB and the base address is defined by bits [31:19].



Bit	Descriptions
31:19	**Memory Base Address—Read/Write.** Set by the OS, these bits correspond to address signals [31:19].
18:4	**Address Mask—RO.** Hardwired to 0s to indicate 512 KB address range.
3	**Prefetchable Memory—RO.** Hardwired to 0 to prevent prefetching.
2:1	**Memory Type—RO.** Hardwired to 0s to indicate 32-bit address.
0	**Memory / IO Space—RO.** Hardwired to 0 to indicate memory space.

3.8.15. SVID—Subsystem Vendor Identification Register (Device 2)

Address Offset: 2C–2Dh
Default Value: 0000h
Access: Read/Write Once

Bit	Descriptions
15:0	**Subsystem Vendor ID (Read/WriteO).** This value is used to identify the vendor of the subsystem. The default value is 0000h. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This Register can only be cleared by a Reset.

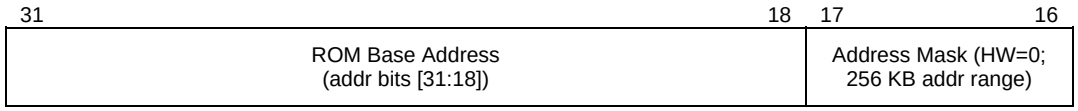
3.8.16. SID—Subsystem Identification Register (Device 2)

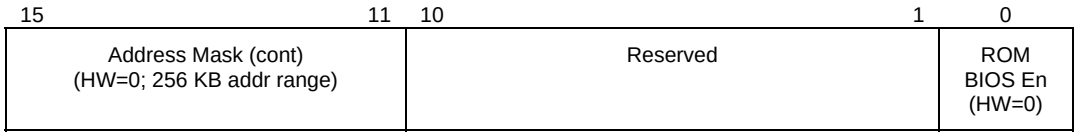
Address Offset: 2E–2Fh
Default Value: 0000h
Access: Read/Write Once

Bit	Descriptions
15:0	**Subsystem ID (Read/WriteO).** This value is used to identify a particular subsystem. The default value is 0000h. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This Register can only be cleared by a Reset.

3.8.17. ROMADR - Video BIOS ROM Base Address Registers (Device 2)

Address Offset: 30–33h
Default Value: 00000000h
Access: Read Only





Bit	Descriptions
31:18	**ROM Base Address—RO.** Hardwired to 0s.
17:11	**Address Mask—RO.** Hardwired to 0s to indicate 256 KB address range.
10:1	**Reserved.** Hardwired to 0s.
0	**ROM BIOS Enable—RO.** 0 = ROM not accessible.

3.8.18. CAPPOINT—Capabilities Pointer Register (Device 2)

Address Offset: 34h
Default Value: DCh
Access: Read Only

Bit	Descriptions
7:0	**Pointer to the start of AGP standard register block.** Since there is no AGP bus on GMCH2-M, this field is set to DCh to point to the Power Management Capabilities ID Register

3.8.19. INTRLINE—Interrupt Line Register (Device 2)

Address Offset: 3Ch
Default Value: 00h
Access: Read/Write

Bit	Descriptions
7:0	**Interrupt Connection.** Used to communicate interrupt line routing information. POST software writes the routing information into this register as it initializes and configures the system. The value in this register indicates which input of the system interrupt controller that the device's interrupt pin is connected to.

3.8.20. INTRPIN—Interrupt Pin Register (Device 2)

Address Offset: 3Dh
Default Value: 01h
Access: Read Only

Bit	Descriptions
7:0	**Interrupt Pin.** As a single function device, GMCH2-M specifies INTA# as its interrupt pin. 01h=INTA#.

3.8.21. MINGNT—Minimum Grant Register (Device 2)

Address Offset: 3Eh
Default Value: 00h
Access: Read Only

Bit	Descriptions
7:0	**Minimum Grant Value.** GMCH2-M does not burst as a PCI compliant master. Bits[7:0]=00h.

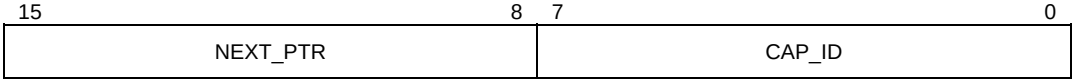
3.8.22. MAXLAT—Maximum Latency Register (Device 2)

Address Offset: 3Fh
Default Value: 00h
Access: Read Only

Bit	Descriptions
7:0	**Maximum Latency Value.** Bits[7:0]=00h. GMCH2-M has no specific requirements for how often it needs to access the PCI bus.

3.8.23. PM_CAPID—Power Management Capabilities ID Register (Device 2)

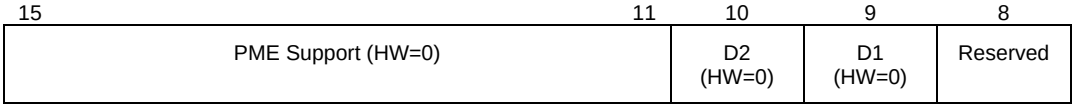
Address Offset: DCh–DDh
Default Value: 0001h
Access: Read Only

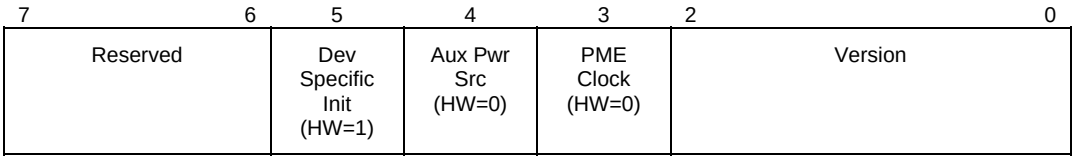


Bits	Description
15:8	**NEXT_PTR.** This contains a pointer to next item in capabilities list. This the final capability in the list and must be set to 00h.
7:0	**CAP_ID.** SIG defines this ID is 01h for power management.

3.8.24. PM_CAP—Power Management Capabilities Register (Device 2)

Address Offset: DEh–DFh
Default Value: 0022h
Access: Read Only

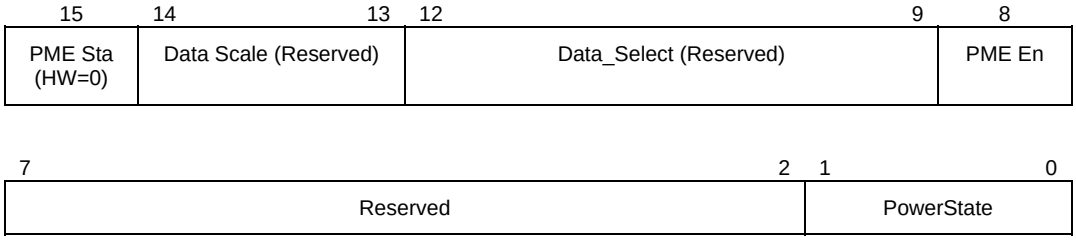




Bits	Description
15:11	**PME Support.** This field indicates the power states in which GMCH2-M may assert PME#. Hardwired to 0 to indicate that GMCH2-M does not assert the PME# signal.
10	**D2.** Hardwired to 0 to indicate D2 power management state is not supported.
9	**D1.** Hardwired to0 to indicate that D1 power management state is NOT supported.
8:6	**Reserved.** Read as 0s.
5	**Device Specific Initialization (DSI).** Hardwired to 1 to indicate that special initialization of GMCH2-M is required before generic class device driver is to use it.
4	**Auxiliary Power Source.** Hardwired to 0.
3	**PME Clock.** Hardwired to 0 to indicate GMCH2-M does not support PME# generation.
2:0	**Version.** Hardwired to 010b to indicate there are 4 bytes of power management registers implemented and that this device complies with revision 1.1 of the *PCI Power Management Interface Specification*.

3.8.25. PM_CS - Power Management Control/Status Register (Device 2)

Address Offset: E0h–E1h
Default Value: 0000h
Access: Read/Write



Bits	Description
15	**PME_Status —RO.** This bit is 0 to indicate that GMCH2-M does not support PME# generation from D3 (cold).
14:13	**Data Scale (Reserved) —RO.** GMCH2-M does not support data register. This bit always returns 0 when read; write operations have no effect.
12:9	**Data_Select (Reserved) —RO**. GMCH2-M does not support data register. This bit always returns 0 when read; write operations have no effect.
8	**PME_En—Read/Write.** This bit is 0 to indicate that PME# assertion from D3 (cold) is disabled.
7:2	**Reserved.** Always returns 0s when read; write operations have no effect.
1:0	**PowerState—Read/Write.** This field indicates the current power state of GMCH2-M and can be used to set GMCH2-M into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs. 00 = D0 01 = D1 (Not supported in GMCH2-M) 10 = D2 (Not supported in GMCH2-M) 11 = D3

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4. Functional Description

This chapter describes the Graphics and Memory Controller Hub (GMCH2-M) interfaces, and boot sequencing. The “System Address Map” provides a system-level address memory map and describes the memory space controls provided by the GMCH2-M.

4.1. System Memory and I/O Address Map

A mobile Intel® Pentium® III processor or mobile Intel® Celeron™ processor system based on the GMCH2-M, supports 4 GB of addressable memory space and 64 KB+3 of addressable I/O space. (The Pentium® III bus I/O addressability is 64KB + 3). There is a programmable memory address (PAM) space under the 1 MB region which can be controlled with programmable attributes of Write Only, or Read Only. Attribute programming is described in the Configuration Register Description section. This section focuses on how the memory space is partitioned and what these separate memory regions are used for. The I/O address space is explained at the end of this section.

The mobile Intel® Pentium® III processor, mobile Intel® Celeron™ processor supports addressing of memory ranges larger than 4 GB. The GMCH2-M Host Bridge claims any access over 4 GB by terminating transaction (without forwarding it to the hub interface). Writes are terminated by dropping the data and for reads the GMCH2-M returns all zeros on the host bus.

In the following sections, it is assumed that all of the compatibility memory ranges reside on the hub interface. The exceptions to this rule are the VGA ranges, which may be mapped to the internal Graphics Device.

The GMCH2-M Memory Map includes a number of programmable ranges, ALL of these ranges MUST be unique and NON-OVERLAPPING. There are NO Hardware Interlocks to prevent problems in the case of overlapping ranges. Accesses to overlapped ranges may produce indeterminate results.

4.1.1. Memory Address Space

The following figure shows a high-level representation of the system memory address map. Figure 5 provides additional details on mapping specific memory regions as defined and supported by the GMCH2-M chipset.

Figure 4. System Memory Address Map

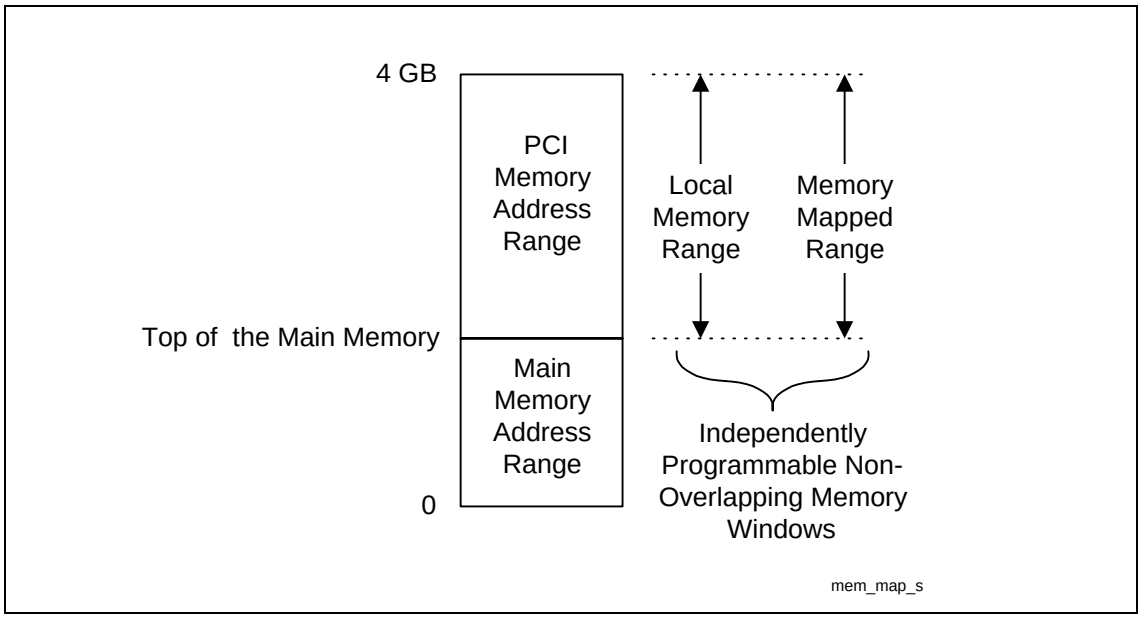
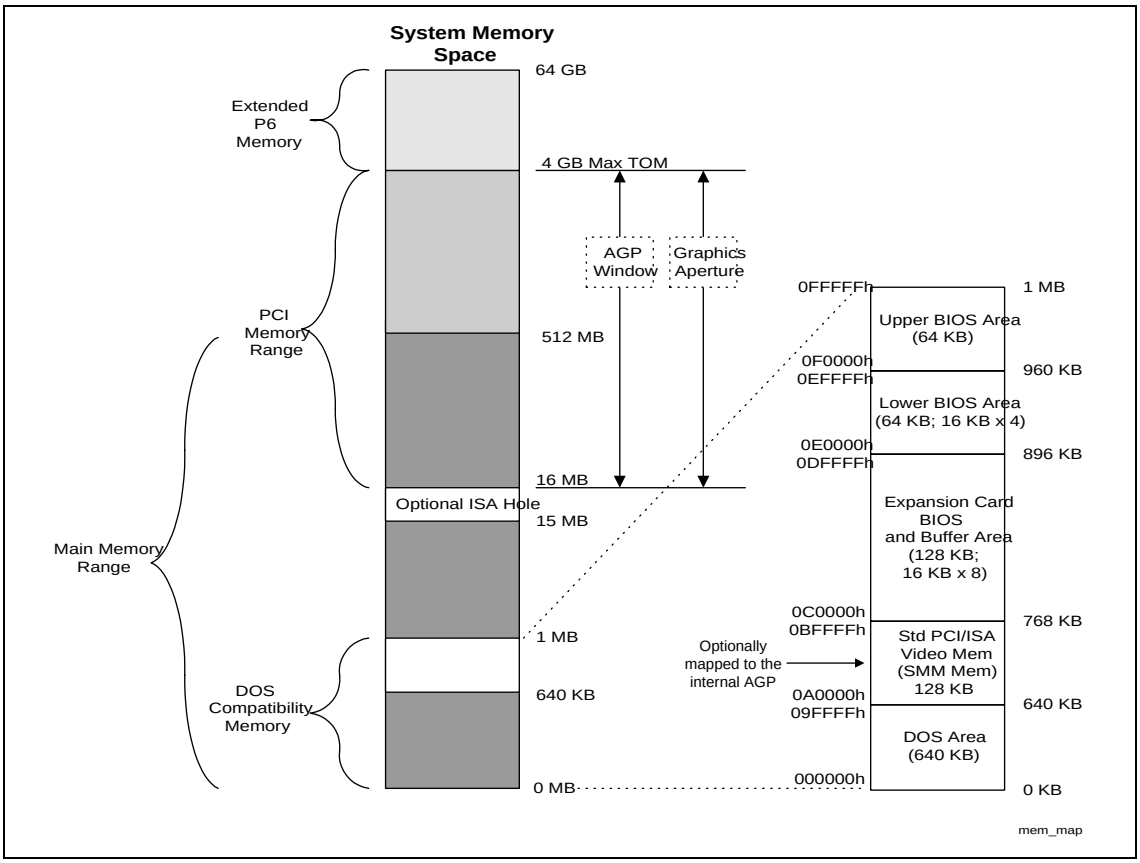


Figure 5. Detailed Memory System Address Map



4.2. DOS Compatibility Memory Space

This area is divided into the following address regions:

- 0 - 640 KB DOS Area
- 640 - 768 KB Video Buffer Area
- 768 - 896 KB in 16KB sections (total of 8 sections) - Expansion Area
- 896 -960 KB in 16KB sections (total of 4 sections) - Extended System BIOS Area
- 960 KB - 1 MB Memory (BIOS Area) - System BIOS Area

The Intel® 815EM chipset supports all sixteen memory segments of interest in the compatibility area. Thirteen of the memory ranges can be enabled or disabled independently for both read and write cycles.

Table 10. Memory Segments and Their Attributes

Memory Segments	Attributes	Comments
000000H - 09FFFFH	Fixed - always mapped to main DRAM	0 to 640K - DOS Region
0A0000H - 0BFFFFH	Mapped to the hub interface, AGP/PCI bus or internal graphics - configurable as SMM space	Video Buffer (physical DRAM configurable as SMM space)
0C0000H - 0C3FFFH	WE RE	Add-on BIOS
0C4000H - 0C7FFFH	WE RE	Add-on BIOS
0C8000H - 0CBFFFH	WE RE	Add-on BIOS
0CC000H - 0CFFFFH	WE RE	Add-on BIOS
0D0000H - 0D3FFFH	WE RE	Add-on BIOS
0D4000H - 0D7FFFH	WE RE	Add-on BIOS
0D8000H - 0DBFFFH	WE RE	Add-on BIOS
0DC000H - 0DFFFFH	WE RE	Add-on BIOS
0E0000H - 0E3FFFH	WE RE	BIOS Extension
0E4000H - 0E7FFFH	WE RE	BIOS Extension
0E8000H - 0EBFFFH	WE RE	BIOS Extension
0EC000H - 0EFFFFH	WE RE	BIOS Extension

Memory Segments	Attributes	Comments
0F0000H - 0FFFFFH	WE RE	BIOS Area

4.2.1.1. DOS Area (00000h-9FFFh)

The DOS area is 640 KB in size is always mapped to the main memory controlled by the GMCH2-M.

4.2.1.2. Video Buffer Area (A0000h-BFFFFh)

The 128KB graphics adapter memory region is normally mapped to a legacy video device on the PCI bus (typically VGA controller). This memory area is not controlled by attribute bits of the PAM register. processor-initiated cycles in this region are forwarded to the hub interface or the AGP/Internal Graphics Device for termination. Accesses to this range are directed to either the hub interface or AGP/internal Graphics Device based on the configuration. The configuration are specified by:

- AGP on/off configuration bit
- AGP off: GMS bits of the SMRAM register in the GMCH2-M Device #0 configuration space. There is additional steering information coming from the Device #2* configuration registers and from some of the VGA registers in the Graphics device.
- AGP on: PCICMD1 (PCI-PCI Command) and BCTRL (PCI-PCI Bridge Control) registers in Device #1 configuration registers

The control is applied for accesses initiated from any of the system interface i.e. processor bus, the hub interface, or AGP (if enabled).

For Hub interface to AGP/PCI bus accesses, only memory write operations are supported. Any AGP/PCI initiated VGA accesses targeting the GMCH2-M will master abort.

This region is also the default region for SMM space in GFX mode. The SMRAM Control register controls how SMM accesses to this space are treated.

4.2.1.3. Monochrome Adapter (MDA) Range (B0000h - B7FFFh)

Legacy support requires the ability to have a second graphics controller (monochrome) in the system.

In an AGP system, accesses in the standard VGA range are forwarded to the AGP bus (depending on configuration bits). Since the monochrome adapter may be on the hub interface/PCI (or ISA) bus, GMCH2-M must decode cycles in the MDA range and forward them to the hub interface. This capability is controlled by a configuration bit (MDA bit – Device 0, BEh). In addition to the memory range B0000h to B7FFFh, the GMCH2-M decodes IO cycles at 3B4h, 3B5h, 3B8h, 3B9h, 3BAh and 3BFh and forwards them to the hub interface bus

In an internal graphics system, the GMS bits of the SMRAM register in Device #0, bits in the Device #2 PCICMD2 register and bits from some of the VGA registers control this functionality.

4.2.1.4. Expansion Area (C0000h-DFFFFh)

This 128 KB ISA Expansion region is divided into eight 16 KB segments. Each segment can be assigned one of four Read/Write states: read-only, write-only, Read/Write, or disabled. Typically, these blocks are mapped through GMCH2-M and are subtractively decoded to ISA space. Memory that is disabled is not remapped.

4.2.1.5. Extended System BIOS Area (E0000h-EFFFFh)

This 64 KB area is divided into four 16 KB segments. Each segment can be assigned independent read and write attributes so it can be mapped either to main DRAM or to the hub interface. Typically, this area is used for RAM or ROM. Memory segments that are disabled are not remapped elsewhere.

4.2.1.6. System BIOS Area (F0000h-FFFFFh)

This area is a single 64KB segment. This segment can be assigned read and write attributes. It is by default (after reset) Read/Write disabled and cycles are forwarded to the hub interface. By manipulating the Read/Write attributes, the GMCH2-M can “shadow” BIOS into the main DRAM. When disabled, this segment is not remapped.

4.3. Extended Memory Area

This memory area covers 10 0000h (1 MB) to FFFF FFFFh (4 GB-1) address range and it is divided into the following regions:

- Main DRAM Memory from 1 MB to the Top of Main Memory (TOM); maximum of 512 MB.
- PCI Memory space from the Top of Memory to 4 GB

4.3.1. Main DRAM Address Range (0010_0000h to TOM)

The address range from 1 MB to the top of main memory (TOM) is mapped to main DRAM address range. The Tom of memory is limited to 512Mb. All accesses to addresses within this range will be forwarded to the DRAM unless a hole in this range is created.

4.3.1.1. 15MB-16MB Hole Area

A hole can be created at 15MB-16MB as controlled by the fixed hole enable (FDHC register) in Device 0 space. Accesses within this hole are forwarded to the hub interface. The range of physical DRAM memory disabled by opening the hole is not remapped to the Top of the memory – that physical DRAM space is not accessible. This 15MB-16MB hole is an optionally enabled ISA hole. Video accelerators originally used this hole. It is also used by validation and customer SV teams for some of their test cards. That is why it is being supported. There is no inherent BIOS request for the 15-16 hole.

4.3.1.2. Extended SMRAM Address Range

The HSEG and TSEG SMM transaction address spaces reside in this extended memory area. This memory resource is normally hidden from the system OS so that the processor has immediate access to this memory space upon entry to SMM.

4.3.1.3. HSEG (High Segment)

SMM-mode processor accesses to enabled HSEG are remapped to 000A0000h-000BFFFFh. Non-SMM-mode processor accesses to enabled HSEG are considered invalid are terminated immediately on the FSB. The exception to this is non-SMM-mode Write Back cycles. They are remapped to SMM space to maintain cache coherency. AGP and hub interface originated cycles to enabled SMM space are not allowed. Physical DRAM behind the HSEG transaction address is not remapped and is not accessible.

4.3.1.3.1. TSEG (Top of Memory Segment)

TSEG can be up to 1MB in size and is at the top of memory (TOM). SMM-mode processor accesses to enabled TSEG access the physical DRAM at the same address. Non-SMM-mode processor accesses to enabled TSEG are considered invalid and are terminated immediately on the FSB. The exception is non-SMM-mode Write Back cycles. They are directed to the physical SMM space to maintain cache coherency. AGP and Hub interface originated cycles to enabled SMM memory space are not allowed.

The size of the SMRAM space is determined by the USMM value in the SMRAM register. When the extended SMRAM space is enabled, non-SMM processor accesses and all other accesses in this range are forwarded to the hub interface. When SMM is enabled the amount of memory available to the system is equal to the amount of physical DRAM minus the value in the TSEG register.

4.3.2. PCI Memory Address Range (Top of Main Memory to 4 GB)

The address range from the top of main DRAM to 4 GB (top of physical memory space supported by the GMCH2-M) is normally mapped via the hub interface to PCI. There are two exceptions to this rule:

Internal graphics configuration (GFX)

- Addresses decoded to the Local Memory Range are forwarded to the GFX
- Addresses decoded to the Memory Mapped Range of the internal graphics device (GFX) are forwarded to the GFX

AGP configuration

- Addresses decoded to the AGP Memory Window defined by the MBASE, MLIMIT, PMBASE, and PMLIMIT registers are mapped to AGP.
- Addresses decoded to the Graphics Aperture range defined by the APBASE and APSIZE registers are mapped to the main DRAM.

There are two sub-ranges within the PCI Memory address range defined as APIC Configuration Space and High BIOS Address Range. As an internal graphics device, the Local Memory Range and the Memory Mapped Range of the internal Graphics Device **MUST NOT** overlap with these two ranges. Similarly, as an AGP device, the AGP memory window and Graphics Aperture Window **MUST NOT** overlap with these two ranges. These ranges are described in detail in the following sections.

4.3.2.1. APIC Configuration Space (FEC0_0000h -FECF_FFFFh, FEE0_0000h-FEEF_FFFFh)

These ranges are reserved for APIC configuration space. The default Local APIC configuration space is FEE0_0000h to FEEF_FFFFh.

Processor accesses to the Local APIC configuration space do not result in external bus activity since the Local APIC configuration space is internal to the processor. However, a MTRR must be programmed to make the Local APIC range uncacheable (UC). The Local APIC base address in each processor should be relocated to the FEC0_0000h (4GB-20MB) to FECF_FFFFh range so that one MTRR can be programmed to 64 KB for the Local and I/O APICs. *The I/O APIC(s) usually reside in the I/O Bridge portion (ICH2-M) of the chip-set or as a stand-alone component(s).*

I/O APIC units will be located beginning at the default address FEC0_0000h. The first I/O APIC will be located at FEC0_0000h. Each I/O APIC unit is located at FEC0_x000h where *x* is I/O APIC unit number 0 through F(hex). This address range will be normally mapped via the hub interface to PCI.

Note: There is no provision to support an I/O APIC device on AGP.

The address range between the APIC configuration space and the High BIOS (FED0_0000h to FFDF_FFFFh) is always mapped via the hub interface to PCI.

4.3.2.2. High BIOS Area (FFE0_0000h -FFFF_FFFFh)

The top 2 MB of the Extended Memory Region is reserved for System BIOS (High BIOS), extended BIOS for PCI devices, and the A20 alias of the system BIOS. Processor begins execution from the High BIOS after reset. This region is mapped via the hub interface to PCI so that the upper subset of this region aliases to 16 MB-256 MB range. The actual address space required for the BIOS is less than 2 MB but the minimum processor MTRR range for this region is 2 MB so that full 2 MB must be considered. The ICH2-M supports a maximum of 1MB in the High BIOS range.

4.4. System Management Mode (SMM) Memory Range

The GMCH2-M supports the use of main memory as System Management RAM (SMRAM) enabling the use of System Management Mode (SMM). The GMCH2-M supports three SMM options:

- Compatible SMRAM (AB segment enabled)
- High Segment (HSEG)
- Top of Memory Segment (TSEG)

System Management RAM (SMRAM) space provides a memory area that is available for the SMI handler's and code and data storage. This memory resource is normally hidden from the operating system so that the processor has immediate access to this memory space upon entry to SMM. The GMCH2-M provides three SMRAM options:

- Below 1 MB option that supports compatible SMI handlers.
- Above 1 MB option that allows new SMI handlers to execute with write-back cacheable SMRAM.
- Optional larger write-back cacheable TSEG area of either 512 KB or 1MB in size above 1MB that is reserved from the highest area in system DRAM memory. The above 1MB solutions require changes to compatible SMRAM handlers code to properly execute above 1MB.

The hub interface and AGP masters are not allowed to access the SMM space. This must be insured even for the GTLB translation.

4.4.1. SMM Space Definition

SMM space has **addressed** SMM space and **DRAM** SMM space. The addressed SMM space is the range of bus addresses used by the processor to access SMM space. DRAM SMM space is the range of physical DRAM memory locations containing the SMM code.

SMM space can be accessed at one of three transaction address ranges: Compatible, HSEG and TSEG. The Compatible and TSEG SMM space is not remapped. Therefore the addressed and DRAM SMM space is the same address range. Since the HSEG SMM space is remapped, the addressed and DRAM SMM space is a different address range. Note that the HSEG DRAM space is the same as the Compatible Transaction Address space. Therefore the table below describes three unique address ranges:

- Compatible Transaction Address (Adr C)
- High Transaction Address (Adr H)
- TSEG Transaction Address (Adr T)

These abbreviations are used later in the table describing SMM Space Transaction Handling.

Table 11. SMM Space Abbreviations

SMM Space Enabled	Transaction Address Space (Adr)	DRAM Space (DRAM)
Compatible (C)	A_0000h to B_FFFFh	A_0000h to B_FFFFh
High (H)	0FEE_A0000h to 0FEE_BFFFFh	A_0000h to B_FFFFh
TSEG (T)	(TOM-TSEG_SZ) to TOM	(TOM-TSEG_SZ) to TOM

If the GMCH2-M is operating in internal graphics mode, a 512Kb or 1Mb window can optionally be used for the display frame buffer. This window is taken after the TSEG window.

4.4.2. SMM Space Restrictions

If any of the following conditions are violated the results of SMM accesses are unpredictable and may cause the system to hang:

- The Compatible SMM space must not be set-up as cacheable.
- HSEG or TSEG SMM transaction address space must not overlap address space assigned to system DRAM, the AGP aperture range, or to any “PCI” devices (including the hub interface and AGP devices). This is a BIOS responsibility.
- When TSEG SMM space is enabled, the TSEG space must not be reported to the OS as available DRAM. This is a BIOS responsibility.
- Any address translated through the AGP Aperture GTLB must not target DRAM from 000A_0000h to 000F_FFFFh.

4.4.3. SMM Space Combinations

When HSEG SMM is enabled, the Compatible SMM space must be disabled. Processor originated accesses to the Compatible SMM space are forwarded to AGP if VGAEN=1 (also depends on MDAP), otherwise they are forwarded to the hub interface. AGP and the hub interface originated accesses are **never** allowed to access SMM space. Only the processor is allowed to access SMM space. AGP and hub interface originated transactions are not allowed to SMM space.

4.4.4. Initialization and Usage of SMRAM and Graphics Local Memory

SMRAM Register Bits 7:4 control the usage of memory from Main Memory space for use as Graphics Local Memory and SMM TSEG memory. The blocks of memory selected by these fields are NOT accessible as general system RAM. When Bit 5 of the SMRAM register is a "1" the TSEG segment of memory can ONLY be accessed by the processor in SMM mode (No other agent can access this memory). Therefore, BIOS should initialize this block of memory BEFORE setting either Bit 5 or Bit 7 of the SMRAM register. The memory for TSEG is used first and then the Graphics Local Memory is used. An example of this memory usage mechanism is:

- TOM equal 64 MB,
- TSEG selected as 512 KB in size,
- Graphics Local Memory selected as 1 MB in size
- General System RAM available in system = 62.5 MB
  - General System RAM Range 00000000h to 03E7FFFFh
  - TSEG Address Range 03F80000h to 03FFFFFFh
  - TSEG used from 03F80000h to 03FFFFFFh
  - Graphics Local Memory used from 03E80000h to 03F7FFFFh

4.5. Memory Shadowing

Any block of memory that can be designated as read-only or write-only can be "shadowed" into GMCH2-M DRAM memory. Typically this is done to allow ROM code to execute more rapidly out of main DRAM. ROM is used as a read-only during the copy process while DRAM at the same time is designated write-only. After copying, the DRAM is designated read-only so that ROM is shadowed. processor bus transactions are routed accordingly.

4.6. I/O Address Space

The GMCH2-M does not support the existence of any other I/O devices other than itself on the processor bus. The GMCH2-M generates either hub interface or AGP/PCI (if enabled) bus cycles for all processor I/O accesses. If internal graphics is enabled, the GMCH2-M routes the access to hub interface or legacy I/O registers supported by the internal Graphics Device.

The GMCH2-M contains two internal registers in the processor I/O space, Configuration Address Register (CONFIG_ADDRESS) and the Configuration Data Register (CONFIG_DATA). These locations are used to implement PCI configuration space access mechanism and as described in chapter 3.

The I/O accesses, other than ones used for PCI configuration space access or ones that target the internal Graphics Device (GFX) (or AGP/PCI) are forwarded to the hub interface. The GMCH2-M will not post I/O write cycles to IDE. The PCICMD1 or PCICMD2 register can disable the routing of I/O cycles to the AGP. The GMCH2-M never responds to I/O cycles initiated on AGP.

4.6.1. AGP/PCI - I/O Address Mapping

The GMCH2-M can be programmed to direct non-memory (I/O) accesses to the AGP bus interface when processor initiated I/O cycle addresses are within the AGP I/O address range. This range is controlled via the I/O Base Address (IOBASE) and I/O Limit Address (IOLIMIT) registers in GMCH2-M Device #1 configuration space.

Address decoding for this range is based on the following concept. The top 4 bits of the respective I/O Base and I/O Limit registers correspond to address bits A[15:12] of an I/O address. For the purpose of address decoding, the GMCH2-M assumes that lower 12 address bits A[11:0] of the I/O base are zero and that address bits A[11:0] of the I/O limit address are FFFh. This forces the I/O address range alignment to 4KB boundary and produces a size granularity of 4KB. The GMCH2-M positively decodes I/O accesses to AGP I/O address space as defined by the following equation:

I/O_Base_Address ≤ processor I/O Cycle Address ≤ I/O_Limit_Address

The plug-and-play configuration software programs the effective size of the range and it depends on the size of I/O space claimed by the AGP device.

The GMCH2-M also forwards accesses to the Legacy VGA I/O ranges according to the settings of Device #1 configuration registers BCTRL (VGA Enable) and PCICMD1 (IOAE1), unless a second adapter (monochrome) is present on the hub interface/PCI (or ISA). The MDAP configuration bit determines the presence of a second graphics adapter. When MDAP is set, the MCH will decode legacy monochrome IO ranges and forward them to the hub interface. The IO ranges decoded for the monochrome adapter are 3B4h, 3B5h, 3B8h, 3B9h, 3Bah and 3BFh. The PCICMD1 register can disable the routing of I/O cycles to the AGP.

Note that the GMCH2-M Device #1 I/O address range registers defined above are used for all I/O space allocation for any devices requiring such a window on AGP. These devices would include the AGP device, PCI-66MHz/3.3V agents, and multifunctional AGP devices where one or more functions are implemented as PCI devices.

4.7. GMCH2-M Address Decode Rules and Cross-Bridge Address Mapping

The GMCH2-M's address map applies globally to accesses arriving on any of the three interfaces (i.e., Host bus, hub interface or from the internal Graphics Device).

4.7.1. Address Decode Rules

The GMCH2-M accepts all memory Read and Write accesses from the hub interface to both System Memory and Graphics Memory. The hub interface accesses that fall elsewhere within the PCI memory range will not be accepted. The GMCH2-M never responds to hub interface initiated I/O read or write cycles.

The GMCH2-M accepts accesses from the hub interface to the following address ranges:

- All memory Read/Write accesses to Main DRAM including PAM region (except SMM space)
- All memory Read/Write accesses to the Graphics Aperture defined by APBASE and APSIZE.
- All Hub interface memory write accesses to AGP memory range defined by MBASE, MLIMIT, PMBASE, and PMLIMIT.
- Memory writes to VGA range on AGP if enabled.

The hub interface memory accesses that fall elsewhere within the memory range are considered invalid and will be remapped to a translated memory address, snooped on the host bus, and dispatched to DRAM. Reads will return all 1's with Master Abort completion. Writes will have BE's deasserted and will terminate with Master Abort if completion is required. I/O cycles will not be accepted. They are terminated with Master Abort completion packets.

4.7.2. The Hub Interface Accesses to GMCH2-M that Cross Device Boundaries

The Hub interface accesses are limited to 256 bytes but have no restrictions on crossing address boundaries. A single hub interface request may therefore span device boundaries (AGP, DRAM) or cross from valid addresses to invalid addresses (or visa versa). The GMCH2-M does not support transactions that cross device boundaries. For reads and for writes requiring completion, the GMCH2-M will provide separate completion status for each naturally-aligned 32 or 64 byte block. If the starting address of a transaction hits a valid address the portion of a request that hits that target device (AGP or DRAM) will complete normally.

The remaining portion of the access that crosses a device boundary (targets a different device than that of the starting address) or hits an invalid address will be remapped to memory address 0h, snooped on the host bus, and dispatched to DRAM. Reads will return all 1's with Master Abort completion. Writes will have BE's deasserted and will terminate with Master Abort if completion is required.

If the starting address of a transaction hits a invalid address the entire transaction will be remapped to memory address 0h, snooped on the host bus, and dispatched to DRAM. Reads will return all 1's with Master Abort completion. Writes will have BE's deasserted and will terminate with Master Abort if completion is required.

4.7.3. AGP Interface Decode Rules

4.7.3.1. Cycles Initiated Using PCI Protocol

The GMCH2-M does not support any AGP/PCI access targeting the hub interface. The GMCH2-M will claim AGP/PCI initiated memory read and write transactions decoded to the main DRAM range or the Graphics Aperture range. All other memory read and write requests will be master-aborted by the AGP/PCI initiator as a consequence of GMCH2-M not responding to a transaction.

Under certain conditions, the GMCH2-M restricts access to the DOS Compatibility ranges governed by the PAM registers by distinguishing access type and destination bus. The GMCH2-M accepts AGP/PCI write transactions to the compatibility ranges if the PAM designates DRAM as write-able. If accesses to a range are not write enabled by the PAM, the GMCH2-M does not respond and the cycle will result in a master-abort. AGP/PCI read transactions to the compatibility ranges are accepted if the PAM designates DRAM as readable. If accesses to a range are not read enabled by the PAM, the GMCH2-M does not respond and the cycle will result in a master-abort.

If agent on AGP/PCI issues an I/O or PCI Special Cycle transaction, the GMCH2-M will not respond and cycle will result in a master-abort. The GMCH2-M will not accept PCI configuration cycles to the internal GMCH2-M devices.

4.7.3.2. Cycles Initiated Using AGP Protocol

All cycles must reference main memory i.e. main DRAM address range (*excluding* PAM) or Graphics Aperture range (also physically mapped within DRAM but using different address range). AGP accesses to the PAM region from 640K -to- 1MB are not allowed. AGP accesses to SMM space are not allowed. AGP initiated cycles that target DRAM are not snooped on the host bus, even if they fall outside of the AGP aperture range.

If a cycle is outside of a valid main memory range then it will terminate as follows:

Reads: Remap to memory address 0h, return data from address 0h, and set the IAAF error flag.

Writes: Remapped to memory address 0h with BE's deasserted (effectively dropped "on the floor") and set the IAAF error flag.

4.7.3.3. AGP Accesses to GMCH2-M that Cross Device Boundaries

For FRAME# accesses, when an AGP or PCI master gets disconnected it will resume at the new address which allows the cycle to be routed to or claimed by the new target. Therefore, accesses should be disconnected by the target on potential device boundaries. The GMCH2-M will disconnect AGP/PCI transactions on 4KB boundaries.

AGP PIPE# and SBA accesses are limited to 256 bytes and must hit DRAM. AGP accesses are dispatched to DRAM on naturally aligned 32 byte block boundaries. The portion of the request that hits a valid address will complete normally. The portion of a read access that hits an invalid address will be remapped to address 0h, return data from address 0h, and set the IAAF error flag. The portion of a write access that hits an invalid address will be remapped to memory address 0h with BE's deasserted (effectively dropped "on the floor") and set the IAAF error flag.

4.7.4. Legacy VGA Ranges

The legacy VGA memory range A_0000h-B_FFFFh is mapped either to the hub interface or to AGP/PCI1 depending on the programming of the VGA Enable bit in the BCTRL configuration register in GMCH2-M Device #1 configuration space, and the MDAP bit in the GMCH2-MCFG configuration register in Device #0 configuration space. The same register controls mapping VGA I/O address ranges. VGA I/O range is defined as addresses where A[9:0] are in the ranges 3B0h to 3BBh and 3C0h to 3DFh (inclusive of ISA address aliases - A[15:10] are not decoded). The function and interaction of these two bits is described below:

MDA Present (MDAP): This bit works with the VGA Enable bit in the BCTRL register of device 1 to control the routing of processor initiated transactions targeting MDA compatible I/O and memory address ranges. This bit should not be set when the VGA Enable bit is not set. If the VGA enable bit is set, then accesses to IO address range x3BCh-x3BFh are forwarded to the hub interface. If the VGA enable bit is not set, then IO address range accesses x3BCh-x3BFh are treated like other IO accesses - the cycles are forwarded to AGP if the address is within IOBASE and IOLIMIT and ISA enable bit is not set, otherwise they are forwarded to the hub interface. MDA resources are defined as the following:

- Memory: 0B0000h - 0B7FFFh
- I/O: 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh,

Note: Including ISA address aliases, A[15:10] are not used in decode.

Any I/O reference that includes the I/O locations listed above, or their aliases, will be forwarded to the hub interface even if the reference includes I/O locations not listed above.

VGA Enable: Controls the routing of processor initiated transactions targeting VGA compatible I/O and memory address ranges. When this bit is set, GMCH2-M will forward the following processor accesses to the AGP:

- Memory accesses in the range 0A0000h to 0BFFFFh
- I/O addresses where A[9:0] are in the ranges 3B0h to 3BBh and 3C0h to 3DFh

Note: Inclusive of ISA address aliases - A[15:10] are not decoded.

When this bit is set, forwarding of these accesses issued by the processor is independent of the I/O address and memory address ranges defined by the previously defined base and limit registers. Forwarding of these accesses is also independent of the settings of the bit 2 (ISA Enable) of BCTRL if this bit is “1”. If the VGA enable bit is set, then accesses to IO address range x3BCh-x3BFh are forwarded to the hub interface. If the VGA enable bit is not set, then IO address range accesses x3BCh-x3BFh are treated like other IO accesses - the cycles are forwarded to AGP if the address is within IOBASE and IOLIMIT and ISA enable bit is not set, otherwise they are forwarded to the hub interface.

If this bit is “0” (default) , then VGA compatible memory and I/O range accesses are not forwarded to AGP but rather they are mapped to the hub interface unless they are mapped to AGP via I/O and memory range registers defined above (IOBASE, IOLIMIT, MBASE, MLIMIT, PMBASE, PMLIMIT

4.8. Host Interface

The host interface of the GMCH2-M is optimized to support the mobile Intel® Pentium® III processor, Intel® Pentium® II processor, and Intel® Celeron™ processor. The GMCH2-M implements the host address, control, and data bus interfaces within a single device. The GMCH2-M supports a 4-deep in-order queue (i.e., supports pipelining of up to 4 outstanding transaction requests on the host bus). Host bus addresses are decoded by the GMCH2-M for accesses to system memory, PCI memory & PCI I/O (via hub interface), PCI configuration space and Graphics memory. The GMCH2-M takes advantage of the pipelined addressing capability of the processor to improve the overall system performance.

4.8.1. Host Bus Device Support

The GMCH2-M supports a large subset of the transaction types that are defined for the Intel® Pentium® III processor, Intel® Pentium® II processor, or Intel® Celeron™ processor bus interface. However, each of these transaction types has a multitude of response types, some of which are not supported by this controller. All transactions are processed in the order that they are received on the processor bus.

Table 12. Summay of Transactions Supported By GMCH2-M

Transaction	REQa[4:0]#	REQb[4:0]#	GMCH2-M Support
Deferred Reply	0 0 0 0 0	X X X X X	The GMCH2-M will initiate a deferred reply request for a previously deferred transaction.
Reserved	0 0 0 0 1	X X X X X	Reserved
Interrupt Acknowledge	0 1 0 0 0	0 0 0 0 0	Interrupt acknowledge cycles are forwarded to the hub interface.
Special Transactions	0 1 0 0 0	0 0 0 0 1	See separate table in special cycles section.
Reserved	0 1 0 0 0	0 0 0 1 x	Reserved
Reserved	0 1 0 0 0	0 0 1 x x	Reserved
Branch Trace Message	0 1 0 0 1	0 0 0 0 0	The GMCH2-M will terminate a branch trace message without latching data.
Reserved	0 1 0 0 1	0 0 0 0 1	Reserved
Reserved	0 1 0 0 1	0 0 0 1 x	Reserved
Reserved	0 1 0 0 1	0 0 1 x x	Reserved
I/O Read	1 0 0 0 0	0 0 x LEN#	I/O read cycles are forwarded to hub interface. I/O cycles which are in the GMCH2-M configuration space will not be forwarded to the hub interface.
I/O Write	1 0 0 0 1	0 0 x LEN#	I/O write cycles are forwarded to hub interface. I/O cycles which are in the GMCH2-M configuration space will not be forwarded to hub interface.
Reserved	1 1 0 0 x	0 0 x x x	Reserved
Memory Read & Invalidate	0 0 0 1 0	0 0 x LEN#	Host initiated memory read cycles are forwarded to DRAM or the hub interface.
Reserved	0 0 0 1 1	0 0 x LEN#	Reserved

Transaction	REQa[4:0]#	REQb[4:0]#	GMCH2-M Support
Memory Code Read	0 0 1 0 0	0 0 x LEN#	Memory code read cycles are forwarded to DRAM or hub interface.
Memory Data Read	0 0 1 1 0	0 0 x LEN#	Host initiated memory read cycles are forwarded to DRAM or the hub interface.
Memory Write (no retry)	0 0 1 0 1	0 0 x LEN#	This memory write is a writeback cycle and cannot be retried. The GMCH2-M will forward the write to DRAM.
Memory Write (can be retried)	0 0 1 1 1	0 0 x LEN#	The standard memory write cycle will be forwarded to DRAM or hub interface.

For Memory cycles, REQa[4:3]# = ASZ#. GMCH2-M only supports ASZ# = 00 (32 bit address).

REQb[4:3]# = DSZ#. DSZ# = 00 (64 bit data bus size).

LEN# = data transfer length as follows:

LEN#	Data length
00	<= 8 bytes (BE[7:0]# specify granularity)
01	Length = 16 bytes BE[7:0]# all active
10	Length = 32 bytes BE[7:0]# all active
11	Reserved

Table 13. Host Responses Supported by the GMCH2-M

RS2#	RS1#	RS0#	Description	GMCH2-M Support
0	0	0	idle	
0	0	1	Retry Response	This response is generated if an access is to a resource that cannot be accessed by the processor at this time and the logic must avoid deadlock. Hub interface directed reads, writes, and DRAM locked reads can be retried.
0	1	0	Deferred Response	This response can be returned for all transactions that can be executed 'out of order.' Hub interface directed reads (memory, I/O and Interrupt Acknowledge) and writes (I/O only), and internal Graphics device directed reads (memory and I/O) and writes (I/O only) can be deferred.
0	1	1	Reserved	Reserved
1	0	0	Hard Failure	Not supported.
1	0	1	No Data Response	This is for transactions where the data has already been transferred or for transactions where no data is transferred. Writes and zero length reads receive this response.
1	1	0	Implicit Writeback	This response is given for those transactions where the initial transactions snoop hits on a modified cache line.
1	1	1	Normal Data Response	This response is for transactions where data accompanies the response phase. Reads receive this response.

4.8.2. Special Cycles

A Special Cycle is defined when REQa [4:0] = 01000 and REQb [4:0]= xx001. The first address phase Aa [35:3]# is undefined and can be driven to any value. The second address phase, Ab [15:8]# defines the type of Special Cycle issued by the processor.

The following table specifies the cycle type and definition, as well as the action taken by the GMCH2-M when the corresponding cycles are identified.

Table 14. Special Cycles

BE[7:0}#	Special Cycle Type	Action Taken
0000 0000	NOP	This transaction has no side-effects.
0000 0001	Shutdown	This transaction is issued when an agent detects a severe software error that prevents further processing. This cycle is claimed by the GMCH2-M. The GMCH2-M issues a shutdown special cycle on the hub interface. This cycle is retried on the processor bus after it is terminated on the hub interface via a master abort mechanism.
0000 0010	Flush	This transaction is issued when an agent has invalidated its internal caches without writing back any modified lines. The GMCH2-M claims this cycle and retries it.
0000 0011	Halt	This transaction is issued when an agent executes a HLT instruction and stops program execution. This cycle is claimed by the GMCH2-M and propagated to the hub interface as a Special Halt Cycle. This cycle is retried on the processor bus after it is terminated on the hub interface via a master abort mechanism.
0000 0100	Sync	This transaction is issued when an agent has written back all modified lines and has invalidated its internal caches. The GMCH2-M claims this cycle and retries it.
0000 0101	Flush Acknowledge	This transaction is issued when an agent has completed a cache sync and flush operation in response to an earlier FLUSH# signal assertion. The GMCH2-M claims this cycle and retires it.
0000 0110	Stop Clock Acknowledge	This transaction is issued when an agent enters Stop Clock mode. This cycle is claimed by the GMCH2-M and propagated to the hub interface as a Special Stop Grant Cycle. This cycle is completed on the processor bus after it is terminated on the hub interface via a master abort mechanism.
0000 0111	SMI Acknowledge	This transaction is first issued when an agent enters the System Management Mode (SMM). Ab[7]# is also set at this entry point. All subsequent transactions from the processor with Ab[7]# set are treated by the GMCH2-M as accesses to the SMM space. No corresponding cycle is propagated to the hub interface. To exit the System Management Mode the processor issues another one of these cycles with the Ab[7]# bit deasserted. The SMM space access is closed by the GMCH2-M at this point.
all others	Reserved	

4.9. System Memory DRAM Interface

The GMCH2-M integrates a system DRAM controller that supports a 64-bit DRAM array. The DRAM type supported is Synchronous (SDRAM). The GMCH2-M generates the SCSA#, SCSB#, SDQM, SCAS#, SRAS#, SWE# and multiplexed addresses, SMA for the DRAM array. The GMCH2-M's DRAM interface operates at a clock frequency of 100MHz, dependent upon the system bus interface clock frequency. The DRAM controller interface is fully configurable through a set of control registers. Complete descriptions of these registers are given in the register description section of this document.

The GMCH2-M supports industry standard 64-bit wide SO-DIMM modules with SDRAM devices. The 2 bank select lines SBS[1:0], the 12 Address lines SMAA[11:0], and copies of 4 Address lines SMAB[7:4]# and SMAC[7:4]# allow the GMCH2-M to support 64 bit wide SO-DIMMs using 16Mb, 64Mb, 128Mb or 256Mb technology SDRAMs. The GMCH2-M has a sufficient amount of SCS# lines to enable the support of up to six 64-bit rows of DRAM. For write operations of less than a Qword in size, the GMCH2-M will perform a byte-wise write. The GMCH2-M targets SDRAM with CL2 and CL3 and supports both single and double-sided SO-DIMMs. The GMCH2-M provides refresh functionality with programmable rate (normal DRAM rate is 1 refresh/15.6 µs). The GMCH2-M can be configured via the Page Closing Policy Bit in the GMCH2-M Configuration Register to keep multiple pages open within the memory array. Pages can be kept open in any one row of memory. Up to 4 pages can be kept open within that row (The GMCH2-M only supports 4 Bank SDRAMs on system DRAM interface).

4.9.1. DRAM Organization and Configuration

The GMCH2-M supports 64-bit SDRAM configurations. In the following discussion the term row refers to a set of memory devices that are simultaneously selected by a SCS# signal. The GMCH2-M will support a maximum of 6 rows of memory.

The interface consists of the following pins:

Multiple copies: SMAA[7:4], SMAB[7:4]# , SMAC[7:4]#

Single Copies: SMD[63:0]

SDQM[7:0]

SMAA[12:8,3:0]

SBS[1:0]

SCSA[5:0]#

SCSB[5:0]#

SCAS#

SRAS#

SWE#

SCKE[5:0]

The GMCH2-M supports SO-DIMMs with 16 bit wide SDRAM devices. Registered DIMMs or DIMMs populated with 4 bit wide SDRAM devices are not supported. The GMCH2-M supports 3.3v standard SDRAMs.

4.9.1.1. Configuration Mechanism SO-DIMMs

Detection of the type of DRAM installed on the SO-DIMM is supported via Serial Presence Detect mechanism as defined in the JEDEC 168-pin DIMM standard and 144-pin SO-DIMM standard. This standard uses the SCL, SDA and SA[2:0] pins on the SO-DIMMs to detect the type and size of the installed SO-DIMMs. No special programmable modes are provided on the GMCH2-M for detecting the size and type of memory installed. Type and size detection must be done via the serial presence detection pins. Use of Serial Presence Detection is required.

Memory Detection and Initialization

Before any cycles to the memory interface can be supported, the GMCH2-M DRAM registers must be initialized. The GMCH2-M must be configured for operation with the installed memory types. Detection of memory type and size is done via the System Management Bus (SMBus) interface on the ICH2-M. This two wire bus is used to extract the DRAM type and size information from the serial presence detect port on the DRAM SO-DIMM modules.

4.9.1.2. DRAM Register Programming

This section provides an overview of how the required information for programming the DRAM registers is obtained from the Serial Presence Detect ports on the SO-DIMMs. The Serial Presence Detect ports are used to determine Refresh Rate, MA and MD Buffer Strength, Row Type (on a row by row basis), SDRAM Timings, Row Sizes and Row Page Sizes.

The following Table 5-6 lists a subset of the data available through the on-board Serial Presence Detect ROM on each SO-DIMM module.

Table 15. Data Bytes on DIMM Used for Programming DRAM Registers

Byte	Function
2	Memory Type (EDO, SDRAM) the GMCH2-M only supports SDRAM.
3	# of Row Addresses, not counting Bank Addresses
4	# of Column Addresses
5	# of banks of DRAM (Single or Double sided) DIMM
12	Refresh Rate
17	# Banks on each SDRAM Device
36-41	Access Time from Clock for CAS# Latency 1 through 7
42	Data Width of SDRAM Components

These bytes collectively provide enough data for BIOS to program the GMCH2-M DRAM registers.

4.9.2. DRAM Address Translation and Decoding

The GMCH2-M contains address decoders that translate the address received on the host bus, hub interface, or from the internal Graphics device to an effective memory address. The GMCH2-M supports 16 and 64 Mbit SDRAM devices. The GMCH2-M supports a 2 KB page sizes only. The multiplexed row / column address to the DRAM memory array is provided by the SBS[1:0] and SMAA[11:0] signals and copies. These addresses are derived from the host address bus as defined by the following table for SDRAM devices. Row size is internally computed using the values programmed in the DRP register. Up to 4 pages can be open at any time within any row (Only 2 active pages are supported in rows populated with either 8 MBs or 16 MBs).

Table 16. GMCH2-M DRAM Address Mux Function

Tech (Mb)	Depth	Width	Address Usage			MemSize (MB)	BS 1	BS 0	MA 12	MA 11	MA 10	MA 9	MA 8	MA 7	MA 6	MA 5	MA 4	MA 3	MA 2	MA 1	MA 0
			Row	Col	Bank																
16	2M	8	11	9	1	16	X	11	X	X	[A]	22	21	20	19	18	17	16	15	14	13
							X	11	X	X	PA	X	23	10	9	8	7	6	5	4	3
64	8M	8	12	9	2	64	12	11	X	24	[A]	22	21	20	19	18	17	16	15	14	13
							12	11	X	X	PA	X	25	10	9	8	7	6	5	4	3
64	4M	16	12	8	2	32	12	11	X	24	[A]	22	21	20	19	18	17	16	15	14	13
							12	11	X	X	PA	X	X	10	9	8	7	6	5	4	3
128	16M	8	12	10	2	128	12	11	X	24	[A]	22	21	20	19	18	17	16	15	14	13
							12	11	X	X	PA	26	25	10	9	8	7	6	5	4	3
128	8M	16	12	9	2	64	12	11	X	24	[A]	22	21	20	19	18	17	16	15	14	13
							12	11	X	X	PA	X	25	10	9	8	7	6	5	4	3
256	32M	8	13	10	2	256	12	11	27	24	[A]	22	21	20	19	18	17	16	15	14	13
							12	11	X	X	PA	26	25	10	9	8	7	6	5	4	3
256	16M	16	13	9	2	128	12	11	26	24	[A]	22	21	20	19	18	17	16	15	14	13
							12	11	X	X	PA	X	25	10	9	8	7	6	5	4	3

NOTES: MA bit 10 at RAS time uses the XOR of Address bit 12 and Address bit 23

4.9.3. SDRAMT Register Programming

Several DRAM timing parameters are programmable in the GMCH2-M configuration registers. Table 18 summarizes the programmable parameters.

Table 17. Programmable SDRAM Timing Parameters

Parameter	DRAMT Bit	Values (SCLKs)
RAS# Precharge (SRP)	0	2,3
RAS# to CAS# Delay (SRCD)	1	2,3
CAS# Latency (CL)	2	2,3
DRAM Cycle Time (DCT)	4	Tras = 5,6 Trc = 7,8

These parameters are controlled via the DRAMT register. In order to support different device speed grades, CAS# Latency, RAS# to CAS# Delay, and RAS# Precharge are all programmable as either two or three SCLKs. To provide flexibility, these are each controlled by separate register bits. That is, the GMCH2-M can support any combination of CAS# Latency, RAS# to CAS# Delay and RAS# Precharge.

4.9.4. SDRAM Paging Policy

The GMCH2-M can maintain up to 4 active pages in any one row; however, the GMCH2-M does not support active pages in more than 1 row at a time.

The DRAM page closing policy (DPCP) in the GMCH2-M configuration register (GMCHCFG) controls the page closing policy of the. This bit controls whether the GMCH2-M will precharge bank or precharge all during the service of a page miss. When this bit is set to 0, the GMCH2-M will prechange bank during the service of a page miss. When this bit is set to 1, the GMCH2-M will prechange all during the service of a page miss.

4.10. Intel® Dynamic Video Memory Technology (D.V.M.T.)

The internal graphics device on the GMCH2-M supports Intel® Dynamic Video Memory Technology (D.V.M.T.). Intel® D.V.M.T. dynamically responds to application requirements by allocating the proper amount of display and texturing memory. For more details please refer to the document entitled, “Intel® 810 chipset: Great Performance for Value PCs” available at: http://deverlolper.intel.com/design/ chipsets/ 810/810white.htm.

In addition to Intel® D.V.M.T., the GMCH2-M supports Display Cache (DC). The graphics engine of the GMCH2-M uses DC for implementing rendering buffers (e.g., Z buffers). This rendering model requires 4 MB of display cache and allows graphics rendering (performed across the graphics display cache bus) and texture MIP map access (performed across the system memory bus) simultaneously. In using Intel® D.V.M.T., all graphics rendering is implemented in system memory. The system memory bus is arbitrated between texture MIP-map accesses and rendering functions.

4.11. Display Cache Interface

The GMCH2-M Display Cache (DC) is a single channel 32 bit wide SDRAM interface. The GMCH2-M handles the control and timing for the display cache. The display cache interface of the GMCH2-M generates the LCS#, LDQM[7:0], LSCAS#, LSRAS#, LWE#, LMD[31:0] and multiplexed addresses, LMA[11:0] for the display cache DRAM array. The GMCH2-M also generates the clock LTCLK[1:0] for write cycles as well as LOCLK for read cycle timings.

The display cache interface of the GMCH2-M supports single data rate synchronous dynamic random access memory (SDRAM). It supports a single 32-bit wide memory channel. The interface handles the operation of D.V.M. with DC at 100/133MHz. The DRAM controller interface is fully configurable through a set of control registers.

Internal buffering (FIFOs) of the data to and from the display cache ensures the synchronization of the data to the internal pipelines. The D.V.M. with DC interface clocking is divided synchronous with respect to the core and system bus.

The startup sequencing for the local memory display cache, is as follows:

- System BIOS detects if an external AGP device is present by doing a config read to PCI. If an AGP device is present, it becomes the display device and bit 0 of the APCONT register should be set to 0. No further initialization of internal graphics will take place. If internal graphics is the preferred display device, bit 0 of the APCONT register should be set to 1. If no AGP device is present, the internal graphics becomes the display device and bit 0 of the APCONT register should be set to 1. PCI enumeration takes place at this point.

In the case where internal graphics is selected, the remaining steps still apply:

- System BIOS determines if local memory display cache is present. If present the following steps take place:
  - Local Memory Clock Frequency is determined with a reset strap (on AGP pin SBA[7]) sampled as an input during reset.
  - Memory Timing Options will be determined empirically by the system BIOS. The BIOS will start with programming slow timings (CAS Latency, RAS Pre-charge, etc.) and then trying faster timings until it breaks. The settings, which optimize performance without compromising functionality, will be selected.

4.11.1. Supported DRAM Types for Display Cache Memory

1Mx16 and 2Mx32 SDRAMs are supported, but the maximum memory supported is 4MB of display cache memory.

4.11.2. Memory Configurations

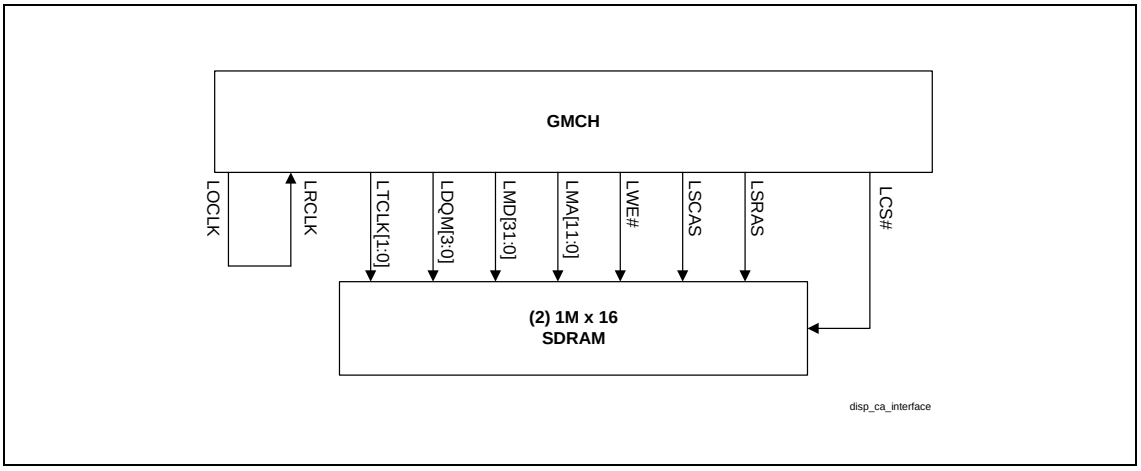
The following table gives a summary of the characteristics of memory configurations supported. The GMCH2-M supports a 32-bit wide channel populated with a single row of 1Mx16 SDRAMs.

Table 18. Memory Size for each configuration:

SDRAM	SDRAM	SDRAM	# of	Address Size			DRAM	DRAM Size
Tech.	Density	Width	Banks	Bank	Row	Column	Addressing	
16 Mbit	1M	16	2	1	11	8	Asymmetric	4MB
16 Mbit	1M	32						

The following figure shows the GMCH LMI connected to 4 MB of memory in a 32-bit SDRAM channel configuration.

Figure 6. MCH2-M Display Cache Interface to 4MB



4.11.3. Address Translation

The GMCH2-M contains address decoders that translate the address received by the display cache into an effective display cache address. The LMA[11:0] bits are as defined in the following table. Entries in the table (e.g., A21(X)) imply that the GMCH2-M puts out A21 on that MA line but it is not used by the SDRAM.

Table 19, GMCH2-M Local Memory Address Mapping

MA	1Mx16	
	Row	Column
11(BA)	A10	A10
10	A11	X
9	A21	X
8	A20	X
7	A19	A9
6	A18	A8
5	A17	A7
4	A16	A6
3	A15	A5
2	A14	A4
1	A13	A3
0	A12	A2

NOTES: BA = Bank address

4.11.4. Display Cache Interface Timing

The GMCH2-M provides a variety of programmable wait states for DRAM read and write cycles. These options are programmed in the display cache I/O addresses of the GMCH2-M configuration space. The wrap type and the burst length is implied since they are not programmable and fixed. Only sequential wrap is allowed. Burst length is fixed at two.

4.12. Internal Graphics Device

4.12.1. 3D/2D Instruction Processing

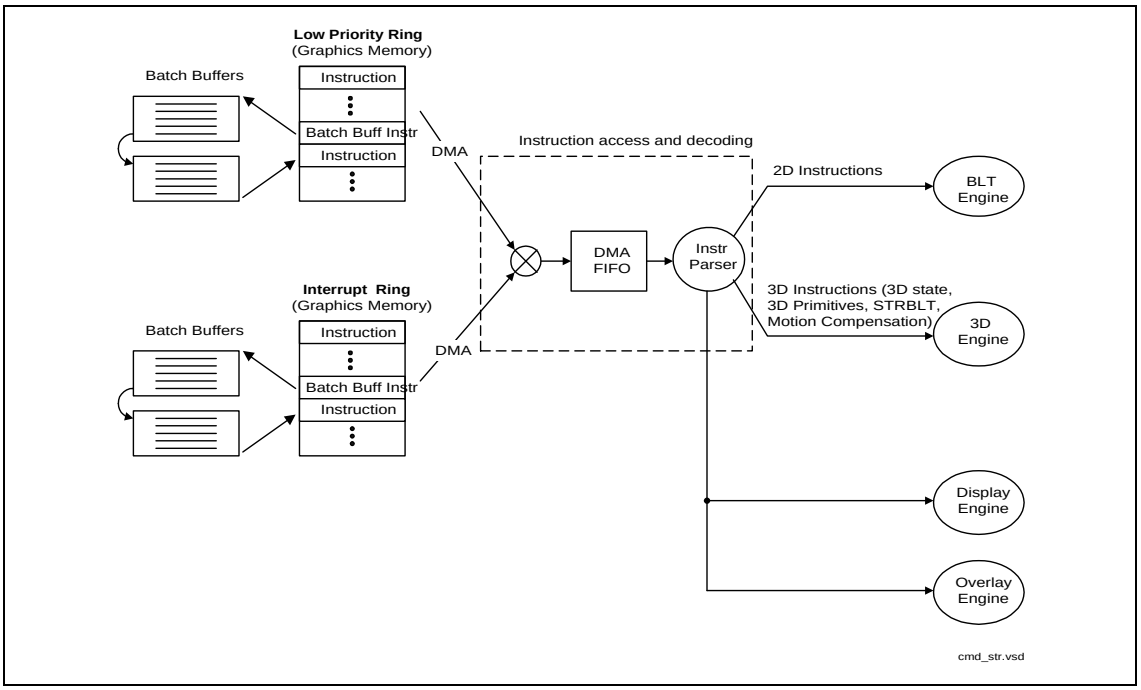
The GMCH2-M contains an extensive set of instructions that controls various functions including 3D rendering, BLT and STRBLT operations, display, motion compensation, and overlay. The 3D instructions set 3D pipeline states and control the processing functions. The 2D instructions provide an efficient method for invoking BLT and STRBLT operations.

The graphics controller executes instructions from one of two instruction buffers located in system memory: Interrupt Ring or Low Priority Ring. Instead of writing instructions directly to the GMCH2-M's graphics controller, software sets up instruction packets in these memory buffers and then instructs the GMCH2-M to process the buffers. The GMCH2-M uses DMAs to put the instructions into its FIFO and executes them. Instruction flow in the ring buffer instruction stream can make calls to other buffers, much like a software program makes subroutine calls. Flexibility has been built into the ring operation permitting software to efficiently maintain a steady flow of instructions.

Batching instructions in memory ahead of time and then instructing the graphics controller to process the instructions provides significant performance advantages over writing directly to FIFOs including:

1) Reduced software overhead, 2) Efficient DMA instruction fetches from graphics memory, and 3) Software can more efficiently set up instruction packets in buffers in graphics memory (faster than writing to FIFOs).

Figure 7. 3D/2D Pipeline Preprocessor



4.12.2. 3D Engine

The 3D engine of the GMCH2-M has been architected as a deep pipeline, where performance is maximized by allowing each stage of the pipeline to simultaneously operate on different primitives or portions of the same primitive. The internal graphics device of the GMCH2-M supports perspective-correct texture mapping, bilinear, trilinear, and anisotropic MIP map filtering, Gouraud shading, alpha-blending, colorkeying and chromakeying, full color specular shading, fogging and Z Buffering. These features can be independently enabled or disabled via set of 3D instructions. In addition, the GMCH2-M supports a Dynamic Video Memory Technology (D.V.M.T.) which allows the entire 3D rendering process to take place in system memory; thus, alleviating the need for the display cache.

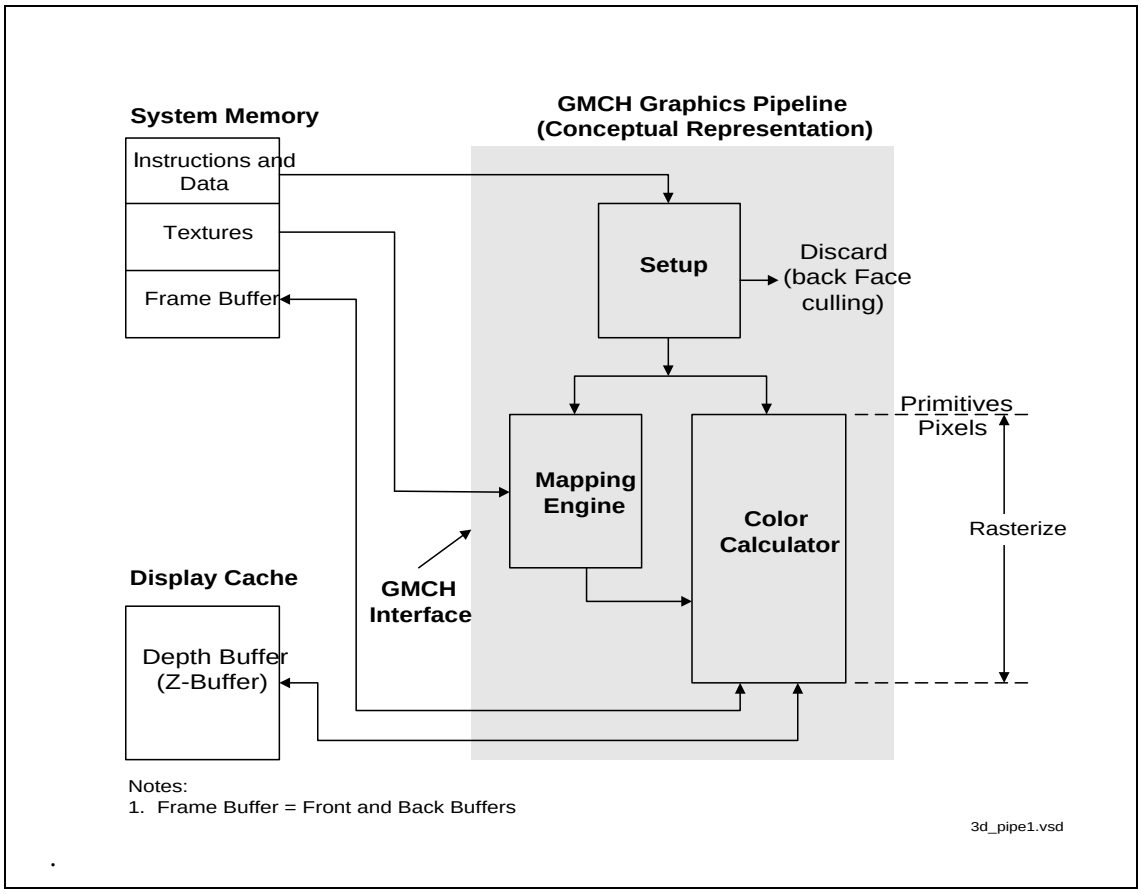
The main blocks of the pipeline are the Setup Engine, Scan Converter, Texture Pipeline, and Color Calculator block. A typical programming sequence would be to send instructions to set the state of the pipeline followed by rendering instructions containing 3D primitive vertex data.

4.12.3. Buffers

The 2D, 3D and video capabilities of the internal graphics device of the GMCH2-M provide control over a variety of graphics buffers which can be implemented either in display cache or system memory. To aid the rendering process, the display cache of the GMCH2-M contains two hardware buffers—the Front Buffer (display buffer) and the Back Buffer (rendering buffer). The image being drawn is not visible until the scene is complete and the back buffer made visible (via an instruction) or copied to the front buffer (via a 2D BLT operation). By rendering to one and displaying from the other, the possibility of image tearing is removed. This also speeds up the display process over a single buffer.

The 3D pipeline of the GMCH2-M operates on the Back Buffer and the Z Buffer. The pixels' 16-bit (or 15-bit) RGB colors are stored in the back buffer. The Z-buffer can be used to store 16-bit depth values or 5-bit "destination alpha" values. The Instruction set of the GMCH2-M provides a variety of controls for the buffers (e.g., initializing, flip, clear, etc.).

Figure 8. Data Flow for the 3D Pipeline



4.12.4. Setup

The setup stage of the pipeline takes the input data associated with each vertex of the line or triangle primitive and computes the various parameters required for scan conversion. In formatting this data, the GMCH2-M maintains sub-pixel accuracy. Data is dynamically formatted for each rendered polygon and output to the proper processing unit. As part of the setup, the GMCH2-M removes polygons from further processing, if they are not facing the user's viewpoint (referred to as " Back Face Culling").

4.12.5. Texturing

The internal graphics device of the GMCH2-M allows an image, pattern, or video to be placed on the surface of a 3D polygon. Textures must be located in system memory. Being able to use textures directly from system memory means that large complex textures can easily be handled without the limitations imposed by the traditional approach of only using the display cache.

The texture processor receives the texture coordinate information from the setup engine and the texture blend information from the scan converter. The texture processor performs texture color or chroma-key matching, texture filtering (anisotropic, bilinear, and trilinear interpolation), and YUV to RGB conversions.

The GMCH2-M supports up to 11 Levels-of-Detail (LODs) ranging in size from 1024x1024 to 1x1 texels. (A texel is defined as a texture map pixel). Textures need not be square. Included in the texture processor is a small cache, which provides efficient mip-mapping.

- **Nearest.** Texel with coordinates nearest to the desired pixel is used. (This is used if only one LOD is present).
- **Linear.** A weighted average of a 2x2 area of texels surrounding the desired pixel are used. (This is used if only one LOD is present).
- **Mip Nearest.** This is used if many LODs are present. The appropriate LOD is chosen and the texel with coordinates nearest to the desired pixel are used.
- **Mip Linear.** This is used if many LODs are present. The appropriate LOD is chosen and a weighted average of a 2x2 area of texels surrounding the desired pixel are used. This is also referred to as bi-linear mip-mapping.
- **Trilinear.** Tri-linear filtering blends two mip maps of the same image to provide a smooth transition between different mips (floor and ceiling of the calculated LOD).
- **Anisotropic.** This can be used if multiple LODs are present. This filtering method improves the visual quality of texture-mapped objects when viewed at oblique angles (i.e., with a high degree of perspective foreshortening). The improvement comes from a more accurate (anisotropic) mapping of screen pixels onto texels -- where using bilinear or trilinear filtering can yield overly-blurred results. Situations where anisotropic filtering demonstrates superior quality include text viewed at an angle, lines on roadways, etc.

The GMCH2-M can store each of the above mip-maps in any of the following formats:

- 8bpt Surface Format
- 16bpt Surface Format
  - RGB 565
  - ARGB 1555
  - ARGB 4444
  - AY 88
- 8bpt (Indexed) Surface Format
  - RGB 565
  - ARGB 1555
  - ARGB 4444
  - AY 88
- 4:2:2
  - YCrCb, Swap Y Format
  - YCrCb, Normal
  - YCrCb, UV Swap
  - YCrCb, UV/Y Swap

Many texture mapping modes are supported. Perspective correct mapping is always performed. As the map is fitted across the polygon, the map can be tiled, mirrored in either the U or V directions, or

mapped up to the end of the texture and no longer placed on the object (this is known as clamp mode). The way a texture is combined with other object attributes is also definable.

Texture ColorKey and ChromaKey

ColorKey and ChromaKey describe two methods of removing a specific color or range of colors from a texture map before it is applied to an object. For “nearest” texture filter modes, removing a color simply makes those portions of the object transparent (the previous contents of the back buffer show through). For “ linear “ texture filtering modes, the texture filter is modified if only the non-nearest neighbor texels match the key (range).

ColorKeying occurs with paletted textures, and removes colors according to an index (before the palette is accessed). When a color palette is used with indices to indicate a color in the palette, the indices can be compared against a state variable “ColorKey Index Value” and if a match occurs and ColorKey is enabled, then this value’s contribution is removed from the resulting pixel color. The GMCH2-M defines index matching as ColorKey.

ChromaKeying can be performed for both paletted and non-paletted textures, and removes texels that fall within a specified color range. The ChromaKey mode refers to testing the RGB or YUV components to see if they fall between high and low state variable values. If the color of a texel contribution is in this range and ChromaKey is enabled, then this contribution is removed from the resulting pixel color.

Multiple Texture Composition

The GMCH2-M includes support for two simultaneous texture maps. This support greatly reduces the need for multipass compositing techniques for effects such as diffuse light maps, specular reflection maps, bump mapping, detail textures, gloss maps, shadows, and composited effects like dirt or tire marks. Supporting these techniques in hardware greatly increases compositing performance by reducing the need to read and write the frame buffer multiple times.

This multitexture support provides a superset of the “legacy” one-texture (pre-DirectX 6) texture blend modes and a large subset of the operations defined in DirectX 6 and the OpenGL ARB multitexture extensions.

The Multitexture Compositing Unit is capable of combining the interpolated vertex diffuse color, a constant color value, and up to two texels per pixel in a fully programmable fashion. Up to three operations (combinations) can be performed in a pipelined organization, with intermediate storage to support complex equations, e.g., of the form “A*B + C*D” required for light maps and specular gloss maps. Separate operations can be performed on color (RGB) and alpha components.

4.12.6. 2D Operation

The GMCH2-M contains BLT and STRBLT functionality, a hardware cursor, and an extensive set of 2D registers and instructions.

GMCH2-M VGA Registers and Enhancements

The 2D registers are a combination of registers defined by IBM* when the Video Graphics Array (VGA) was first introduced, and others that Intel® has added to support graphics modes that have color depths, resolutions, and hardware acceleration features that go beyond the original VGA standard. The internal graphics device of the GMCH2-M improves upon VGA by providing additional features that are used through numerous additional registers.

The GMCH2-M also supports an optional display cache. As an improvement on the VGA standard display cache port-hole, the GMCH2-M also maps the entire display cache into part of a single contiguous memory space at a programmable location, providing what is called “linear” access to the display cache. The size of this memory can be up to 4 MB, and the base address is set via PCI configuration registers. Alternatively, these buffers may be implemented in system memory (via D.V.M.), thus alleviating the need for the display cache.

4.12.7. Fixed Blitter (BLT) and Stretch Blitter (STRBLT) Engines

The GMCH2-M‘s 64-bit BLT engine provides hardware acceleration for many common Windows* operations. The following are two primary BLT functions: Fixed Blitter (BLT) and Stretch Blitter (STRBLT). The term BLT refers to a block transfer of pixel data between memory locations. The word “fixed” is used to differentiate from the Stretch BLT engine. The BLT engine can be used for the following:

- Move rectangular blocks of data between memory locations
- Data Alignment
- Perform logical operations

The internal graphics device of the GMCH2-M has instructions to invoke BLT and STRBLT operations, permitting software to set up instruction buffers and use batch processing as described in the 3D/2D Instruction Processing (Pipeline Preprocessor) Section. Note that these instructions replace the need to do PIO directly to BLT and STRBLT registers, which speeds up the operation.

4.12.7.1. Fixed BLT Engine

The rectangular block of data does not change as it is transferred between memory locations. The allowable memory transfers are between: system memory and display cache, display cache and display cache, and system memory and system memory. Data to be transferred can consist of regions of memory, patterns, or solid color fills. A pattern will always be 8x8 pixels wide and may be 8, 16, or 24 bits per pixel.

The internal graphics device of the GMCH2-M has the ability to expand monochrome data into a color depth of 8, 16, or 24 bits. BLTs can be either opaque or transparent. Opaque transfers, move the data specified to the destination. Transparent transfers, compare destination color to source color and write according to the mode of transparency selected.

Data is horizontally and vertically aligned at the destination. If the destination for the BLT overlaps with the source memory location, the GMCH2-M can specify which area in memory to begin the BLT transfer. Use of this BLT engine accelerates the Graphical User Interface (GUI) of Microsoft* Windows. Hardware is included for all 256 raster operations (Source, Pattern, and Destination) defined by Microsoft*, including transparent BLT.

4.12.7.2. Arithmetic Stretch BLT Engine

The stretch BLT function can stretch source data in the X and Y directions to a destination larger or smaller than the source. Stretch BLT functionality expands a region of memory into a larger or smaller region using replication and interpolation.

The stretch BLT engine also provides format conversion and data alignment. Through an algorithm implemented in the mapping engine, object expansion and contraction can occur in the horizontal and vertical directions.

4.12.8. Hardware Motion Compensation

The Motion Compensation (MC) process consists of reconstructing a new picture by predicting (either forward, backward or bidirectionally) the resulting pixel colors from one or more reference pictures. The GMCH2-M intercepts the DVD pipeline at Motion Compensation and implements Motion Compensation and subsequent steps in hardware. Performing Motion Compensation in hardware reduces the processor demand of software-based MPEG-2 decoding, and thus improves system performance.

The GMCH2-M's implementation of Hardware Motion Compensation supports a motion smoothing algorithm. When the system processor is not able to process the MPEG decoding stream in a timely manner (as can happen in software DVD implementations), the Intel® 815EM chipset GMCH2-M supports downsampled MPEG decoding. Downsampling allows for reduced spatial resolution in the MPEG picture while maintaining a full frame rate, and thus reduces processor load while maintaining the best video quality possible given the processor constraints.

4.12.9. Hardware Cursor and Popup Support

The internal graphics device of the GMCH2-M allows an unlimited number of cursor patterns to be stored in the display cache or system memory. Two sets of registers, contain the x and y position of the cursor relative to the upper left corner of the display. The following four cursor modes are provided:

- 32x32 2 bpp AND/XOR 2-plane mode
- 64x64 2 bpp 3-color and transparency mode
- 64x64 2 bpp AND/XOR 2-plane mode
- 64x64 2 bpp 4-color mode

Intel® 815EM chipset implements a popup in addition to the cursor. The Intel® 815EM chipset popup and cursor have the same functionality as the Intel® 815E chipset cursor. The Intel® 815EM chipset popup is implemented by replicating the cursor logic, it is allowable for both the cursor and the popup to be active on the screen at the same time.

4.12.10. Overlay Engine

The overlay engine provides a method of merging either video capture data (from an external PCI Video Capture Adapter) or data delivered by the processor, with the graphics data on the screen. Supported data formats include YUV 4:2:2, YUV 4:2:0, YUV 4:1:0, YUV 4:1:1, RGB15, and RGB16. The source data can be mirrored horizontally or vertically or both. Overlay data comes from a buffer located in system memory. Additionally, the overlay engine can be quadruple buffered in order to support flipping between different overlay images. Data can either be transferred into the overlay buffer from the host or from an external PCI adapter, such as DVD hardware or video capture hardware. Buffer swaps can be done by the host and internally synchronized with the display VBLANK.

The internal graphics device of the GMCH2-M can accept line widths up to 720 pixels. In addition, overlay source and destination ChromaKeying are also supported. Overlay source/destination ChromaKeying enables blending of the overlay with the underlying graphics background. Destination color/chroma keying can be used to handle occluded portions of the overlay window on a pixel by pixel basis, which is actually an underlay. Source color/chroma keying is used to handle transparency based on the overlay window on a pixel by pixel basis. This is used when "blue screening" an image in order to overlay the image on a new background later.

To compensate for overlay color intensity loss due to the non-linear response between display devices, the overlay engine supports independent gamma correction. In addition, the brightness, saturation, and contrast of the overlay may be independently varied.

4.12.11. Display

The display function contains a RAM-based Digital-to-Analog Converter (RAMDAC) that transforms the digital data from the graphics and video subsystems to analog data for the monitor. The GMCH2-M's integrated 230MHz RAMDAC provides resolution support up to 1600x1200. Circuitry is incorporated to limit the switching noise generated by the DACs. Three 8-bit DACs provide the R, G, and B signals to the monitor. Sync signals are properly delayed to match any delays from the D-to-A conversion. Associated with each DAC is a 256 pallet of colors. The RAMDAC can be operated in either direct or indexed color mode. In Direct color mode, pixel depths of 15, 16, or 24 bits can be realized. Non-interlaced mode is supported. Gamma correction can be applied to the display output.

The GMCH2-M supports a wide range of resolutions, color depths, and refresh rates via a programmable dot clock that has a maximum frequency of 230MHz.

Table 20. Partial List of Display Modes Supported

Resolution	Bits Per Pixel (frequency in Hz)		
	8-bit Indexed	16-bit	24-bit
320x200	70	70	70
320x240	70	70	70
352x480	70	70	70
352x576	70	70	70
400x300	70	70	70
512x384	70	70	70
640x400	70	70	70
640x480	60,70,72,75,85	60,70,72,75,85	60,70,72,75,85
720x480	75,85	75,85	75,85
720x576	60,75,85	60,75,85	60,75,85
800x600	60,70,72,75,85	60,70,72,75,85	60,70,72,75,85
1024x768	60, 70,72,75,85	60, 70,72,75,85	60, 70,72,75,85
1152x864	60,70,72,75,85	60,70,72,75,85	60,70,72,75,85
1280x720	60,75,85	60,75,85	60,75,85
1280x960	60,75,85	60,75,85	60,75,85
1280x1024	60,70,72,75,85	60,70,72,75,85	60,70,75,85
1600x900	60,75,85	60,75,85	
1600x1200	60,70,72,75		

4.12.12. Digital Video Out (DVO) Port

The Digital Video Out (DVO) port is an Intel® standard. This port is a 16 bit digital port (4 control bits and 12 data bits). The DVO Port is a scaleable low voltage interface that ranges from nominal 1.1V to 1.8V. It consists of a single interface that can serve as either a TV-Out or Digital-Out interface.

TV-Out interface is an output of PC graphics controller to one of many possible connections to analog video standard (NTSC or PAL) that can be connected to a TV monitor, VCR or other video devices. This is accomplished by using a TV Encoder device that encodes the digital pixel data generated by the graphics controller into a usable video signal. Depending on the capabilities of the TV Encoder, this may be NTSC or PAL TV format.

The Digital-Out interface is an output of the PC graphics controller to the Digital TFT (Thin-Film-Transistor) Flat Panel or Digital CRT monitor. This is accomplished by using a TMDS (Transition Minimized Differential Signaling) device that transmits the digital pixel data generated by the graphics controller into a TMDS interface.

4.12.12.1. VCH interface

For mobile applications, this DVO port can be connected to the VCH chip that has integrated LVDS and
panel fitting logic. The VCH provides direct flat panel interface via LVDS (or CMOS) signaling and can be set to bypass the DVO stream (DVOr) to support other DVO devices to the platform. When used with the VCH, a LTVCLKIN/STALL signal is used for panel fitting flow control.

This DVO port is used to stream the primary and overlay surfaces to an LCD Display, TV, or digital display. This is accomplished by providing the interface to the discrete TV Encoder, discrete TMDS Transmitter, or integrated TV Encoder & TMDS Transmitter, all of which are external to the GMCH2-M. Simultaneous operation of the LCD Panel and the DVO bypass is not allowed. However, switching between TV Display and LCD Display modes is possible at any time, and will not require the device to be powered down.

Figure 9. Digital Video Out Port Mobile Application Block Diagram With VCH

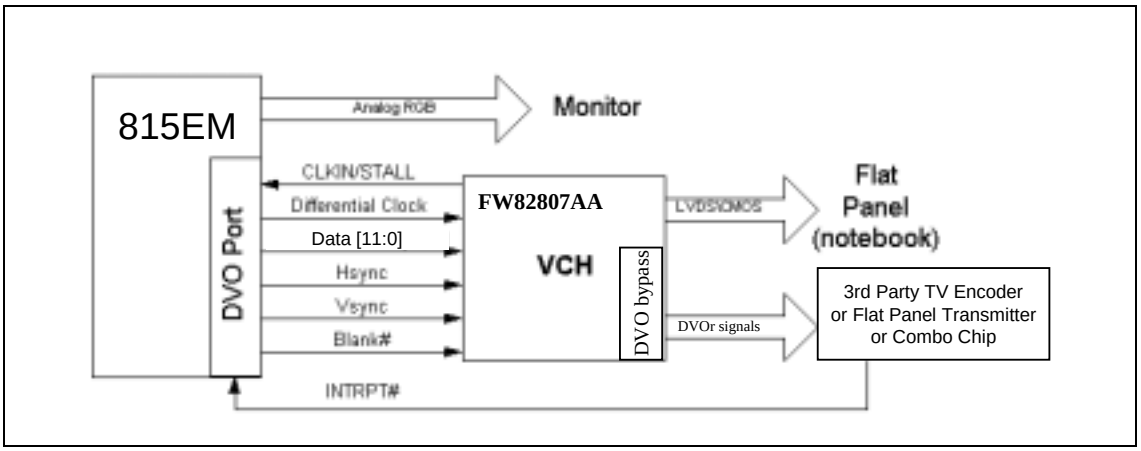
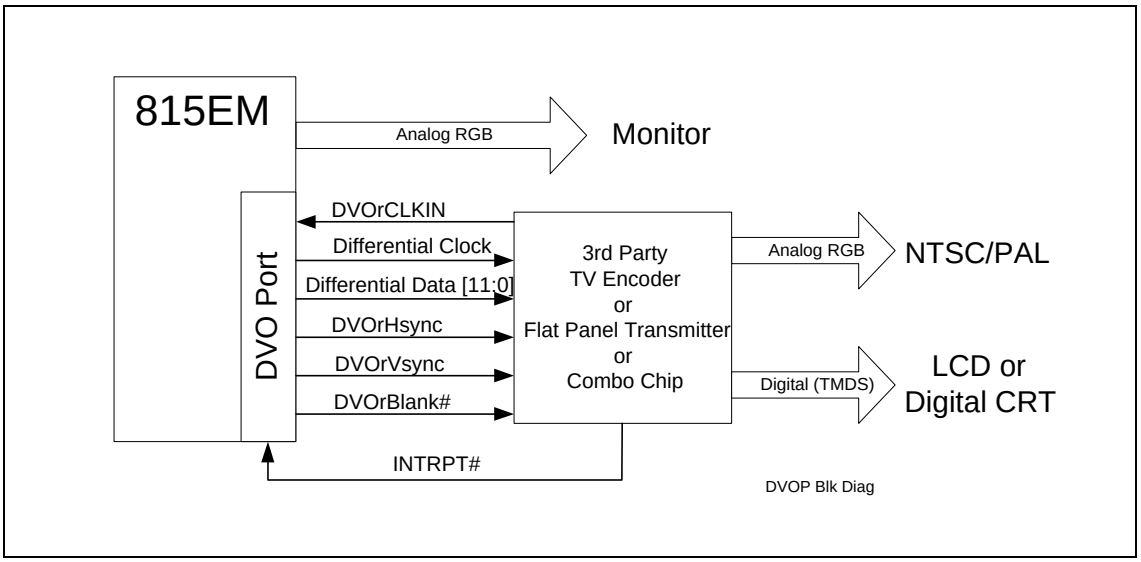


Figure 10. Digital Video Out Port Block Diagram Without VCH



4.12.12.2. DVO Port Data Format

The Intel® DVO port data bus width is 12-bits wide, the data is output in a 12-bit package at each edge of a pixel clock, and uses the LTVBLANK signal to determine when active pixel data is available.

Intel® DVO port overlay input data can be YUV progressive. In this case the overlay should be set to frame mode. Each overlay buffer contains a frame, and the overlay is flipped between them. The overlay does not do anything special, since the data matches the typical non-interlaced CRT screens. In other cases, where the input data is an interlaced field type data, the overlay can be set to field mode, and interlaced scanning is bi-linearly filtered into progressive data before it is displayed.

Connecting the GMCH2-M to a flat panel transmitter is demonstrated below. For more details, refer to The *815EM Mobile Platform Recommended Design and Debug Practices*.

The 815EM supports a variety of Flat Panel display modes and refresh rates that require up to a 65MHz dot clock over this interface. The following table shows some of the display modes supported by the 815EM.

Table 21. Partial List of Flat Panel Modes Supported

Resolution	Bits Per Pixel (frequency in Hz)		
	8-bit Indexed	16-bit	24-bit
320x200[1]	60	60	60
320x240[1]	60	60	60
352x480[1]	60	60	60
352x480[1]	60	60	60
352x576[1]	60	60	60
400x300[1]	60	60	60
512x384[1]	60	60	60
640x350[1]	60	60	60
640x400[1]	60	60	60
640x480	60	60	60
720x480[1]	60	60	60
720x576[1]	60	60	60
800x600	60	60	60
1024x768	60	60	60
1400x1050	60	60	N/A

[1] These resolutions are supported via centering.

Table 22. Partial List of TV-Out Modes Supported

Resolution	Colors	NTSC	PAL
320x200[1]	256	Yes	Yes
	16M	Yes	Yes
	64k	Yes	Yes
320x240	256	Yes	Yes
	16M	Yes	Yes
	64k	Yes	Yes
352x480[1]	256	Yes	Yes
	16M	Yes	Yes
	64k	Yes	Yes
352x576[1]	256	Yes	Yes
	16M	Yes	Yes
	64k	Yes	Yes

Resolution	Colors	NTSC	PAL
400x300[1]	256	Yes	Yes
	16M	Yes	Yes
	64k	Yes	Yes
640x400[1]	256	Yes	Yes
640x480	256	Yes	Yes
	64k	Yes	Yes
	16M	Yes	Yes
720x480[1]	256	Yes	Yes
	64k	Yes	Yes
	16M	Yes	Yes
720x576[1]	256	Yes	Yes
	64k	Yes	Yes
	16M	Yes	Yes
800x600	16	Yes	Yes
	256	Yes	Yes
	32k	Yes	Yes
	64k	Yes	Yes
	16M	Yes	Yes

These resolutions are supported via centering.

4.12.12.3. DVO Port I²C Functionality

I²C bus is a standard 2-wire communications bus/protocol. There are two I²C compatible buses in the GMCH2-M for DDC and DVO connectivities. The I²C buses are used to collect EDID from Digital Display Panel, and to detect and configure registers in the TV Encoder, or TMDS Transmitter chips. The Intel® DVO port controls the video front-end devices through the I²C bus using LTVDA and LTVCK pins. The Display Data Channel or DDC uses I²C bus via DDDA and DDCK pins.

4.12.13. DDC (Display Data Channel)

DDC is a standard defined by VESA. Its purpose is to allow communication between the host system and display. Both configuration and control information can be exchanged allowing plug-and-play systems to be realized. Support for DDC 2B is implemented.

4.13. System Reset for the GMCH2-M

Refer to the *Intel® 815 Chipset Platform* Design Guide (Power Sequencing section) for details.

4.14. System Clock Description

4.14.1. External Clock Sources

The GMCH2-M device shall receive the following clock frequencies and references:

- 100/66 MHz host clock, used to run core logic (host, 2D, 3D).
- 66 MHz AGP/Hub Interface.
- 48 MHz reference - used to derive video dot clocks for Display and LCD/TVOut interfaces.
- 40 MHz Tvclkin from the External DVO device

The following table describes the clock alignments for the external clock sources.

Table 23. Supported Frequencies and Corresponding Phase Alignments

Host Interface (HCLK)	Hub / AGP Interface (BCLK)	System Memory (SCLK)	Local Memory (LCLK)	Core (RCLK)	External Phase Alignment
66 Mhz	66 Mhz	100 Mhz	100 Mhz	100 Mhz	HCLK and BCLK 180 degrees out of phase
			133Mhz		
100 Mhz	66 Mhz	100 Mhz	100 Mhz	100 Mhz	HCLK and SCLK 180 degrees out of phase
			133Mhz		

4.14.2. Internal Clock Sources

The internal graphics device shall source the following interface frequencies and references:

1. 100 MHz for the system memory subsystem.
2. 133/100 MHz for the local memory subsystem.
3. 100 MHz for the graphics core.
4. 266/133/66 MHz for AGP in 4X/2X/1X modes respectively.
5. 66 MHz for the hub interface.
6. 20-112 MHz – LCD/TVout interface.

4.15. Power Management

4.15.1. Specifications Supported

The platform is compliant with the following specifications:

- APM Rev 1.2
- ACPI Rev 1.0
- PCI Power Management Rev 1.0
- PC 99 System Design Guide, Rev 1.0

This chapter includes general description of the ACPI power states, transition rules among its states, power states Intel® 815EM chipset supports, entering and exiting C2/C3/S1/S3 state. Intel® 815EM chipset supports several levels of power management.

4.16. General Description of ACPI Power States

Intel® 815EM chipset will support the ACPI compliant power states. The following table describes in general the ACPI power states. It is for informational purposes and should not be used by designers or validations as part of the behavioral description.

Table 24. General Description of ACPI Power States

G0/S0/C0	Full on: Processor is fully operating. Individual devices may be shutdown to save power. Different processor operating levels are described in system level state transition table below. Within the C0 state, the ICH2-M can throttle the STPCLK# signal to further reduce power consumption.
G0/S0/C1	Auto-Halt: Processor has executed an AutoHalt instruction and is not executing code. The processor snoops the bus and maintains cache coherency.
G0/S0/C2	Stop-Grant for Desktop or Quick-start for Mobile: The STPCLK# signal goes active to the processor. The processor performs a Stop-Grant cycle, halts its instruction stream, and remain in that state until the STPCLK# signal goes inactive. In the Stop-Grant state, the processor snoops the bus and maintains cache coherency. The Quick-start state is lower power version, but there are restrictions on what interrupt signals can go active while STPCLK# is active. Note: Some mobile systems may use the Stop-Grant state rather than the Quick-start state.
G0/S0/C3	Stop-Clock: This is only for mobile systems. The STPCLK# signal goes active to the processor. The processor performs a Stop-Grant cycle and halts its instruction stream. ICH2-M then asserts STP_CPU# that forces the clock generator to stop the processor clock. This is also used in the mobile system for Intel® SpeedStep™ Technology support.
G1/S1(Desktop)	Stop-Grant: Similar to G0/S0/C2 state. ICH2-M also has the option to assert CPUSLP# signal to the processor to further reduce power consumption.
G1/S1 (Mobile)	Power-On Suspend (POS): In this state, all clocks are stopped except the 32.768 KHz clock. The system context is maintained in the system memory. Power is on to processor, PCI, memory controller, memory, and all other critical circuits.
G1/S3	Suspend-to-RAM (STR): The system context is maintained in system memory, but power is shut to non-critical circuits. Memory is retained and refreshes continue. All clocks are shut except RTC.
G1/S4	Suspend-to-Disk (STD): The system context is maintained on the disk. All power is shut except for the logic required to resume. Externally appears same as S5, but may have different wake events.

G2/S5	Soft Off (SOFF): System context not maintained. All power is shut except for logic required to restart. A full boot is required when waking.
G3	Mechanical Off (MOFF): System context not maintained. All power is shut except for the RTC. No wake events are possible. When system power returns, transition will depend on the state just prior to the entry to G3.

4.17. Power State Transition Rules at Platform Level

The following table describes in general power states transition rules based on various trigger events. The intermediate transitions and states are not listed in the table. It is for informational purposes and should not be used by designers or validations as part of the behavioral description.

Table 25. State Transition Rules at Platform Level

Present State	Transition Trigger	Next State
G0/S0/C0	processor halt instruction	G0/S0/C1
	ACPI defined Level 2 Read	G0/S0/C2
	ACPI defined Level 3 Read	G0/S0/C3
	SLP_EN bit set	G1/Sx or G2/S5 (specified by SLP_TYP)
	Power Button Override	G2/S5
	Mechanical Off/Power Failure	G3
G0/S0/C1	Any Enabled Break Event	G0/S0/C0
	STPCLK# goes asserted	G0/S0/C2
	Power Button Override	G2/S5
	Power Failure	G3
G0/S0/C2	Any Enabled Break Event	G0/S0/C0
	STPCLK# goes inactive and was in C1	G0/S0/C1
	Power Button Override	G2/S5
	Power Failure	G3
G0/S0/C3	Any Enabled Break Event	G0/S0/C0
	Power Button Override	G2/S5
	Power Failure	G3
G1/S1,G1/S3, G1/S4	Any Enabled Break Event	G0/S0/C0
	Power Button Override	G2/S5
	Power Failure	G3
G2/S5	Any Enabled Break Event	G0/S0/C0
	Power Failure	G3
G3	Power Returns	G0/S0/C0 reboot or G2/S5 till power button pressed / other wake event.

4.18. ACPI Support

Advanced Configuration and Power Management Interface. ACPI primarily describes and runs motherboard devices. It is completely controlled by the operating system that OS drivers directly power down PCI/AGP devices. System or SMI BIOS plays a part of waking the system, however. Device drivers save and restore state while bus drivers change the physical power state of the device.

The Intel® 815EM chipset power management architecture is designed to allow a single system to support multiple suspend modes and to switch between those modes as required. A suspended system can be resumed via a number of different events. It will then return to full operation where it can continue processing or be placed into another suspend mode (potentially a lower power mode than it resumed from).

Intel® 815EM chipset supports the minimum requirements for ACPI support. Intel® 815EM chipset must support the minimum requirements for both system logic and for graphics controllers, as well as be capable of controlling monitors minimum functions. The transition sequences of entering and exiting C2/C3/S1/S3 states are described in respective sections below.

4.18.1. Full on (C0 State)

C0 state is normal operation mode that processor executes instructions. According to typical usage models running battery life benchmark programs, processor is in C0 about 20% of time. To save power, the following is recommended:

If IOQ and Deferred Queue are empty, Intel® 815EM chipset shuts down GTL buffer sense amps. When there is a need to snoop, the logic wakes up on detection of signal ADS#.

4.18.2. Stop Grant or Quick Start (C2 State)

Stop-Grant for Desktop or Quick-start for Mobile: The STPCLK# signal goes active to the processor. The processor performs a Stop-Grant cycle, halts its instruction stream, and remain in that state until the STPCLK# signal goes inactive. In the Stop-Grant state, the processor snoops the bus and maintains cache coherency. The Quick-start state is lower power version, but there are restrictions on what interrupt signals can go active while STPCLK# is active. Note: Some mobile systems may use the Stop-Grant state rather than the Quick-start state.

4.18.3. Stop Clock (C3 State)

According to typical usage models running battery life programs, processor could be in C3 deep sleep mode 64% of time. The ICH2-M performs stop clock functions with the processor directly. The involvement of Intel® 815EM chipset is limited to the following functions: As a result of STPCLK# assertion, the processor responds with a Stop Grant special cycle which Intel® 815EM chipset passes down to Hub Interface to ICH2-M.

Similarly, as a result of Halt instruction, the processor performs Halt special cycle that Intel® 815EM chipset passes to Hub Interface to ICH2-M. Intel® 815EM chipset does *not* prevent snoops while in the Stop Grant State. There are a lot of power savings from Platform viewpoint.

4.18.4. C3 Support AGP Port Signal

This signal is generated either by the AGP Graphics Chip in AGP mode or by the Intel® 815EM chipset in graphics mode, but not by both. This is an input to the ICH2-M I/O Controller Hub.

In AGP mode:

- Asserted (active low): When asserted, AGPBUSY# indicates that the AGP device is currently busy and requests that the system not transition to the C3 state. However, assertion of AGPBUSY# does not guarantee that the system will not enter the C3 state or perform an Intel® SpeedStep™ technology transition. If system is in C3 state, then the assertion of AGPBUSY# is used to request that the system exit from the C3 state.
- The AGP GC must assert AGPBUSY# whenever the AGP GC has a pending request to use the AGP interface. The AGP GC must assert AGPBUSY# regardless of which protocol it intends to use on the AGP interface: SBA, PIPE#, or PCI.
- AGPBUSY# may only be asserted by the AGP GC when AGPBUSY# is in the D0 state and should not be asserted in the D1, D2, or D3 states.
- Deasserted (high): When deasserted, AGPBUSY# indicates that the AGP device is not busy and has no need to use the AGP interface.

In Graphics mode:

- Asserted (active low): When asserted, AGPBUSY# indicates the internal graphics unit is requesting snoop or having interrupt request to be serviced. Therefore, it requests that the system not transition to the C3 state. However, assertion of AGPBUSY# does not guarantee that the system will not enter the C3 state or perform an Intel® SpeedStep™ technology transition. If system is in C3 state, then the assertion of AGPBUSY# is used to request that the system exit from the C3 state.
- Deasserted (high): When deasserted, AGPBUSY# indicates the internal graphics unit has no pending snoop request nor graphics interrupt request.

AGPBUSY#, with a minimum of 100 ns pulse width, is considered by the rest of the system to be asynchronous to the AGP clock.

AGPBUSY# must have a 10-KΩ pull-up on the platform.

Note: This signal is OD since it can be driven by both the 815EM Memory Controller and the AGP GC.

Note: Please refer to Accelerated Graphics Port (AGP) BUSY and STOP signals for 815EM platform rev 0.1 reference number: SC2984.

4.18.5. Power-on-suspend (POS) (S1 State)

S1 state is different in Desktop versus Mobile. S1-Desktop requires processor in C2 State, main memory and all clocks are continuously running. S1-Mobile requires processor in C3 state, main memory in self refresh mode, and all clock inputs are off so only leakage power for PLLs. S1-Mobile is called POS, power on suspend state. Only RTC is on, all other clocks on Platform are off. All devices are in D1 or lower state. The graphics device will be in D3 hot. Intel® 815EM chipset has to retain registers to continue operation from where it was suspended. The ACPI OS may transition the system to S3 state if not exiting from S1.

When the system resumes from POS, ICH2-M can optionally resume without resetting the system, can reset the processor only, or can reset the entire system. When no reset is performed, the ICH2-M only needs to wait for the clock synthesizer and processor PLLs to lock before the system is resumed. This takes typically 20ms.

4.18.6. Suspend-to-RAM (STR) (S3 State)

S3 state is also called STR, suspend to RAM state. Power is removed from most of the system components during STR, except the DRAM. Power is supplied to the host bridge (for DRAM Suspend Refresh) and RTC. ICH2-M provides control signals and 32 kHz Suspend Clock (SUSCLK) to allow for DRAM refresh and to turn off the clock synthesizer and other power planes. ICH2-M will reset the system on resume from STR.

4.18.7. Suspend to DISK (STD) S4 State

Power is removed from most of the system components during STD. Power is maintained to the RTC and Suspend Well logic in the ICH2-M. ICH2-M will reset the system on resume from STD. This state can also be called the Soft Off (SOFF) state. The difference depends on whether the system state is restored by software to a pre-suspend condition or if the system is rebooted.

4.18.8. Graphics Controller Requirements

PC9x implies that D0 and D3 are obligatory for graphics controllers. D0, D2, and D3 are obligatory for monitors. Intel® 815EM chipset also permits D1 for monitors. Intel® 815EM chipset does not implement a D1 graphics controller state.

4.18.8.1. The D0 State

This is the normal on state for the Intel® 815EM chipset graphics functions. The Intel® 815EM chipset graphics functions enter this state after initialization by the Video BIOS.

4.18.8.2. The D3 State

During D3, graphics configuration space must remain accessible when power is on, but memory and I/O space access are disabled. During D3, the driver has turned off the DAC and Intel® 815EM chipset does not pulse **HSYNC** and **VSYNC** in this state.

When the OS decides to put the Intel® 815EM chipset graphics functions into D3, it calls the Intel® 815EM chipset graphics driver and tells it to place the device into the D3 state. The driver saves the device context. Device context consists of the Intel® 815EM chipset graphics mode as well as local and non-local video memory context.

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5. Pinout and Package Information

5.1. GMCH2-M Pinout

Figure 11 and Figure 12 show the ball footprint of the GMCH2-M. These figures represent the ballout by ball number provides an alphabetical signal listing of the ballout.

GMCH2-M is ball compatible to the Intel® 815 chipset GMCH except for the following ballouts in the following table.

GMCH2-M ballout is subject to change prior to ballout freeze.

Table 26. Ballout differences between Intel® 815 Chipset GMCH and Intel® 815EM Chipset GMCH2-M

PIN #	Intel® 815 Chipset GMCH	Intel® 815EM Chipset GMCH2-M
E7	VSS	AGPBUSY#
Y17	VSS	INTRPT#
AA6*	V_1.8	RESERVED
AC18	LTVCLKIN/INT#	LTVCLKIN/STALL

Note: AA6 in Intel® 815EM chipset needs to be connected to V_1.8 for backward compatibility to Intel® 815 chipset

Figure 11. GMCH2-M Pinout (Top View-Left Side)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	SMD_17	SMD_49	SMD_16	SMD_48	SDQM_7	SDQM_3	SDQM_2	SCSB_5#	SMAC_7#	SMAC_5#	SMAA_7	SMAA_5	SMAA_11
B	SMD_50	VSUS_3.3	SMD_56	SMD_23	VSUS_3.3	SDQM_6	SMAA_12	VSUS_3.3	SCSB_4#	SMAC_4#	VSUS_3.3	SMAA_4	SBS_0
C	SMD_18	SMD_25	VSS	SMD_55	SMD_22	VSS	SCKE_5	SCKE_4	VSS	SMAC_6#	SMAA_6	VSS	SMAA_9
D	VSS	SMD_57	SMD_26	SMD_24	SMD_54	SMD_21	SCKE_3	SCKE_0	SCSB_3#	SCSB_2#	SBS_1	SMAA_8	SMAA_0
E	SMD_51	VSUS_3.3	SMD_58	SMD_27	VSS	SMD_53	AGPBUSY#	SCKE_1	SCKE_2	VSS	SMAA_10	VSS	SCSA_4#
F	VSS	SMD_19	VSS	SMD_59	SMD_28	SMD_60	SCLK	SCSB_1#	SCSB_0#	VSUS_3.3	VSS	SMAA_2	VSS
G	ADS#	SMD_52	SMD_20	SMD_29	SMD_61	VSUS_3.3	SRCOMP	VSUS_3.3	VSS	NC			
H	RS_2#	VSUS_3.3	RESET#	SMD_62	VSUS_3.3	VSS	VSUS_3.3						
J	DRDY#	VSS	DBSY#	SMD_63	VSS	SMD_30	VCCDPLL						
K	HIT#	RS_0#	HTRDY#	VSS	SMD_31	V_1.8	VSSDPLL						
L	RS_1#	VSS	HITM#	HLOCK#	HREQ_3#	VSS					VSS	VSS	VSS
M	HREQ_0#	HREQ_2#	DEFER#	VSS	BPRI#	V_1.8					VSS	VSS	VSS
N	HREQ_1#	VSS	HREQ_4#	BNR#	HA_7#	VSS					VSS	VSS	VSS
P	HA_4#	HA_11#	HA_14#	VSS	HA_8#	V_1.8					VSS	VSS	VSS
R	HA_9#	VSS	HA_6#	HA_3#	HA_16#	VSS					VSS	VSS	VSS
T	HA_12#	HA_5#	HA_13#	VSS	HA_15#	V_1.8					VSS	VSS	VSS
U	HA_10#	VSS	HA_28#	HA_21#	HA_25#	GTLREF0	VSS						
V	HA_31#	HA_22#	HA_19#	VSS	HA_17#	VSS	V_1.8						
W	HA_20#	VSS	HA_23#	HA_24#	HA_30#	V_1.8	VSS						
Y	HA_29#	HA_18#	HA_27#	VSS	HA_26#	VSS	V_1.8	VSS	V_1.8	VSS			
AA	HD_0#	VSS	HD_6#	HD_15#	CPURST#	RESERVED	HCLK	V_1.8	VSS	GTLREF1	V_1.8	VSS	V_1.8
AB	HD_4#	HD_1#	HD_5#	VSS	HD_23#	HD_19#	HD_31#	HD_34#	HD_37#	HD_42#	HD_41#	HD_48#	HD_55#
AC	HD_8#	VSS	HD_17#	HD_7#	VSS	HD_25#	VSS	HD_22#	VSS	HD_44#	VSS	HD_63#	VSS
AD	HD_10#	HD_12#	HD_13#	HD_3#	HD_30#	HD_16#	HD_33#	HD_29#	HD_43#	HD_39#	HD_27#	HD_47#	HD_59#
AE	HD_18#	VSS	HD_11#	VSS	HD_21#	VSS	HD_35#	VSS	HD_36#	VSS	HD_49#	VSS	HD_57#
AF	HD_14#	HD_2#	HD_9#	HD_20#	HD_24#	HD_26#	HD_32#	HD_28#	HD_38#	HD_45#	HD_51#	HD_40#	HD_52#
	1	2	3	4	5	6	7	8	9	10	11	12	13

Figure 12. GMCH2-M Pinout (Top View-Right Side)

14	15	16	17	18	19	20	21	22	23	24	25	26	
SMAB_7#	SMAB_5#	SMAA_3	SCSA_1#	SDQM_4	SMD_47	SMD_45	SMD_42	SMD_39	SMD_37	SMD_35	SMD_33	SMD_32	A
VSUS_3.3	SMAB_4#	SMAA_1	SCSA_5#	SMD_12	VSUS_3.3	SMD_44	SMD_41	VSUS_3.3	SMD_36	SMD_34	VSUS_3.3	VSS	B
SMAB_6#	VSS	SRAS#	SDQM_5	VSS	SMD_46	SMD_43	VSS	SMD_38	SMD_1	VSS	V_1.8	HL_10	C
SCSA_2#	SCSA_0#	SDQM_0	SMD_15	SCAS#	SMD_10	SMD_7	SMD_40	SMD_2	SMD_0	HL_9	HL_8	HL_7	D
SCSA_3#	VSS	SWE#	VSS	SMD_11	SMD_9	VSS	SMD_4	VSSBA	VCCBA	V_1.8	HL_6	HL_5	E
VSUS_3.3	SDQM_1	VSS	VSUS_3.3	SMD_13	SMD_8	SMD_6	SMD_3	HLCLK	V_1.8	HL_4	VSS	HLPSTRB#	F
			VSS	SMD_14	VSUS_3.3	SMD_5	VSS	V_1.8	VSS	HL_3	HLPSTRB	V_1.8	G
						HLZCOMP	HLREF	VSS	GCBE_0#	HL_0	HL_2	HL_1	H
						GAD_5	GAD_3	GAD_1	VSS	AGPREF	VSS	GRCOMP	J
						VDDQ	VSS	GAD_8	GAD_7	VSS	GAD_2	GAD_0	K
VSS	VSS	VSS					VDDQ	VSS	ADSTB0#	GAD_4	VSS	GAD_6	L
VSS	VSS	VSS					GAD_12	ADSTB0	VDDQ	GAD_10	GAD_9	GAD_11	M
VSS	VSS	VSS					GCBE_1#	GAD_14	VSS	GAD_13	VDDQ	GAD_15	N
VSS	VSS	VSS					GTRDY#	LRCLK	GIRDY#	VSS	GSTOP#	GDEVSEL#	P
VSS	VSS	VSS					VDDQ	LOCLK	VSS	GPAR	VSS	GFRAME#	R
VSS	VSS	VSS					VSS	GAD_17	GAD_19	GAD_21	GCBE_2#	GAD_16	T
						VDDQ	GAD_23	ADSTB1	VDDQ	GAD_18	VDDQ	GAD_20	U
						VSS	GAD_25	VSS	ADSTB1#	GAD_22	GAD_24	GAD_26	V
						VDDQ	GAD_27	GAD_29	VSS	GAD_28	VSS	GAD_30	W
			INTRPT#	V_1.8	VSSDA	IWASTE	GAD_31	SBA_6	SBSTB	VDDQ	SBA_7	GCBE_3#	Y
VSS	V_1.8	VSS	V_1.8	DDDA	V_1.8	LTVDA	VCCDA	SBA_4	VSS	SBSTB#	VSS	SBA_5	AA
HD_53#	HD_56#	V_1.8	LTVHSYNC	DDCK	LTVBLANK#	V_1.8	LTVCK	SBA_0	SBA_2	WBF#	SBA_1	SBA_3	AB
HD_58#	VSS	LTVVSYNC	VSS	LTVCLKIN/ STALL	VSS	LTVDATA_8	VSS	V_1.8	ST_2	ST_1	VSS	PIPE#	AC
HD_46#	HD_60#	LTVDATA_0	LTVDATA_3	LTVDATA_5	V_1.8	LTVDATA_7	LTVDATA_11	RED	IREF	ST_0	GGNT#	RBF#	AD
VSS	HD_50#	VSS	LTVDATA_2	VSS	LTVCLKOUT_0	VSS	LTVDATA_10	GREEN	BLUE	DCLKREF	VSSDACA	GREQ#	AE
HD_54#	HD_62#	HD_61#	LTVDATA_1	LTVDATA_4	LTVCLKOUT_1	LTVDATA_6	LTVDATA_9	VSYNC	HSYNC	VSSDACA	VCCDACA2	VCCDACA1	AF
14	15	16	17	18	19	20	21	22	23	24	25	26	

Table 27. Alphabetical Pin Assignment (by Signal Name)

Signal Name	Ball #
ADS#	G1
ADSTB0	M22
ADSTB0#	L23
ADSTB1	U22
ADSTB1#	V23
AGPBUSY#	E7
AGPREF	J24
BLUE	AE23
BNR#	N4
BPRI#	M5
CPURST#	AA5
DBSY#	J3
DCLKREF	AE24
DDCK	AB18
DDDA	AA18
DEFER#	M3
DRDY#	J1
GAD_00	K26
GAD_01	J22
GAD_02	K25
GAD_03	J21
GAD_04	L24
GAD_05	J20
GAD_06	L26
GAD_07	K23
GAD_08	K22
GAD_09	M25
GAD_10	M24
GAD_11	M26
GAD_12	M21
GAD_13	N24
GAD_14	N22
GAD_15	N26
GAD_16	T26
GAD_17	T22
GAD_18	U24
GAD_19	T23

Signal Name	Ball #
GAD_20	U26
GAD_21	T24
GAD_22	V24
GAD_23	U21
GAD_24	V25
GAD_25	V21
GAD_26	V26
GAD_27	W21
GAD_28	W24
GAD_29	W22
GAD_30	W26
GAD_31	Y21
GCBE_0#	H23
GCBE_1#	N21
GCBE_2#	T25
GCBE_3#	Y26
GDEVSEL#	P26
GFRAME#	R26
GGNT#	AD25
GIRDY#	P23
GPAR	R24
GRCOMP	J26
GREEN	AE22
GREQ#	AE26
GSTOP#	P25
GTLREF0	U6
GTLREF1	AA10
GTRDY#	P21
HA_03#	R4
HA_04#	P1
HA_05#	T2
HA_06#	R3
HA_07#	N5
HA_08#	P5
HA_09#	R1
HA_10#	U1
HA_11#	P2

Signal Name	Ball #
HA_12#	T1
HA_13#	T3
HA_14#	P3
HA_15#	T5
HA_16#	R5
HA_17#	V5
HA_18#	Y2
HA_19#	V3
HA_20#	W1
HA_21#	U4
HA_22#	V2
HA_23#	W3
HA_24#	W4
HA_25#	U5
HA_26#	Y5
HA_27#	Y3
HA_28#	U3
HA_29#	Y1
HA_30#	W5
HA_31#	V1
HCLK	AA7
HD_00#	AA1
HD_01#	AB2
HD_02#	AF2
HD_03#	AD4
HD_04#	AB1
HD_05#	AB3
HD_06#	AA3
HD_07#	AC4
HD_08#	AC1
HD_09#	AF3
HD_10#	AD1
HD_11#	AE3
HD_12#	AD2
HD_13#	AD3
HD_14#	AF1
HD_15#	AA4

Signal Name	Ball #
HD_16#	AD6
HD_17#	AC3
HD_18#	AE1
HD_19#	AB6
HD_20#	AF4
HD_21#	AE5
HD_22#	AC8
HD_23#	AB5
HD_24#	AF5
HD_25#	AC6
HD_26#	AF6
HD_27#	AD11
HD_28#	AF8
HD_29#	AD8
HD_30#	AD5
HD_31#	AB7
HD_32#	AF7
HD_33#	AD7
HD_34#	AB8
HD_35#	AE7
HD_36#	AE9
HD_37#	AB9
HD_38#	AF9
HD_39#	AD10
HD_40#	AF12
HD_41#	AB11
HD_42#	AB10
HD_43#	AD9
HD_44#	AC10
HD_45#	AF10
HD_46#	AD14
HD_47#	AD12
HD_48#	AB12
HD_49#	AE11
HD_50#	AE15
HD_51#	AF11
HD_52#	AF13

Signal Name	Ball #
HD_53#	AB14
HD_54#	AF14
HD_55#	AB13
HD_56#	AB15
HD_57#	AE13
HD_58#	AC14
HD_59#	AD13
HD_60#	AD15
HD_61#	AF16
HD_62#	AF15
HD_63#	AC12
HIT#	K1
HITM#	L3
HL_00	H24
HL_01	H26
HL_02	H25
HL_03	G24
HL_04	F24
HL_05	E26
HL_06	E25
HL_07	D26
HL_08	D25
HL_09	D24
HL_10	C26
HLCLK	F22
HLOCK#	L4
HLPSTRB	G25
HLPSTRB#	F26
HLREF	H21
HLZCOMP	H20
HREQ_0#	M1
HREQ_1#	N1
HREQ_2#	M2
HREQ_3#	L5
HREQ_4#	N3
HSYNC	AF23
HTRDY#	K3
INTRPT#	Y17

Signal Name	Ball #
IREF	AD23
IWASTE	Y20
LOCLK	R22
LRCLK	P22
LTVBLANK#	AB19
LTVCK	AB21
LTVDA	AA20
LTVCLKOUT_0	AE19
LTVCLKOUT_1	AF19
LTVCLKIN	AC18
LTVDATA_00	AD16
LTVDATA_01	AF17
LTVDATA_02	AE17
LTVDATA_03	AD17
LTVDATA_04	AF18
LTVDATA_05	AD18
LTVDATA_06	AF20
LTVDATA_07	AD20
LTVDATA_08	AC20
LTVDATA_09	AF21
LTVDATA_10	AE21
LTVDATA_11	AD21
LTVHSYNC	AB17
LTVVSYNC	AC16
NC	G10
PIPE#	AC26
RBF#	AD26
RED	AD22
RESERVED	AA6
RESET#	H3
RS_0#	K2
RS_1#	L1
RS_2#	H1
SBA_0	AB22
SBA_1	AB25
SBA_2	AB23
SBA_3	AB26
SBA_4	AA22

Signal Name	Ball #
SBA_5	AA26
SBA_6	Y22
SBA_7	Y25
SBS_0	B13
SBS_1	D11
SBSTB	Y23
SBSTB#	AA24
SCAS#	D18
SCKE_0	D8
SCKE_1	E8
SCKE_2	E9
SCKE_3	D7
SCKE_4	C8
SCKE_5	C7
SCLK	F7
SCSA_0#	D15
SCSA_1#	A17
SCSA_2#	D14
SCSA_3#	E14
SCSA_4#	E13
SCSA_5#	B17
SCSB_0#	F9
SCSB_1#	F8
SCSB_2#	D10
SCSB_3#	D9
SCSB_4#	B9
SCSB_5#	A8
SDQM_0	D16
SDQM_1	F15
SDQM_2	A7
SDQM_3	A6
SDQM_4	A18
SDQM_5	C17
SDQM_6	B6
SDQM_7	A5
SMAA_00	D13
SMAA_01	B16
SMAA_02	F12

Signal Name	Ball #
SMAA_03	A16
SMAA_04	B12
SMAA_05	A12
SMAA_06	C11
SMAA_07	A11
SMAA_08	D12
SMAA_09	C13
SMAA_10	E11
SMAA_11	A13
SMAA_12	B7
SMAB_4#	B15
SMAB_5#	A15
SMAB_6#	C14
SMAB_7#	A14
SMAC_4#	B10
SMAC_5#	A10
SMAC_6#	C10
SMAC_7#	A9
SMD_00	D23
SMD_01	C23
SMD_02	D22
SMD_03	F21
SMD_04	E21
SMD_05	G20
SMD_06	F20
SMD_07	D20
SMD_08	F19
SMD_09	E19
SMD_10	D19
SMD_11	E18
SMD_12	B18
SMD_13	F18
SMD_14	G18
SMD_15	D17
SMD_16	A3
SMD_17	A1
SMD_18	C1
SMD_19	F2

Signal Name	Ball #
SMD_20	G3
SMD_21	D6
SMD_22	C5
SMD_23	B4
SMD_24	D4
SMD_25	C2
SMD_26	D3
SMD_27	E4
SMD_28	F5
SMD_29	G4
SMD_30	J6
SMD_31	K5
SMD_32	A26
SMD_33	A25
SMD_34	B24
SMD_35	A24
SMD_36	B23
SMD_37	A23
SMD_38	C22
SMD_39	A22
SMD_40	D21
SMD_41	B21
SMD_42	A21
SMD_43	C20
SMD_44	B20
SMD_45	A20
SMD_46	C19
SMD_47	A19
SMD_48	A4
SMD_49	A2
SMD_50	B1
SMD_51	E1
SMD_52	G2
SMD_53	E6
SMD_54	D5
SMD_55	C4
SMD_56	B3
SMD_57	D2

Signal Name	Ball #
SMD_58	E3
SMD_59	F4
SMD_60	F6
SMD_61	G5
SMD_62	H4
SMD_63	J4
SRAS#	C16
SRCOMP	G7
ST_0	AD24
ST_1	AC24
ST_2	AC23
SWE#	E16
V_1.8	AA11
V_1.8	AA13
V_1.8	AA15
V_1.8	AA17
V_1.8	AA19
V_1.8	AA8
V_1.8	AB16
V_1.8	AB20
V_1.8	AC22
V_1.8	AD19
V_1.8	C25
V_1.8	E24
V_1.8	F23
V_1.8	G22
V_1.8	G26
V_1.8	K6
V_1.8	M6
V_1.8	P6
V_1.8	T6
V_1.8	V7
V_1.8	W6
V_1.8	Y18
V_1.8	Y7
V_1.8	Y9
VCCBA	E23
VCCDA	AA21

Signal Name	Ball #
VCCDACA1	AF26
VCCDACA2	AF25
VCCDPLL	J7
VDDQ	K20
VDDQ	L21
VDDQ	M23
VDDQ	N25
VDDQ	R21
VDDQ	U20
VDDQ	U23
VDDQ	U25
VDDQ	W20
VDDQ	Y24
VSS	AA12
VSS	AA14
VSS	AA16
VSS	AA2
VSS	AA23
VSS	AA25
VSS	AA9
VSS	AB4
VSS	AC11
VSS	AC13
VSS	AC15
VSS	AC17
VSS	AC19
VSS	AC2
VSS	AC21
VSS	AC25
VSS	AC5
VSS	AC7
VSS	AC9
VSS	AE10
VSS	AE12
VSS	AE14
VSS	AE16
VSS	AE18
VSS	AE2

Signal Name	Ball #
VSS	AE20
VSS	AE4
VSS	AE6
VSS	AE8
VSS	B26
VSS	C12
VSS	C15
VSS	C18
VSS	C21
VSS	C24
VSS	C3
VSS	C6
VSS	C9
VSS	D1
VSS	E10
VSS	E12
VSS	E15
VSS	E17
VSS	E20
VSS	E5
VSS	F1
VSS	F11
VSS	F13
VSS	F16
VSS	F25
VSS	F3
VSS	G17
VSS	G21
VSS	G23
VSS	G9
VSS	H22
VSS	H6
VSS	J2
VSS	J23
VSS	J25
VSS	J5
VSS	K21
VSS	K24

Signal Name	Ball #
VSS	K4
VSS	L11
VSS	L12
VSS	L13
VSS	L14
VSS	L15
VSS	L16
VSS	L2
VSS	L22
VSS	L25
VSS	L6
VSS	M11
VSS	M12
VSS	M13
VSS	M14
VSS	M15
VSS	M16
VSS	M4
VSS	N11
VSS	N12
VSS	N13
VSS	N14
VSS	N15

Signal Name	Ball #
VSS	N16
VSS	N2
VSS	N23
VSS	N6
VSS	P11
VSS	P12
VSS	P13
VSS	P14
VSS	P15
VSS	P16
VSS	P24
VSS	P4
VSS	R11
VSS	R12
VSS	R13
VSS	R14
VSS	R15
VSS	R16
VSS	R2
VSS	R23
VSS	R25
VSS	R6
VSS	T11

Signal Name	Ball #
VSS	T12
VSS	T13
VSS	T14
VSS	T15
VSS	T16
VSS	T21
VSS	T4
VSS	U2
VSS	U7
VSS	V20
VSS	V22
VSS	V4
VSS	V6
VSS	W2
VSS	W23
VSS	W25
VSS	W7
VSS	Y10
VSS	Y4
VSS	Y6
VSS	Y8
VSSBA	E22
VSSDA	Y19

Signal Name	Ball #
VSSDACA	AE25
VSSDACA	AF24
VSSDPLL	K7
VSUS_3.3	B11
VSUS_3.3	B14
VSUS_3.3	B19
VSUS_3.3	B2
VSUS_3.3	B22
VSUS_3.3	B25
VSUS_3.3	B5
VSUS_3.3	B8
VSUS_3.3	E2
VSUS_3.3	F10
VSUS_3.3	F14
VSUS_3.3	F17
VSUS_3.3	G19
VSUS_3.3	G6
VSUS_3.3	G8
VSUS_3.3	H2
VSUS_3.3	H5
VSUS_3.3	H7
VSYNC	AF22
WBF#	AB24

5.2. GMCH2-M Package Dimensions

This specification outlines the mechanical dimensions for the Intel® 815EM chipset GMCH2-M. The package is a 544 ball grid array (BGA).

Figure 13. GMCH2-M GMCH BGA Package Dimensions (Top and Side Views)

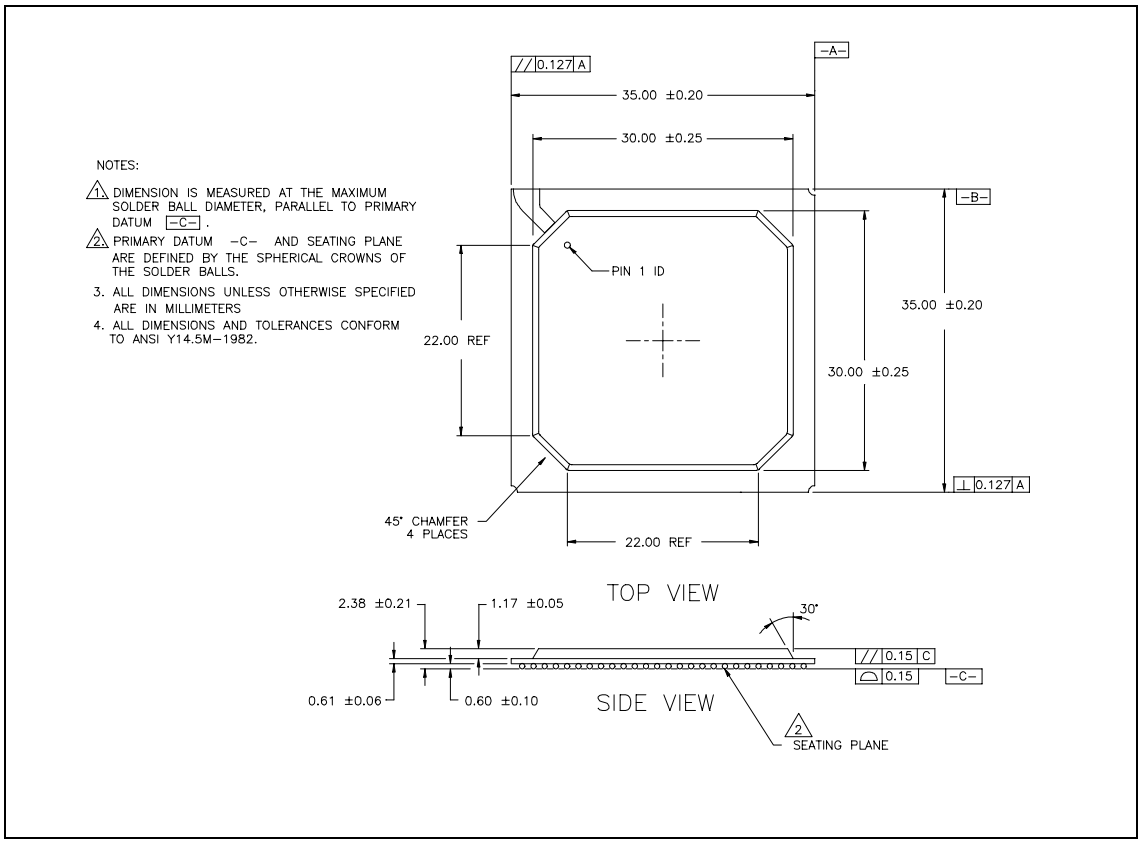
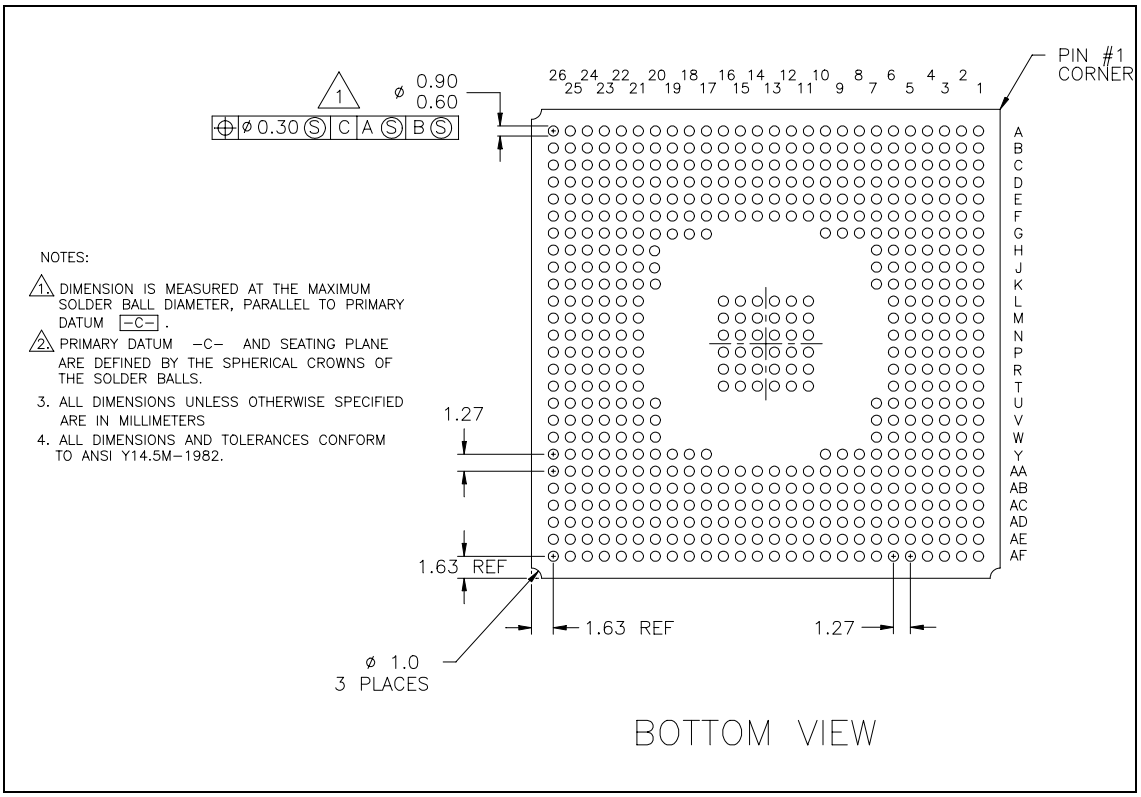


Figure 14. Intel® 815EM Chipset GMCH2-M BGA Package Dimensions (Bottom View)



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6. Testability

6.1. XOR Chain

XOR Chain testing is not supported on the Intel® 815EM Chipset.

6.2. All Z

On a system board in order to be able to apply vectors to XOR chains other chips on the board must be tristated to allow for this vector application. This is a feature that enables all GMCH2-M outputs to be tristated when ICH2-M is in the XOR chain mode. This mode can also be activated using the assigned reset strap.