Intel® 855PM Chipset Memory Controller Hub (MCH) DDR 200/266/333 MHz

Specification Update

September 2003

Notice: The Intel® 855PM chipset may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

Document Number: 253488-002

Contents

Revision History

Revision	Description	Date
-001	Initial release.	July 2003
-002	Updates include: • Added Component Rev ID via Programming table • Added Errata 5 Intel® 855PM MCH Themal Sensor Accuracy	September 2003

Preface

This document is an update to the specifications contained in *Intel® 855PM Chipset Memory Controller Hub (MCH) DDR 200/266 MHz Datasheet*. The Intel 855PM chipset memory controller hub (MCH) will support 333-MHz DDR beginning with the B1 stepping of the product. In addition to documentation changes and errata pertinent to all steppings of the Intel 855PM chipset MCH, this document includes changes to the datasheet for supporting 333-MHz DDR. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Errata may cause the Intel 855PM chipset behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Component Identification via Programming Interface

The Intel® 855PM chipset MCH may be identified by the following register contents.

Stepping	Vendor ID[1]	Device ID[2]	Revision Number[3]
A3	8086h	3340h	03h
B1	8086h	3340h	21h

NOTES:

1. The Vendor ID corresponds to bits 15-0 of the Vendor ID Register located at offset 00-01h in the PCI function 0 configuration space.
2. The Device ID corresponds to bits 15-0 of the Device ID Register located at offset 02-03h in the PCI function 0 configuration space.
3. The Revision Number corresponds to bits 7-0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space.

Indentification Markings

Stepping	S-Spec	Top Marking	Notes
A3	SL6TJ	RG82855PM	Production
B1	SL752	RG82855PM	333 MHz DDR Support

Summary Tables of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the listed MCH steppings. Intel intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Erratum, Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Status

Doc:	Document change or update that will be implemented.
PlanFix:	This erratum may be fixed in a future of the product.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Shaded:	This item is either new or modified from the previous version of the document.

ERRATUM NUMBER	Stepping		ERRATA
	A3	B1	
1	X	X	Intel 855PM MCH issues a pre-charge command (PRE) when Precharge-all command (PCALL) is called.
2	X	X	Intel 855PM MCH CLK (SCK#) signal comes 1-2 clocks after CKE goes active during resume from suspend (S3 and S1-M). This is a violation of the JEDEC spec requirement.
3	X	X	Intel 855PM MCH memory interface may not drive the memory address line MA8 according to JEDEC spec during the Mode Register Set Operation within the memory initialization sequence
4	X	X	Intel 855PM MCH memory interface may drive the memory address signals MA[13:9] high during the mode register set operation.
5	X	X	Intel® 855PM MCH Themal Sensor Accuracy

NO.	SPECIFICATION CHANGES
1	855PM B-step Changes to Section 1
2	855PM B-step Register Changes

NO.	SPECIFICATION CLARIFICATIONS
	There are no Specification Clarifications in this Specification Update revision

NO.	DOCUMENTATION CHANGES
1	Drive Strength Registers Correction

Errata

1. Intel 855PM MCH Initialization Issue

Problem: During the memory initialization sequence in the BIOS, Intel 855PM MCH could issue a pre-charge command (PRE) instead of a precharge-all command (PCALL). The behavior is observed during initialization sequence only if the PCALL command is issued through the BIOS code and can be verified only if the memory interface signals are probed. This behavior is a deviation from the JEDEC recommended sequence.

Implication: There is no functional impact from this behavior.

Workaround: The workaround exists in the memory init code and ensures that the PCALL command is issued correctly. When memory interface signals are probed during the initialization sequence with the workaround code both precharge to single banks and precharge-all operations may be observed.

Status: Closed. A BIOS workaround has been developed to resolve this behavior.

2. Intel 855PM MCH Clock JEDEC Spec Violation

Problem: The Intel 855PM MCH CLK(SCK#) signal comes 1-2 clocks after CKE goes active during resume from suspend. This is not the expected behavior based on the JEDEC spec requirement. JEDEC Spec requires that CLK (SCK#) is stable before CKE goes active.

Implication: No functional failure modes have been identified or reported.

Workaround: BIOS workaround during the S3/S1-M resume path will ensure that a few memory clocks before the DRC register is restored. The procedure is, write a “1” to bit 16 of the DRC register. Restore all MCH register in normal order ensuring the DRC register bit 16 is still set to 1. After memory register are restored, clear DRC bit 16.

Status: Closed. A BIOS workaround has been developed to resolve this behavior.

3. Intel 855PM MCH Mode Register Set Operation JEDEC Spec Violation with MA8

Problem: Under certain conditions, the Intel 855PM chipset memory interface may not drive the memory address line MA8 according to JEDEC spec during the Mode Register Set Operation within the memory initialization sequence.

Implication: No functional failure modes have been identified or reported.

Workaround: A new BIOS algorithm has been implemented to resolve the JEDEC spec violation. Contact your Intel Field Representative for more information.

Status: Closed. A BIOS workaround has been developed to resolve this behavior.

4. Intel 855PM MCH Mode Register Set Operation JEDEC Spec Violation with MA[13:9]

Problem: Under certain conditions, the Intel 855PM chipset memory interface may drive the memory address signals MA[13:9] high during the mode register set operation.

Implication: No functional failure modes have been identified or reported.

Workaround: A new BIOS algorithm has been implemented to resolve the JEDEC spec violation. Contact your Intel Field Representative.

Status: Closed. A BIOS workaround has been developed to resolve this behavior.

5. Intel® 855PM MCH Thermal Sensor Accuracy

Problem: The Intel® 855PM MCH internal thermal sensor may report the die temperature inaccurately.

Implication: When running high stress applications in an elevated ambient temperature, the system BIOS could prematurely initiate hardware throttling or a system halt leading to unpredictable system behavior.

Workaround: Disable the Intel® 855PM MCH internal thermal sensor in BIOS. The thermal sensor is disabled when the Thermal Sensor Enable (TSE) bit in the Thermal Sensor Control Register (TSCR) is a 0. The TSE bit is Device #1, offset 60h, bit [7].

For alternative thermal protection of the Intel® 855PM MCH, Intel recommends enabling bandwidth throttling in both the DRTC (DRAM Read Throttling Control Register) and the DWTC (DRAM Write Throttling Control Register). Refer to the *Intel® 855PM Chipset Memory Controller Hub (MCH) DDR 200/266 MHz Datasheet* for descriptions of these registers.

Status: Closed.

Specification Changes

1. 855PM B-Step Changes to Section 1

The following subsections represent modifications/differences from Section 1 of the *Intel® 855PM Chipset MCH DDR 200/266 MHz Datasheet*. Only the areas that have been modified are included.

1.3 System Architecture

The system architecture of the Intel 855PM chipset (B-step) is identical in features to the Intel 855PM chipset with the additional support for PC2700 DDR.

- Up to 2.0 GB (with 512-Mb stacked memory technology and two SO-DIMMs) of PC1600/2100/2700 DDR with ECC or without ECC.

1.5 DRAM Interface

The Intel 855PM chipset (B-step) memory controller directly supports one channel of PC1600/2100/2700 SO-DIMM DDR memory. The Intel 855PM chipset (B-step) memory interface supports the same DDR devices supported by the Intel 855PM chipset.

Table 1. DDR Memory Capacity

Technology	Width	System Memory Capacity	System Memory Capacity with Stacked Memory
64 Mb	16	128 MB	256 MB
128 Mb	16	256 MB	512 MB
256 Mb	16	512 MB	1 GB
512 Mb	16	1 GB	2 GB
64 Mb	8	128 MB	256 MB
128 Mb	8	256 MB	512 MB
256 Mb	8	512 MB	1 GB
512 Mb	8	1 GB	2 GB

1.8 MCH Clocking

The maximum memory bandwidth for the Intel 855PM chipset (B-step) is 1.6 GB/s with DDR 200 MHz, 2.13 GB/s with DDR 266 MHz, 2.66 GB/s with DDR 333 MHz. The following tables indicate the frequency ratios between the various interfaces that the MCH supports.

Table 2. MCH Clock Ratio Table

Interface	Speed	CPU System Bus Frequency Ratio
System Memory	DDR 200 MHz	1:1 Synchronous
	DDR 266 MHz	3:4 Synchronous
	DDR 333 MHz	3:5 Synchronous
AGP	66 MHz	Asynchronous
Hub interface	66 MHz	Asynchronous

2. Intel 855PM Chipset B-Step Register Changes

The registers contained in the following subsections represent modifications/differences made from the Intel 855PM chipset component register descriptions. Only the bit fields that have been modified are included. Please refer to the *Intel® 855PM chipset Memory Controller Hub (MCH) DDR 200/266 MHz Datasheet* for all other register descriptions.

The following table summarizes the registers that have been modified with the Intel 855PM chipset (B-step).

Table 3. Registers Modified for the Intel 855PM Chipset (B-step)

Address	Device	Register
80-81h	#0	DRDCTL – DRAM Read Timing Control Register
83h	#0	DQSDLY – DQS Control Register
C6-C7h	#0	MCHCFG – MCH-M Configuration Register
E4h	#0	CAPID – Product Specific Capability Identifier
58h	#1	DRTC – DRAM Read Throttle Control Register

3.7.21 DRDCTL – DRAM Read Timing Control Register – Device #0

Offset: 80-81h
Default: 0000h
Access: Read/Write
Size: 16 bits

Bit	Description
3:2	**RCVEN/RDCLK Quarter-Clock Timing Control.** This field selects the number of 200 MHz/266 MHz/333 MHz phase delays that is added in the RCVEN output path. This delay is added serially to the 10/7.5/6.0 ns delay which is programmed in bits[1:0]. 00: 5.0 ns / 3.75 ns / 3.0 ns 01: 7.5 ns / 5.625 ns / 4.5 ns 10: 10.0 ns/ 7.5 ns / 6.0 ns 11: 12.5 ns/ 9.375 ns / 7.5 ns This bit field is programmed by BIOS, based on CAS latency.
1:0	**RCVEN/RDCLK Timing Control** This field selects the number of 100 MHz / 133 MHz / 166 MHz clock delays from the rising edge of the clock to which READ command is driven to the internal clock of which RCVEN output is driven. 00: 1 clocks (10/7.5/6.0 ns) 01: 2 clocks (20/15/12 ns) 10: 3 clocks (30/22.5/18 ns) This bit field will be set by BIOS based on SO-DIMM configurations (including CAS latency).

3.7.23 DQSCTL – DQS Control Register – Device #0

Offset: 83h
Default: 0Ah
Access: Read/Write
Size: 8 bits

Bit	Description
4:0	**DQS Delay (DQSDLY)**: This five-bit field specifies the delay which will be added to DQS so that read data has sufficient setup and hold time. This field affects DQS on reads only. The DDR DRAMs drive data for MCLK Period / 2 (5 ns for DDR 200 MHz, 3.75 ns for DDR 266 MHz, 3 ns for DDR 333 MHz). DQS edges are driven at the same time as data is driven. Therefore DQS must be delayed by some amount so that it can be used to sample DQ. Valid values for this field are 00000-00111. All other values are reserved.

3.7.41 MCHCFG – MCH Configuration Register – Device #0

Offset: C6-C7h
Default: 0001h
Access: Read/Write Once, Read/Write, Read Only
Size: 16 bits

Bit	Description
11:10	**System Memory Frequency Select:** These bits must be programmed prior to memory initialization. DDR 333 MHz is supported only by Intel 855PM chipset (B-step) with Rev ID >=20 **Intel 855PM Chipset (B-step)** 00: 100 MHz (Set for DDR 200 MHz) 01: 166 MHz (Set for DDR 333 MHz) 10: 133 MHz (Set for DDR 266 MHz) 11: Reserved
9:6	**Reserved**

3.7.48 CAPID – Product Specific Capability Identifier– Device #0

Offset: E4h
Default: F104A009h
Access: Read Only
Size: 32 bits

Bit	Description
31	**Enhanced 855PM (B-step) MCH Support** 1 = Component is Intel 855PM chipset, capable of supporting 200/266 MHz DDR. 0 = Component is Intel 855PM chipset (B-step), capable of supporting 200/266/333 MHz DDR.

3.8.24 DRTC – DRAM Read Throttle Control Register – Device #1

Address Offset: 58-5Fh
Default Value: 0000_0000_0000_0000h
Access: Read/Write/Lock
Size: 64 bits

Bit	Description
63:50	**Reserved**
49	**Throttling Counters Per Row Feature Enable:** When set to 0, all DRAM reads are counted together in one counter. When set to 1, DRAM reads for different memory rows are counted in different counters. Read throttling mode is also per-row. **This feature is available only if CAPID[31]=0. Otherwise this bit is reserved.**

Specification Clarifications

There are no specification clarifications in this Specification Update revision.

Documentation Changes

1. Drive Strength Registers Correction

In these sections:

3.6.5 CKESTR – Strength Control Register for CKE Signal Group

3.6.6 CSBSTR – Strength Control Register for CS# Signal Group

3.6.7 CKSTR – Strength Control Register for CK Signal Group (CK/CK#)

Replace the sentence:

The actual strength used for each signal is determined by the Width Select register (offset 4Dh).

With:

The configuration is determined by the DRAMWIDTH register (offset 2Ch).