Intel® Pentium® 4 Processor in 478-pin Package and Intel® 845 Chipset Platform for SDR

Design Guide Update

March 2004

Notice: The Intel® 845 chipset family may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in the Specification Update.

Document Number: 250425-003

Contents

Revision History

Rev.	Draft/Changes	Date
-001	Initial Release	March 2002
-002	(1) Added Documentation Change #3, Replace Figure 118, Intel® 845 Chipset Platform Using PC133 SDRAM System Memory Power Delivery Map (2) Added Documentation Change #4, Added Section 4.6.7, Electrostatic Discharge Platform Recommendations (3) Added Documentation Change #5, Change Table 3, System Bus Routing Summary for the Processor (4) Added Documentation Change #6, Add Section 13.2, Intel® Boxed Processor Mechanical Keep-Outs (5) Added Documentation Change #7, Add Section 15.1.3, Intel® Boxed Processor Mechanical Keep-Outs (6) Added Schematic, Layout, and Routing Updates #1, Schematic change to the 82845 MCH HSWING Circuit	May 2002
-003	(1) Added Documentation Change 8, Revise Section 4.1, Schematic Checklist, Host Interface, PWRGOOD	March 2004

Preface

This Design Guide Update document is an update to the specifications and information contained in the *Intel® Pentium® 4 Processor in 478-pin Package and Intel® 845 Chipset Platform for SDR Design Guide*, January 2002. This Design Guide Update may reference other documents listed in the following Affected Documents/Related Documents table. This document is a compilation of updates to the general design considerations; schematic, layout, and routing updates; and documentation changes. This document is intended for hardware system manufacturers and for software developers of applications, operating systems, and tools. The design guide (and this design guide update) is primarily targeted at the PC market segment and was first published in 2002. Those using this design guide and update should check for device availability before designing in any of the components included in this document.

Information types defined in the Nomenclature section of this document are consolidated into the public design guide update document when the public design guide document is first published. This design guide update document contains a complete list of all known information types.

Affected Documents

Document Title	Document Number
Intel® Pentium® 4 Processor in 478-pin Package and Intel® 845 Chipset Platform for SDR Design Guide, January 2002	298354-002

Related Documents

Document Title	Document Number
Intel® 845 Chipset: 82845 Memory Controller Hub (MCH) for SDR Datasheet, January 2002	290725-002
Intel® 82801BA (ICH2) I/O Controller Hub Datasheet	290687-002

Nomenclature

General Design Considerations include system level considerations that the system designer should account for when developing hardware or software products using the Intel® 845 Chipset: 82845 Memory Controller Hub (MCH) for SDR.

Schematic, Layout, and Routing Updates include suggested changes to the current published schematics or layout, including typos, errors, or omissions from the current published documents.

Documentation Changes include suggested changes to the current published design guide not including the above.

Codes Used in Summary Table

Doc: Document change or update that will be implemented.

Shaded: This item is either new or modified from the previous version of the document.

NO.	Plans	GENERAL DESIGN CONSIDERATIONS
		There are no General Design Consideration changes in this Design Guide Update revision.

NO.	Plans	SCHEMATIC, LAYOUT, AND ROUTING UPDATES
1	Doc	Schematic change to the 82845 MCH HSWING Circuit

NO.	Plans	DOCUMENTATION CHANGES
1	Doc	Change Section 12.4.2, 3.3V/V5REF Sequencing
2	Doc	Change Section 14.8, Power and Ground, V5REF_SUS
3	Doc	Replace Figure 118, Intel® 845 Chipset Platform Using PC133 SDRAM System Memory Power Delivery Map
4	Doc	Add Section 4.6.7, Electrostatic Discharge Platform Recommendations
5	Doc	Change Table 3, System Bus Routing Summary for the Processor
6	Doc	Add Section 13.2, Intel® Boxed Processor Mechanical Keep-Outs
7	Doc	Add Section 15.1.3, Intel® Boxed Processor Mechanical Keep-Outs
8	Doc	Revise Section 14.1, Schematic Checklist, Host Interface, PWRGOOD

General Design Considerations

There are no General Design Considerations in this Design Guide Update revision.

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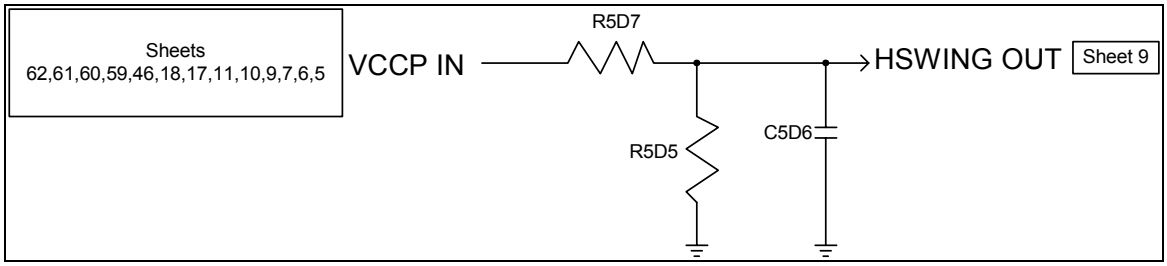
Schematic, Layout, and Routing Updates

1. Schematic Change to the 82845SDR MCH HSWING Circuit

Reference Appendix A, Customer Reference Board Schematics, of the Intel® Pentium® 4 Processor in 478-Pin Package and Intel® 845 Chipset Platform for SDR Design Guide, 298354-002, dated January 2002. Sheet 11 of the "Intel® 845 SDR Schematics Rev 1.3" contains a circuit at grid location C-7. This circuit has a VCCP input and an HSWING output. Capacitor C5D6 is shown as a series capacitor between VCCP and the HSWING output. This circuit is not correct as shown.

Capacitor C5D6 is a decoupling capacitor. It should connect the HSWING output of this circuit to GND so that resistor R5D5 and capacitor C5D6 are in parallel.



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Documentation Changes

1. Changed: Change Section 12.4.2, 3.3V/V5REF Sequencing

Change the third paragraph to read:

As an additional consideration, during suspend, the only signals that are 5 V tolerant capable are USB OC:[3:0]#. If these signals are not needed during suspend, V5REF_SUS can be connected to either VccSus3_3 or 5 V_Always/5V_AUX. If OC:[3:0]# is needed during suspend and 5 V tolerance is required then V5REF_SUS should be connected to 5V_Always/5V_AUX, but if 5 V tolerance is not needed in suspend, then V5REF_SUS can be connected to either VccSus3_3 or 5V_Always/5V_AUX rails.

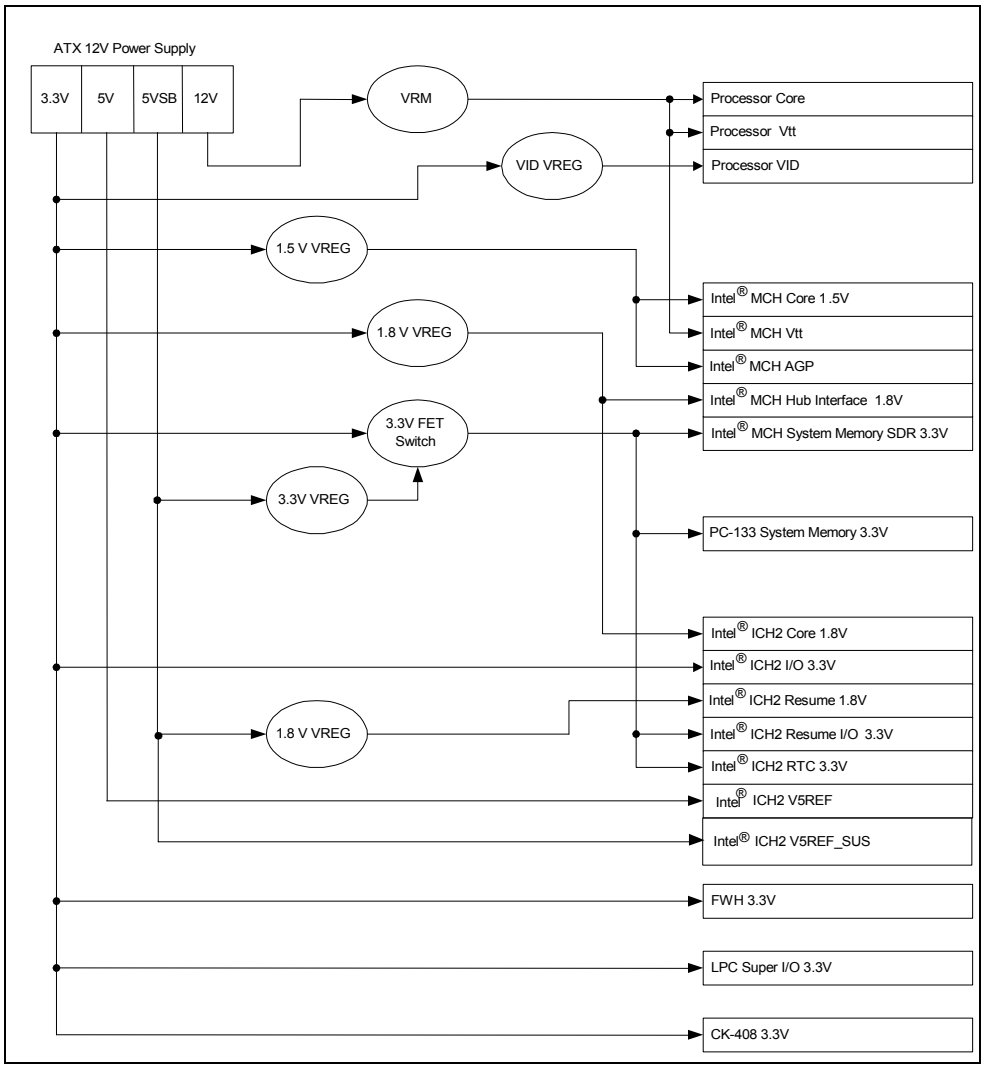
2. Changed: Change Section 14.8, Power and Ground, V5REF_SUS

Change the second bullet in the description of V5REF_SUS to read:

- V5REF_SUS only affects 5 V-tolerance for USB OC:[3:0]# pins and can be connected to either VccSUS3_3 or 5V_Always/5V_AUX if 5V tolerance on these OC:[3:0]# is not needed. If 5V tolerance on OC:[3:0]# is needed then V5REF_SUS USB must be connected to 5V_Always/5V_AUX which remains powered during S5.

3. Replaced: Replace Figure 118, Intel® 845 Chipset Platform Using PC133 SDRAM System Memory Power Delivery Map

Figure 118, Intel® 845 Chipset Platform Using PC133 SDRAM System Memory Power Delivery Map, in Section 12.2, is replaced with the following new Power Delivery Map:



4. Electrostatic Discharge Platform Recommendations

The following new material is added as Section 4.6.7, Electrostatic Discharge Platform Recommendations:

4.6.7 Electrostatic Discharge Platform Recommendations

Electrostatic discharge (ESD) into a system can lead to system instability, and possibly cause functional failures when a system is in use. There are system level design methodologies that when followed can lead to higher ESD immunity. Electromagnetic fields due to ESD are introduced into a system through chassis openings such as the I/O back panel and PCI slots. These fields can introduce noise into signals and cause the system to malfunction. One can reduce the potential for issues at the I/O area by adding more ground plane on the motherboard around the I/O area. This can lead to a higher ESD immunity.

Intel recommends that the I/O area on the top and bottom signal layers of a 4-layer motherboard near the I/O back panel be filled with a ground fill as shown in Figures 1-4. In addition, a ground fill cutout should be placed on the Vcc layer in the area where the ground fill is done on the top and bottom layers. Intel recommends filling the I/O area as much as possible without effecting the signal routing. The board designer should fill the entire I/O area along the board edge.

The spacing from the ground fill to other shapes/traces should be at least 20 mils. It is recommended that these ground fill areas be connected to two chassis mounting holes (as seen in Figure 2). This will allow ESD current to travel to the chassis instead of the board. Ground stitching vias should be placed throughout the entire ground fill if possible. It is important that the vias are placed along the board edge. Ground stitching vias for the ground fill should be 100-150 mils apart or less.

In conclusion, Intel recommends the following:

- Fill the I/O area with the ground fill in all layers including signal layers whenever possible
- Extend the ground fill along the entire back I/O area
- Connect the ground fill to mounting holes
- Place stitching vias 100-150 mils apart in the entire ground fill

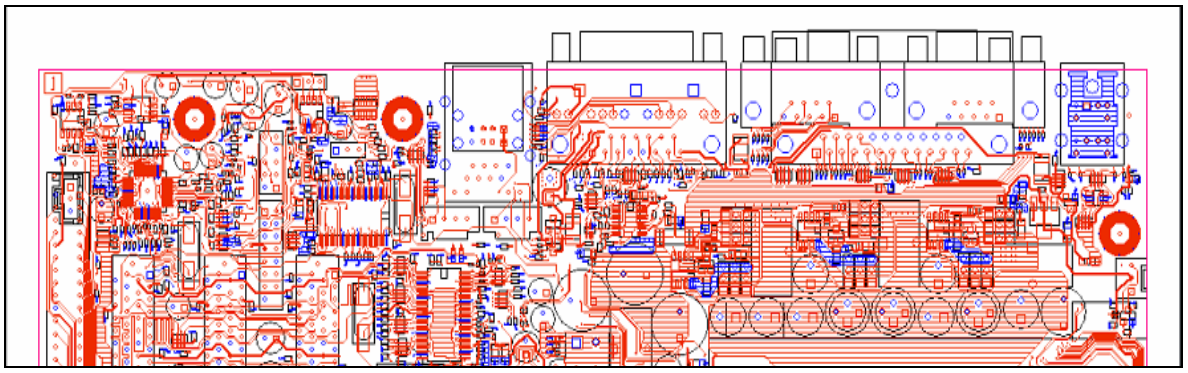


Figure 1, Top signal layer before the ground fill near the I/O area

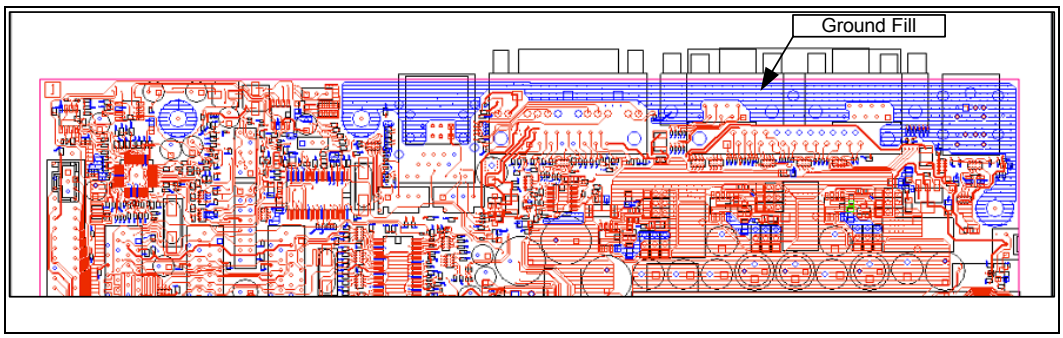


Figure 2, Top signal layer after the ground fill near the I/O layer

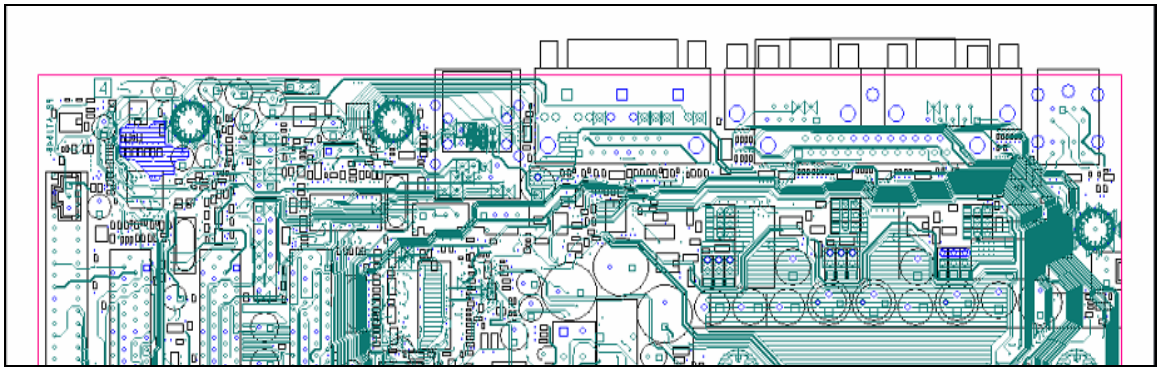


Figure 3, Bottom signal layer before the ground fill near the I/O area

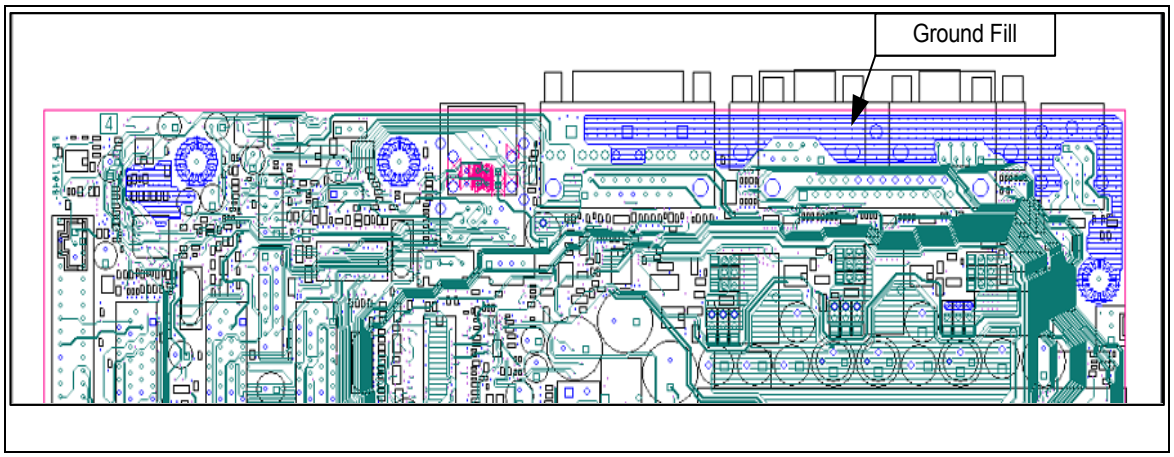


Figure 4, Bottom signal layer after the ground fill near the I/O area

5. Change Table 3, System Bus Routing Summary for the Processor

Reference Table 3, System Bus Routing Summary for the Processor, in Section 4.1. The parameter “Clock keep out zones” is changed as shown:

Clock keep out zones	Refer to Table 55, BCLK [1:0]# Routing Guidelines, of this Design Guide.

6. Add Section 13.2, Intel® Boxed Processor Mechanical Keep-Outs

The following new section is added:

13.2 Intel® Boxed Processor Mechanical Keep-Outs

Verify Intel’s Boxed Processor mechanical keep-outs are marked and visible during board layout. This keep-out zone should be considered during chassis selection.

7. Add Section 15.1.3, Intel® Boxed Processor Mechanical Keep-Outs

The following new section is added:

15.1.3 Intel® Boxed Processor Mechanical Keep-Outs

Checklist Item	
Intel® Boxed Processor Mechanical Keep-Outs	
• Verify Intel's Boxed Processor mechanical keep-outs are marked and visible during board layout. This keep-out zone should be considered during chassis selection.	

8. Revise Section 14.1, Schematic Checklist, Host Interface, PWRGOOD

Revise Section 14.1, Schematic Checklist, Host Interface, PWRGOOD with the following:

Signal	Description
Processor/Intel® ICH2 Signals	
PWRGOOD	Connects to ICH2 CPUPWRGD pin. Note that a weak pullup to V_CPU_IO is required and that such value should not exceed ICH2s Ioh2/Iol2 specs.