PDC20630

Code name: VG4
Manufacturer: Promise Technology, Inc., in 1994 - 1995
Function: VESA Local Bus IDE controller
Features
- one fixed IDE channel
- speed settable by jumpers to 2, 4, 6
- Multiword DMA 2 support
- IORDY support

Used in: Promise EIDE2300 and EIDE2300plus controllers and by various OEMs (Kentech): .
Manufacturer support: none.
Documentation available: none.
Drivers available: DOS, Win 3.1x, Win 95, WinNT 3.x, Netware 386 3.1x, 4.01, OS/2 2.0, 2.1x, SCO Unix 3.2.X, AT&T UNIX SVR 4.0

Note: DMA transfer is between disk and PDC20630 only, for transfer from PDC20630 to computer standard ins/outs are used.

This chip can be detected by the same sequence as PDC20230-C

```
inb (0x1F5);
outb (inb (0x1F2) | 0x80, 0x1F2);
cli ();
inb (0x1F2);
inb (0x3F6);
inb (0x3F6);
inb (0x1F2);
inb (0x1F2);
sti ();
if (inb (0x1F2) & 0x80)
    printf ("Chip is not PDC20230-C nor PDC20630");
else
    printf ("Chip is PDC20230-C or PDC20630");
```

PDC20630 clears highest bit of sector count register after this sequence.
This sequence switches PDC20630 chip to programming mode. In programming mode, following registers have special meaning:

Register 1F3 - speed settings
bit 7 - unknown, set to 1 for speed setting 7 of device 0 or 1.
bit 6 - VL bus clock, 0 means > 33 Mhz, 1 means <= 33 MHz ?? allowed only for device 0 speed 7
bit 3,4,5 - speed setting of device 0 (master), 0 to 7
bit 0,1,2 - speed setting of device 1 (slave), 0 to 7

After reset, lowest 3 bits of 1F3 registers contains speed setting set by jumpers (0, 2, 4, 6)

	bit 6 = 1	@ 33 MHz	bit 6 = 0	@ 50 MHz	
Speed	Clocks	Cycle Time	Clocks	Cycle Time	
0	21	630	31	620	PIO 0
1	20	600	28	560	
2	17	510	26	520	
3	16	480	25	500	
4	13	390	20	400	PIO 1
5	12	360	19	380	
6	9	270	15	300	
7	8	240	12	240	PIO 2

Register 1F4
bit 7 - set by set_speed routine to 1 for xx0=8
bit 6 - set by set_speed routine to 1 for xx1=8
bit 5 - set by set_transfer_mode for device 0 (IORDY support?)
bit 4 - set by set_transfer_mode for device 1 (IORDY support?)
bit 3 - 0/1 = disable/enable 0x1F8/0x1F9 registers
bit 2
bit 1
bit 0
Start of initialization sequece in DOS driver:
outb (inb (0x1F4) & 0x07, 0x1F4)

Writing new values ???

```
        somedelay ();
        outb (inb (0x1F2) | 0x01, 0x1F2);
        somedelay ();
        inb (0x1F5);
```
The somedelay is 100 loops in assembler code.

Register 1F5 - close programming mode
Reading from register 1F5 closes programming mode.

There are 8 additional registers accessed by ports 1F8 (index) and 1F9 (data). The access is enabled
by writing
outb (inb (0x1F4) | 0x08, 0x1F4)
and disabled by
outb (inb (0x1F4) & 0xF7, 0x1F4)

Register 0 - timing of device 0 (master)
Register 1 - timing of device 0 (master)
Register 2 - timing of device 1 (slave)

Register 3 - timing of device 1 (slave)
Register 4
Register 5
Register 6
Register 7 - status
bit 7
bit 6
bit 5
bit 4 - 1 = DMA error ?
bit 3
bit 2
bit 1 - 1 = DMA read completed ?
bit 0 - 1 = DMA write completed ?

port 1F8 read:
bit 7
bit 6
bit 5
bit 4
bit 3
bit 2 to bit 0 - selected register 0 to 7

In DOS driver is used command code 2 (outb(2,0x1F7) - I don't know the meanig.
In DOS driver is several times read port 0x101 - I don't know the meanig.

DOS driver for PDC20630 uses VLB sync sequence for 32-bit I/O, but it seems it works without it.

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updated 21-May-2000 by [Petr Soucek](#)