# ICE1232

## AC'97 2.1 VSR Audio Codec with 3D

*Preliminary*

## Features

- AC'97 2.1 compliant codec
- 18-bit stereo full duplex $\Sigma\Delta$ codec
- VSR (Variable Sampling Rate), 1Hz resolution
- 3D stereo expansion for simulated surround
- 4 stereo analog line-level inputs
- 2 mono analog line-level inputs
- MIC level input switchable from two sources
- Second line-level output with volume control
- Multiple codec mode
- External Audio Amplifier Control
- Power management support
- Low Power consumption mode
- Exceeds Microsoft® PC'9x requirements
- 3.3V, 5V or split analog/digital power supply
- 48-pin TQFP or LQFP package

## Description

IC Ensemble's ICE1232™ 18-bit $\Sigma\Delta$ audio codec conforms to the AC'97 2.1 specification with excellent analog performance. The ICE1232 integrates a sophisticated Sample Rate Converter that can be adjusted in 1Hz increments. This makes it ideal for host-based signal processing motherboard applications which lacks a hardware accelerator. The mixer circuitry integrates a stereo enhancement to provide a pleasing 3D surround sound effect for stereo media. This codec is designed with aggressive power management to achieve ultra low power consumption when used with a 3.3V supply. The primary applications for this part are desktop and portable personal computers multimedia subsystems. However, it is suitable for any system requiring audio domain conversion, mixing and volume control at competitive prices.
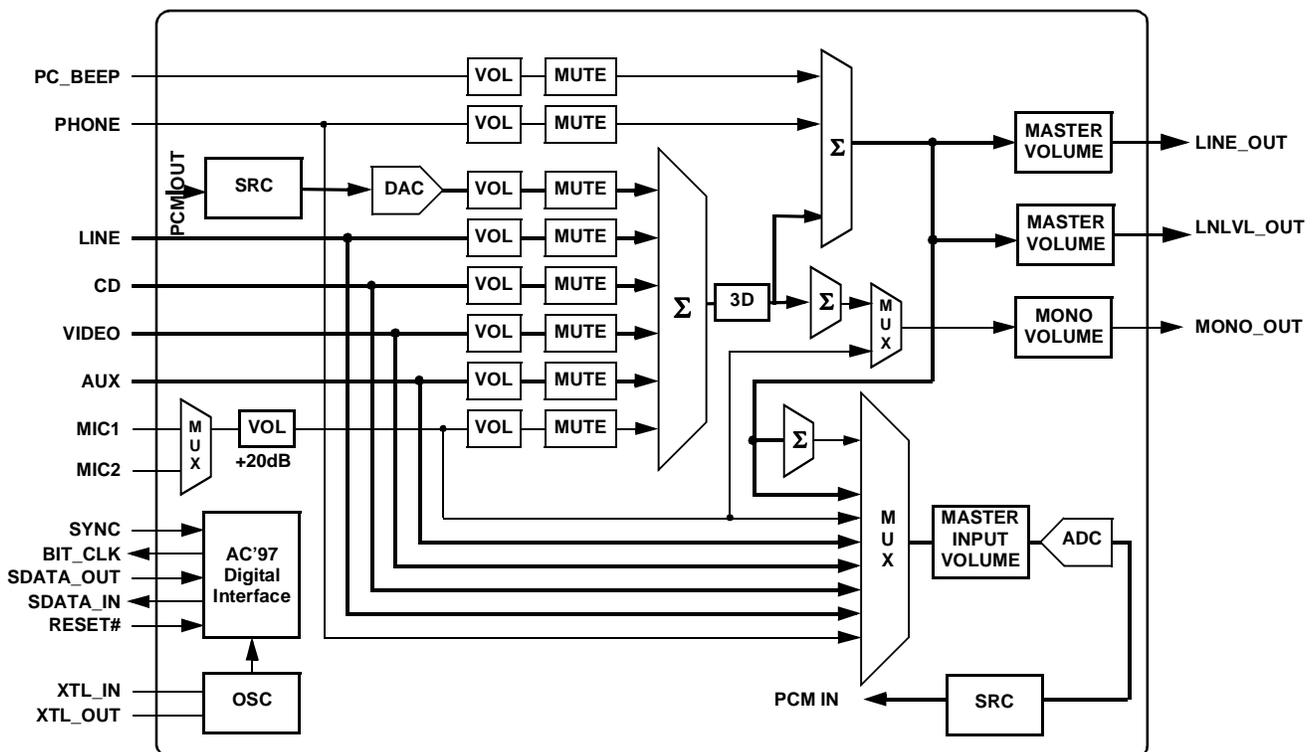


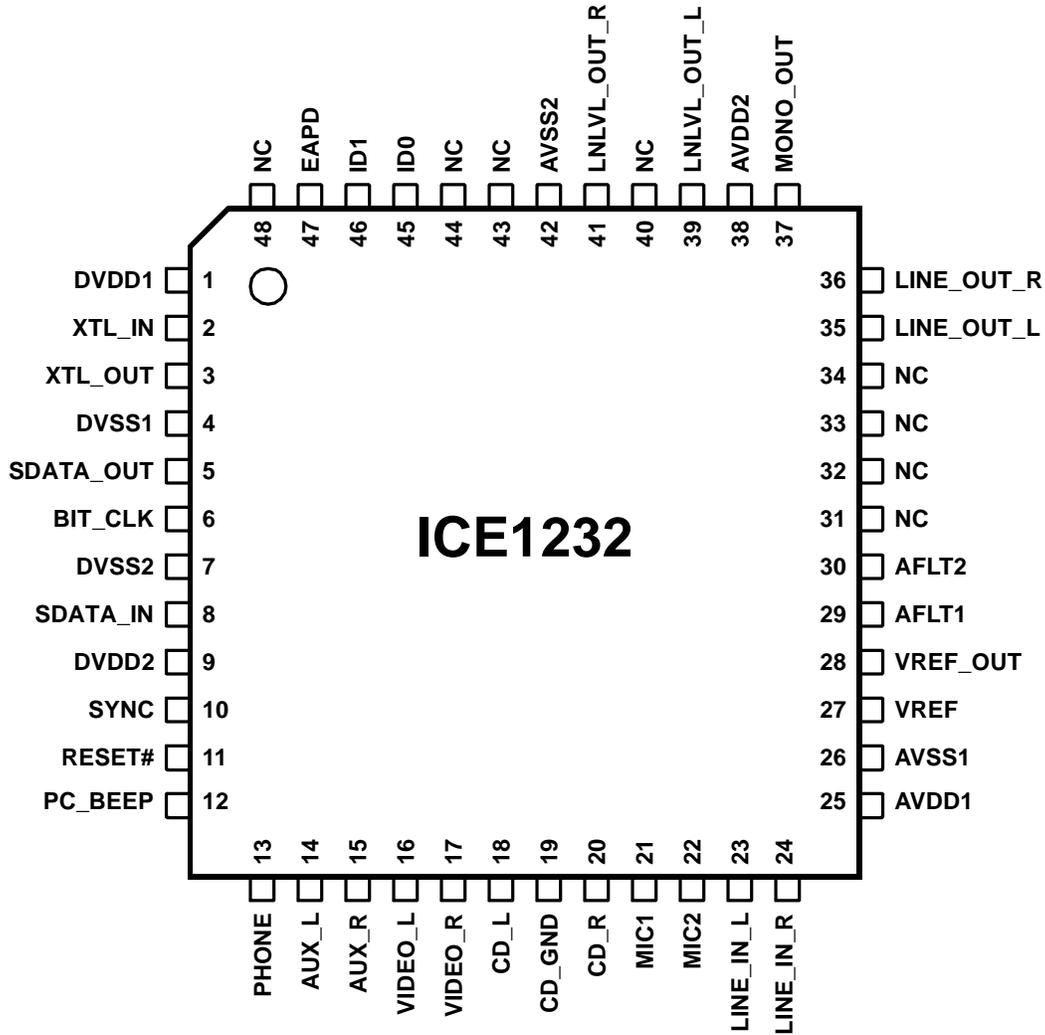**Figure 1. Functional Block Diagram**

Pin labels (top, left to right): NC (48), EAPD (47), ID1 (46), ID0 (45), NC (44), NC (43), AVSS2 (42), LNLVL_OUT_R (41), NC (40), LNLVL_OUT_L (39), AVDD2 (38), MONO_OUT (37)

Left side pins:
- DVDD1 — 1
- XTL_IN — 2
- XTL_OUT — 3
- DVSS1 — 4
- SDATA_OUT — 5
- BIT_CLK — 6
- DVSS2 — 7
- SDATA_IN — 8
- DVDD2 — 9
- SYNC — 10
- RESET# — 11
- PC_BEEP — 12

Center: **ICE1232**

Right side pins:
- 36 — LINE_OUT_R
- 35 — LINE_OUT_L
- 34 — NC
- 33 — NC
- 32 — NC
- 31 — NC
- 30 — AFLT2
- 29 — AFLT1
- 28 — VREF_OUT
- 27 — VREF
- 26 — AVSS1
- 25 — AVDD1

Bottom pins (13–24): PHONE (13), AUX_L (14), AUX_R (15), VIDEO_L (16), VIDEO_R (17), CD_L (18), CD_GND (19), CD_R (20), MIC1 (21), MIC2 (22), LINE_IN_L (23), LINE_IN_R (24)

**Figure 2.  48-pin TQFP/LQFP**

**Table 1. Pin Description**

| Pin # | Symbol | Type | Description |
|-------|--------|------|-------------|
| 1 | DVDD1 | P | Digital Supply Voltage, 5 or 3.3V. Match controller's Supply Voltage |
| 2 | XTL_IN | I | 24.576MHz Crystal or clock input |
| 3 | XTL_OUT | O | 24.576MHz Crystal |
| 4 | DVSS1 | P | Digital Ground |
| 5 | SDATA_OUT | I | AC'97 Serial Data Input Stream |
| 6 | BIT_CLK | I/O | 12.288MHz Serial Data Clock |
| 7 | DVSS2 | P | Digital Ground |
| 8 | SDATA_IN | O | AC'97 Serial Data Output Stream |
| 9 | DVDD2 | P | Digital Supply Voltage, 5 or 3.3V. Match controller's Supply Voltage |
| 10 | SYNC | I | 48kHz Fixed Rate Sync Pulse |
| 11 | RESET# | I | AC'97 Master Reset |
| 12 | PC_BEEP | I | PC Speaker Beep Pass Through |
| 13 | PHONE | I | Telephony Subsystem Speakerphone |
| 14 | AUX_L | I | Auxiliary Audio Left Channel |
| 15 | AUX_R | I | Auxiliary Audio Right Channel |
| 16 | VIDEO_L | I | Video Audio Left Channel |
| 17 | VIDEO_R | I | Video Audio Right Channel |
| 18 | CD_L | I | CD Audio Left Channel |
| 19 | CD_GND | I | CD Audio Analog Ground |
| 20 | CD_R | I | CD Audio Right Channel |
| 21 | MIC1 | I | Desktop Microphone |
| 22 | MIC2 | I | Second Microphone |
| 23 | LINE_IN_L | I | Line In Left Channel |
| 24 | LINE_IN_R | I | Line In Right Channel |
| 25 | AVDD1 | P | Analog Supply Voltage, 5V or 3.3V |
| 26 | AVSS1 | P | Analog Ground |
| 27 | VREF | I | Reference Voltage |
| 28 | VREFOUT | O | Reference Voltage Output |
| 29 | AFLT1 | O | Left Channel Anti-Aliasing Filter Capacitor |
| 30 | AFLT2 | O | Right Channel Anti-Aliasing Filter Capacitor |
| 31 | NC | – | No Connect |
| 32 | NC | – | No Connect |
| 33 | NC | – | No Connect |
| 34 | NC | – | No Connect |
| 35 | LINE_OUT_L | O | Line Out Left Channel |
| 36 | LINE_OUT_R | O | Line Out Right Channel |
| 37 | MONO_OUT | O | Mono Output |

**Table 1. Pin Description (*continued...*)**

| Pin # | Symbol | Type | Description |
|-------|--------|------|-------------|
| 38 | AVDD2 | P | Analog Supply Voltage, 5V or 3.3V |
| 39 | LNLVL_OUT_L | O | Alternate Left Line Level out |
| 40 | NC | – | No Connect |
| 41 | LNLVL_OUT_R | O | Alternate Right Line Level out |
| 42 | AVSS2 | P | Analog Ground |
| 43 | NC | – | No Connect |
| 44 | NC | – | No Connect |
| 45 | ID0 | I | Multiple Codec Select (Internal pull-up). *Please see **Table 19***. |
| 46 | ID1 | I | Multiple Codec Select (Internal pull-up). *Please see **Table 19***. |
| 47 | EAPD | O | External Power Amplifier Power Down |
| 48 | NC | – | No Connect |

**Note:** ICE1232 supports mixed +5V and +3.3V analog and digital power supply combinations. **You must use 3.3V as digital supply if the AC-link controller is also 3.3V**. For best analog performance use 5V analog supply. For maximum power savings use 3.3V for both analog and digital sections.
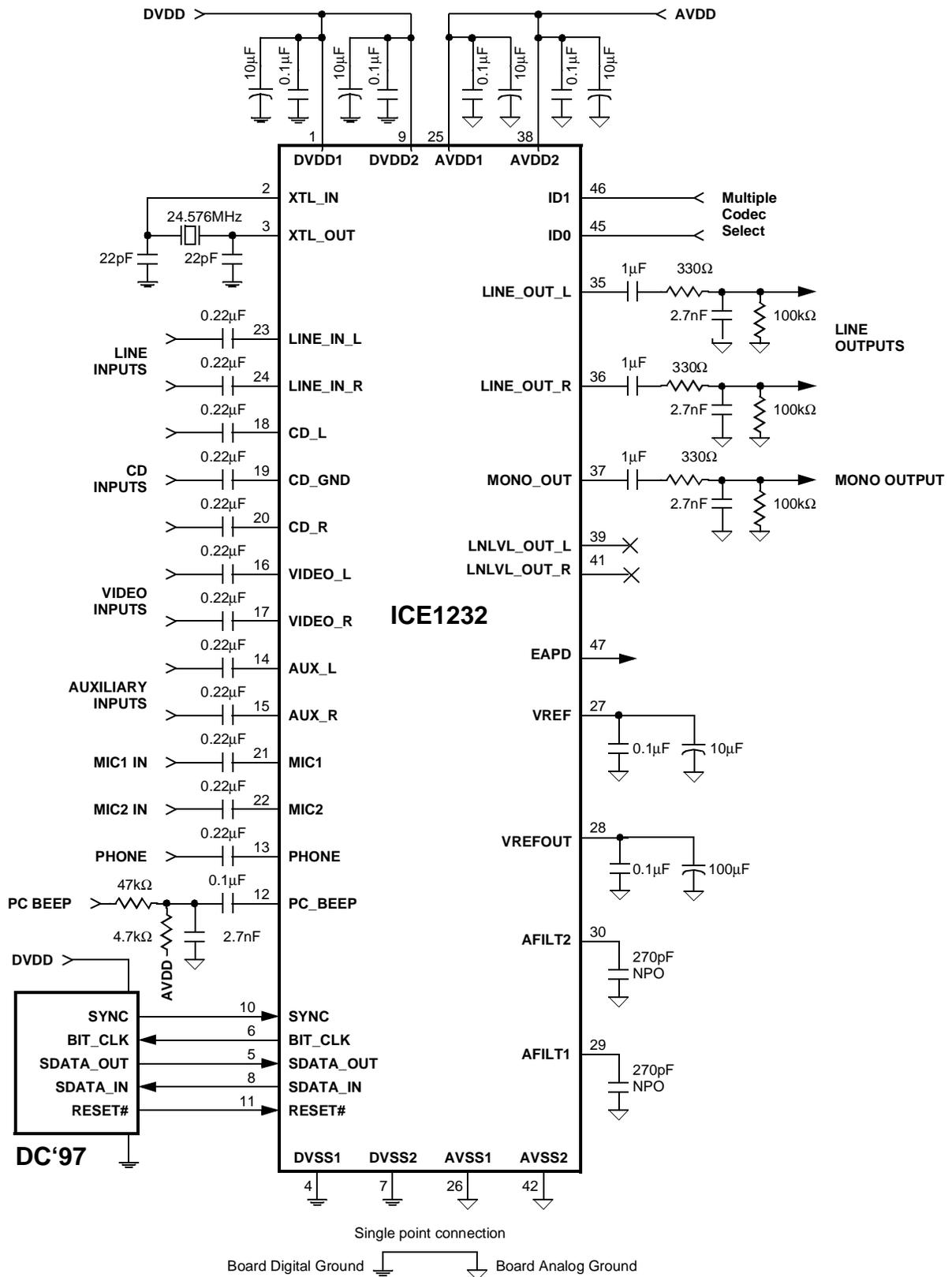
**Figure 3. Typical Connection Diagram**

# Absolute Maximum Ratings

### Table 2.  Absolute Maximum Ratings

( AVSS = DVSS = 0V)

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| – | Power Supplies (AVDD, DVDD) | -0.3 | | 6.0 | V |
| – | Input Current per Pin | -10 | | 10 | mA |
| – | Output Current per Pin | -15 | | 15 | mA |
| – | Digital Input Voltage | -0.3 | | DVDD+0.3 | V |
| – | Analog Input Voltage | -0.3 | | AVDD+0.3 | V |
| – | Total Power Dissipation | | | TBD | W |
| – | Ambient Temperature | -55 | | 110 | °C |
| – | Storage Temperature | -65 | | 150 | °C |

**Caution:**   Exceeding any of these limits can cause permanent failure of the device and will void any claims against product quality.

# Recommended Operating Conditions

### Table 3.  Recommended Operating Conditions

( AVSS = DVSS = 0V)

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| – | Digital Power Supplies (DVDD), preferred | 3.135 | 3.3 | 3.465 | V |
| – | Digital Power Supplies (DVDD), if controller 5V | 4.75 | 5 | 5.25 | V |
| – | Analog Power Supplies (AVDD), preferred | 4.75 | 5 | 5.25 | V |
| – | Analog Power Supplies (AVDD), for low power apps | 3.135 | 3.3 | 3.465 | V |
| – | Operating Ambient Temperature | 0 | | 70 | °C |

## Performance Specifications

### Table 4. Analog Performance Characteristics (+5V Power)

TA=25°C, AVDD = DVDD = 5.0V ± 5%; AVSS = DVSS =0V; 10kΩ / 50pF Load; FS = 48kHz, 0dB = 1VRMS; BW: 20Hz ~ 20kHz, 0dB Attentuation, IB[1:0]=00 (power up default), as measured on a 2-layers AMR eval card

| Symbol | Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | Full Scale Input Voltage: | Line Inputs | | 1.0 | | VRMS |
| | | Mic Inputs (20dB = 0) | | 1.0 | | VRMS |
| | | Mic Inputs (20dB = 1) | | 0.1 | | VRMS |
| | Full Scale Output Voltage: | Line Outputs | | 1.0 | | VRMS |
| | | Mono Output | | 1.0 | | VRMS |
| | Analog S/N: | CD to LINE_OUT | | 95 | | dB |
| | | Other to LINE_OUT | | 95 | | dB |
| | Analog Frequency Response | | 20 | | 20,000 | Hz |
| | Digital S/N: | DAC | 85 | 94 | | dB |
| | | ADC | 75 | 90 | | dB |
| | Total Harmonic Distortion: LINE_IN to LINE_OUT | | | -88 | -74 | dB |
| | (DA) DAC to LINE_OUT | | | -86 | -74 | dB |
| | D/A and A/D Frequency Response: | DAC | 20 | | 19,200 | Hz |
| | | ADC | 20 | | 19,200 | Hz |
| | Transition Band: | DAC | 19,200 | | 28,800 | Hz |
| | | ADC | 19,200 | | 28,800 | Hz |
| | Stop Band: | DAC | 28,800 | | infinity | Hz |
| | | ADC | 28,800 | | infinity | Hz |
| | Stop Band Rejection: | DAC | 75 | | | dB |
| | | ADC | 75 | | | dB |
| | Out-of-Band Rejection | | | -40 | | dB |
| | Group Delay | | | | 1 | ms |
| | Power Supply Rejection Ratio (1kHz) | | | -40 | | dB |
| | Input Channel Crosstalk | | | | -70 | dB |
| | Spurious Tone Reduction | | | -100 | | dB |
| | Attenuation, Gain Step Size | | | 1.5 | | dB |
| | Input Impedance | | 10 | 45 | | kΩ |
| | Input Capacitance | | | 15 | | pF |
| | VREFOUT | | 2.0 | 2.4 | 2.8 | V |

**Note:** VIL = 0.8V, VIH = 2.0V

Analog Frequency Response has ±1dB limits

SNR (measured as THD+N) of rms output level with 1kHz full-scale input to rms output level with all zeros into digital input

Measured "A wtd" over a 20Hz ~ 20kHz bandwidth (AES17-1991 Idle Channel Noise or EIAJ CP-307 SNR)

THD: 0dB gain, 20kHz BW, Fs = 48kHz, -3dB "large" signal

A/D and D/A Frequency Response has ±0.25dB limits

Stop Band Rejection determines filter requirements

Out-of-Band rejection determines audible noise

Integrated Out-of-band noise generated by DAC during normal PCM audio playback over: BW = 28.8kHz~100kHz, with respect to 1 VRMS DAC output

## Performance Specifications  (*continued...*)

### Table 5.  Analog Performance Characteristics (+3.3V Power)

T$_A$=25°C, AVDD = DVDD = 3.3V ± 5%;  AVSS = DVSS =0V;  10kΩ / 50pF Load;  F$_S$ = 48kHz, 0dB = 0.70V$_{RMS}$;
BW: 20Hz ~ 20kHz, 0dB Attentuation,  IB[1:0]=10 (set by software), as measured on a 2-layers PCI add-in card

| Symbol | Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | Full Scale Input Voltage: | Line Inputs | | 0.7 | | VRMS |
| | | Mic Inputs (20dB = 0) | | 0.7 | | VRMS |
| | | Mic Inputs (20dB = 1) | | 0.07 | | VRMS |
| | Full Scale Output Voltage: | Line Outputs | | 0.70 | | VRMS |
| | | Mono Output | | 0.07 | | VRMS |
| | Analog S/N: | CD to LINE_OUT | | 92 | | dB |
| | | Other to LINE_OUT | | 92 | | dB |
| | Analog Frequency Response | | 20 | | 20,000 | Hz |
| | Digital S/N: | DAC | | 90 | | dB |
| | | ADC | | 85 | | dB |
| | Total Harmonic Distortion: | Line Outputs | | -70 | | dB |
| | D/A and A/D Frequency Response: | DAC | 20 | | 19,200 | Hz |
| | | ADC | 20 | | 19,200 | Hz |
| | Transition Band: | DAC | 19,200 | | 28,800 | Hz |
| | | ADC | 19,200 | | 28,800 | Hz |
| | Stop Band: | DAC | 28,800 | | infinity | Hz |
| | | ADC | 28,800 | | infinity | Hz |
| | Stop Band Rejection: | DAC | TBD | | | dB |
| | | ADC | TBD | | | dB |
| | Out-of-Band Rejection | | | -40 | | dB |
| | Group Delay | | | | 1 | ms |
| | Power Supply Rejection Ration (1kHz) | | | -40 | | dB |
| | Input Channel Crosstalk | | | | -70 | dB |
| | Spurious Tone Reduction | | | -100 | | dB |
| | Attenuation, Gain Step Size | | | 1.5 | | dB |
| | Input Impedance | | 10 | 50 | | kΩ |
| | Input Capacitance | | | 15 | | pF |
| | V$_{REFOUT}$ | | | 1.5 | | V |

**Note:**   V$_{IL}$ = 0.6V, V$_{IH}$ = 1.6V

Analog Frequency Response has ±1dB limits

SNR (measured as THD+N) of rms output level with 1kHz full-scale input to rms output level with all zeros into digital input

Measured "A wtd" over a 20Hz ~ 20kHz bandwidth (AES17-1991 Idle Channel Noise or EIAJ CP-307 SNR)

THD: 0dB gain, 20kHz BW, Fs = 48kHz,  -3dB "large" signal

A/D and D/A Frequency Response has ±0.25dB limits

Stop Band Rejection determines filter requirements

Out-of-Band rejection determines audible noise

Integrated Out-of-band noise generated by DAC during normal PCM audio playback over: BW = 28.8kHz~100kHz, with respect to 0.70 VRMS DAC output

## Performance Specifications (*continued...*)

### Table 6. Miscellaneous Analog Performance Characteristics

( TA=25°C, AVDD = DVDD = 5.0V ± 5%;  AVSS = DVSS =0V;  10kΩ / 50pF Load);  FS = 48kHz, 0dB = 1VRMS;
BW: 20Hz ~ 20kHz, 0dB Attentuation)

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| | Mixer Gain Range Span: | | | | |
| | LINE_IN, AUX, VIDEO, MIC1, MIC2, PHONE, PC_BEEP | | 46.5 | | dB |
| | LINE_OUT, MONO_OUT | | 46.5 | | dB |
| | Mixer Step Size: | | | | |
| | All Volume Controls except PC_BEEP | | 1.5 | | dB |
| | PC_BEEP | | 3.0 | | dB |
| | Mixer Mute Level | | 110 | | dB |
| | Mixer Gain:              Interchannel Gain Mismatch | -0.5 | | 0.5 | dB |
| | Gain Drift | | 100 | | ppm/°C |
| | ADC and Analog Inputs (Rs=50Ω):          Resolution | | | 18 | bits |
| | Gain Error | | ± 2 | ± 5 | % |
| | Offset Error | | 10 | | mV |
| | Input Impedance | | 50 | | kΩ |
| | DAC and Analog Outputs:          Resolution | | | 18 | bits |
| | Interchannel Isolation | | 80 | | dB |
| | Interchannel Gain Mismatch | | 0.1 | 0.2 | dB |
| | Gain Error | | | ± 5 | % |
| | Gain Drift | | 60 | | ppm/°C |

## Electrical Specifications

### Table 7. DC Characteristics

( TA=25°C, AVDD = DVDD = 5.0V or 3.3V ± 5%;  AVSS = DVSS =0V;  50pF Load )

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| VIN | Input Voltage Range | -0.3 | | VDD+0.3 | V |
| VIL | Input Low Voltage | | | 0.2 x VDD | V |
| VIH | Input High Voltage | 0.4 x VDD | | | V |
| VOL | Output Low Voltage | | | 0.2 x VDD | V |
| VOH | Output High Voltage | 0.5 x VDD | | | V |
| – | Input Leakage Current (AC-Link) | -10 | | 10 | µA |
| – | Output Leakage Current (AC-Link and Hi-Z) | -10 | | 10 | µA |
| – | Output Buffer Drive Current | | TBD | | mA |

## Electrical Specifications (*continued...*)

### Table 8. Power Consumption (+5V Power)

( TA=25°C, AVDD = DVDD = 5.0V ± 5%;  AVSS = DVSS =0V;  50pF Load )

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| IVDD | Digital Supply Current:  Power Up | | 58 | | mA |
| IVDD | Digital Supply Current:  Power Down | | 0.2 | | mA |
| IAVDD | Analog Supply Current:  Power Up default | | 44 | | mA |
| IAVDD | Analog Supply Current:  Power Up, IB[1:0]=11 | | 17 | | mA |
| IAVDD | Analog Supply Current:  Power Down, IB[1:0]=xx | | 0.4 | | mA |

### Table 9. Power Consumption (+3.3V Power)

( TA=25°C, AVDD = DVDD = 3.3V ± 5%;  AVSS = DVSS =0V;  50pF Load )

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| IVDD | Digital Supply Current:  Power Up | | 32 | | mA |
| IVDD | Digital Supply Current:  Power Down | | 0.03 | | mA |
| IAVDD | Analog Supply Current:  Power Up default | | 27 | | mA |
| IAVDD | Analog Supply Current:  Power Up, IB[1:0]=11 | | 11 | | mA |
| IAVDD | Analog Supply Current:  Power Down, IB[1:0]=xx | | 0.25 | | mA |

## AC Timing Characteristics

(Test Conditions: TA=25°C, AVDD = DVDD = 5.0V or 3.3V ± 5%;  AVSS = DVSS =0V;  50pF Load)

### Table 10. Cold Reset

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| TRST_LOW | RESET# Active Low Pulse Width | 1 | | | µs |
| TRST2CLK | RESET# Inactive to BIT_CLK Startup Delay | 162.8 | | | ns |
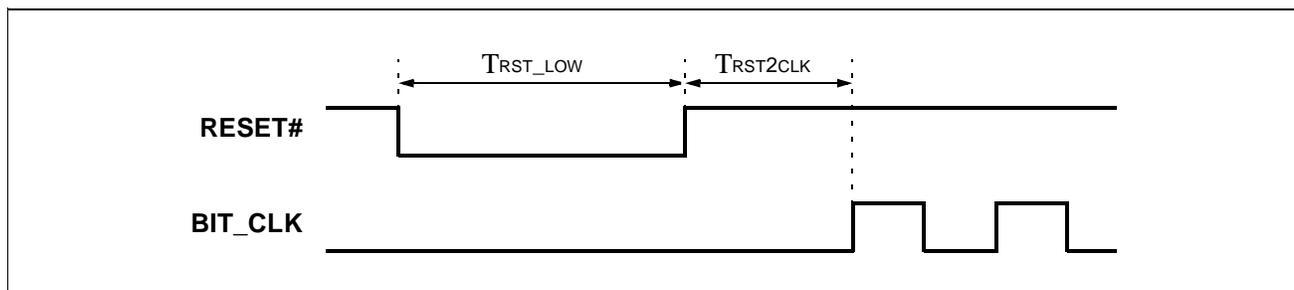
**Figure 4.  Cold Reset Timing**

# AC Timing Characteristics  (*continued...*)

**Table 11.  Warm Reset**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| T$_{SYNC\_HIGH}$ | Sync Active High Pulse Width | | 1.3 | | µs |
| T$_{SYNC2CLK}$ | SYNC Inactive to BIT_CLK Startup Delay | 162.8 | | | ns |
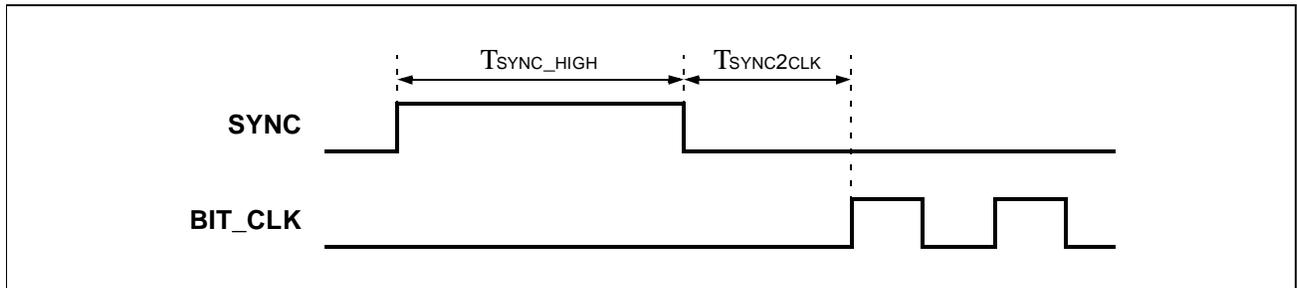


**Figure 5.  Warm Reset Timing**

**Table 12.  BIT_CLK / SYNC Timing**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| | BIT_CLK Frequency | | 12.288 | | MHz |
| T$_{CLK\_PERIOD}$ | BIT_CLK Period | | 81.4 | | ns |
| | BIT_CLK Output Jitter | | | 750 | ps |
| T$_{CLK\_HIGH}$ | BIT_CLK Pulse Width (high) | 32.56 | 40.7 | 48.84 | ns |
| T$_{CLK\_LOW}$ | BIT_CLK Pulse Width (low) | 32.56 | 40.7 | 48.84 | ns |
| T$_{CLK\_DC}$ | BIT_CLK Duty Cycle | 40 | | 60 | % |
| | SYNC Frequency | | 48 | | kHz |
| T$_{SYNC\_PERIOD}$ | SYNC Period | | 20.8 | | µs |
| T$_{SYNC\_HIGH}$ | SYNC Pulse Width (high) | | 1.3 | | µs |
| T$_{SYNC\_LOW}$ | SYNC Pulse Width (low) | | 19.5 | | µs |
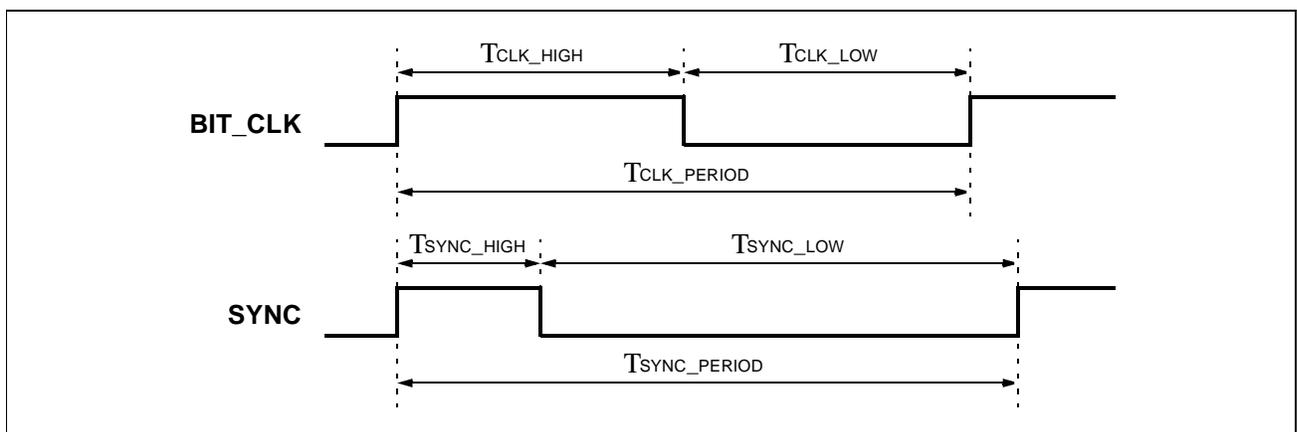


**Figure 6.  BIT_CLK to SYNC Timing**

## AC Timing Characteristics  (*continued...*)

**Table 13.  Setup and Hold**

| Symbol | Parameter | Min | Typ | Max | Unit |
|--------|-----------|-----|-----|-----|------|
| TSETUP1 | SDATA_OUT Setup to falling edge of BIT_CLK | 15 | | | ns |
| THOLD1 | SDATA_OUT Hold from falling edge of BIT_CLK | 5 | | | ns |
| TSETUP2 | SYNC Setup to rising edge of BIT_CLK | 15 | | | ns |
| THOLD2 | SYNC Hold to rising edge of BIT_CLK | 5 | | | ns |

**Note:** SDATA_IN seup and hold calculations determined by AC'97 controller propagation delay.
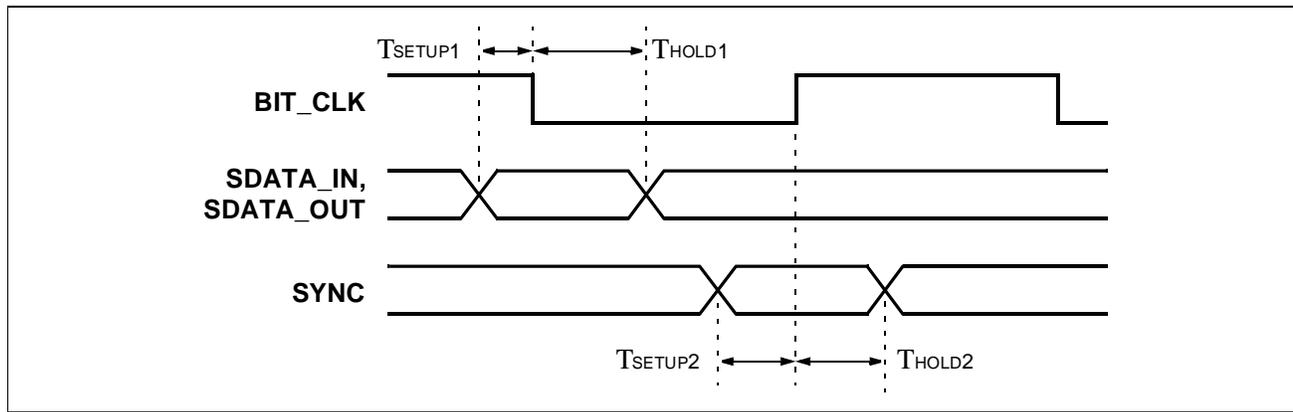
**Figure 7.  Setup and Hold Time**

**Table 14.  Rise and Fall Time**

| Symbol | Parameter | Min | Typ | Max | Unit |
|--------|-----------|-----|-----|-----|------|
| TRISE | BIT_CLK rise time | 2 | | 6 | ns |
| TFALL | BIT_CLK fall time | 2 | | 6 | ns |
| TRISE | SYNC  rise time | 2 | | 6 | ns |
| TFALL | SYNC  fall time | 2 | | 6 | ns |
| TRISE | SDATA_IN rise time | 2 | | 6 | ns |
| TFALL | SDATA_OUT fall time | 2 | | 6 | ns |
| TRISE | SDATA_OUT rise time | 2 | | 6 | ns |
| TFALL | SDATA_OUT fall time | 2 | | 6 | ns |
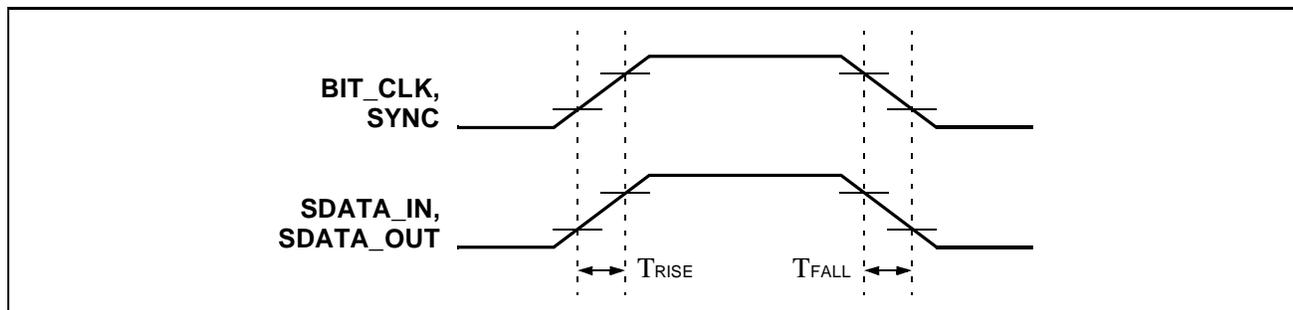
**Figure 8.  Rise Time and Fall Time**

## AC Timing Characteristics  (*continued...*)

**Table 15.  AC Link Low Power Mode**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{S2\_PDOWN}$ | End of Slot 2 to BIT_CLK / SDATA_IN low | | | 1 | µs |

**Note:**    BIT_CLK not to scale.
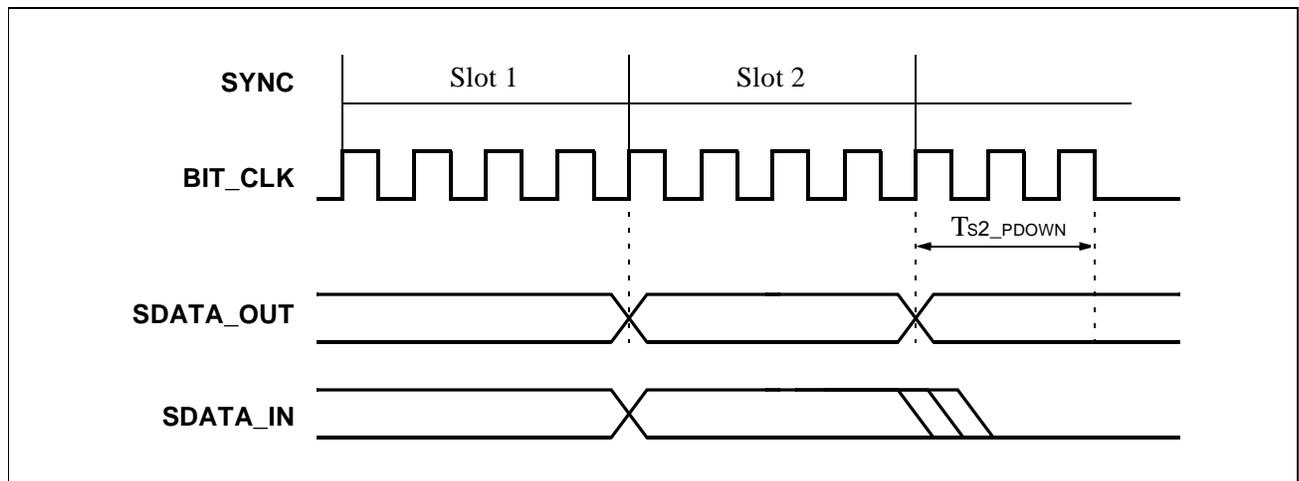


**Figure 9.  AC Link Power Mode Timing**

**Table 16.  ATE/Vendor Test Mode**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{SETUP2RST}$ | SDATA_OUT/SYNC setup to RESET# rising edge | 15 | | | ns |
| $T_{OFF}$ | RESET# rising edge to Hi-Z state | | | 25 | ns |
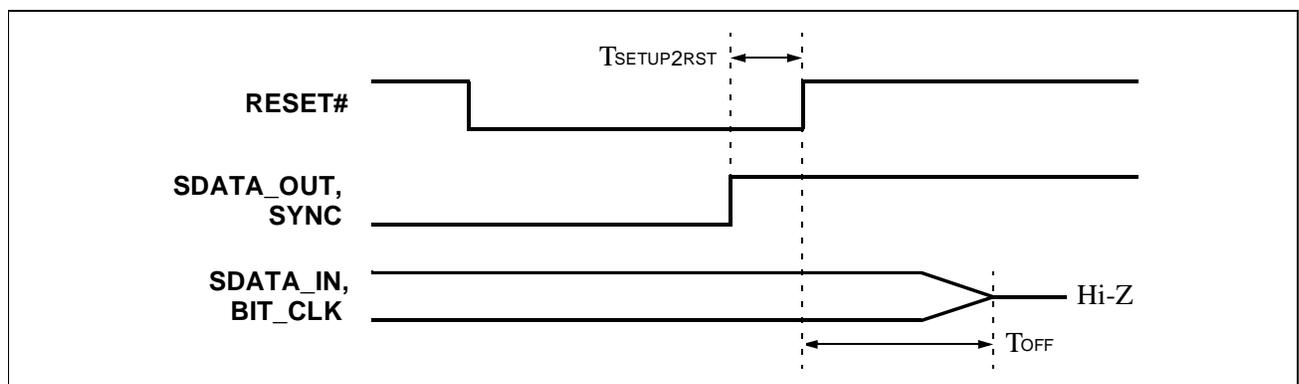


**Figure 10.  ATE/Vendor Test Mode Timing**

## Register Map

| Index | Register Name | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------|---------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 00h | Reset | – | SE4 | SE3 | SE2 | SE1 | SE0 | ID9 | ID8 | ID7 | ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 |
| 02h | Stereo Output Volume | Mute | – | – | ML4 | ML3 | ML2 | ML1 | ML0 | – | – | – | MR4 | MR3 | MR2 | MR1 | MR0 |
| 04h | Alt. Line Output Vol. | Mute | – | – | ML4 | ML3 | ML2 | ML1 | ML0 | – | – | – | MR4 | MR3 | MR2 | MR1 | MR0 |
| 06h | Mono Output Volume | Mute | – | – | – | – | – | – | – | – | – | – | MM4 | MM3 | MM2 | MM1 | MM0 |
| 0Ah | PC Beep Volume | Mute | – | – | – | – | – | – | – | – | – | – | PV3 | PV2 | PV1 | PV0 | – |
| 0Ch | Phone Volume | Mute | – | – | – | – | – | – | – | – | – | – | GN4 | GN3 | GN2 | GN1 | GN0 |
| 0Eh | Mic In Volume | Mute | – | – | – | – | – | – | – | – | 20dB | – | GN4 | GN3 | GN2 | GN1 | GN0 |
| 10h | Line In Volume | Mute | – | – | GL4 | GL3 | GL2 | GL1 | GL0 | – | – | – | GR4 | GR3 | GR2 | GR1 | GR0 |
| 12h | CD In Volume | Mute | – | – | GL4 | GL3 | GL2 | GL1 | GL0 | – | – | – | GR4 | GR3 | GR2 | GR1 | GR0 |
| 14h | Video In Volume | Mute | – | – | GL4 | GL3 | GL2 | GL1 | GL0 | – | – | – | GR4 | GR3 | GR2 | GR1 | GR0 |
| 16h | Aux In Volume | Mute | – | – | GL4 | GL3 | GL2 | GL1 | GL0 | – | – | – | GR4 | GR3 | GR2 | GR1 | GR0 |
| 18h | PCM Out volume | Mute | – | – | GL4 | GL3 | GL2 | GL1 | GL0 | – | – | – | GR4 | GR3 | GR2 | GR1 | GR0 |
| 1Ah | Record Select | – | – | – | – | – | SL2 | SL1 | SL0 | – | – | – | – | – | SR2 | SR1 | SR0 |
| 1Ch | Record Gain | Mute | – | – | – | GL3 | GL2 | GL1 | GL0 | – | – | – | – | GR3 | GR2 | GR1 | GR0 |
| 20h | General Purpose | – | – | 3D | – | – | – | MIX | MS | LPBK | – | – | – | – | – | – | – |
| 22h | 3D Control | – | – | – | – | – | – | – | – | – | – | – | – | DP3 | DP2 | DP1 | DP0 |
| 26h | Power Down & Status | EAPD | PR6 | PR5 | PR4 | PR3 | PR2 | PR1 | PR0 | – | – | – | – | REF | ANL | DAC | ADC |
| 28h | Extended Audio ID | ID1 | ID0 | – | – | – | – | AMAP | – | – | – | – | – | – | – | – | VRA |
| 2Ah | Ext. Audio Stat/Control | – | – | – | – | – | – | – | – | – | – | – | – | – | – | – | VRA |
| 2Ch | PCM Front DAC Rate | SR15 | SR14 | SR13 | SR12 | SR11 | SR10 | SR9 | SR8 | SR7 | SR6 | SR5 | SR4 | SR3 | SR2 | SR1 | SR0 |
| 32h | PCM LR ADC Rate | SR15 | SR14 | SR13 | SR12 | SR11 | SR10 | SR9 | SR8 | SR7 | SR6 | SR5 | SR4 | SR3 | SR2 | SR1 | SR0 |
| ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... |
| 5Ah | Test Control Register | – | – | – | – | – | – | – | – | Res. | Res. | Res. | Res. | IB1 | IB0 | – | Res. |
| ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... |
| 7Ah | Vendor Reserved | – | – | – | – | – | – | – | – | – | – | – | – | – | – | – | – |
| 7Ch | Vendor ID1 | F7 | F6 | F5 | F4 | F3 | F2 | F1 | F0 | S7 | S6 | S5 | S4 | S3 | S2 | S1 | S0 |
| 7Eh | Vendor ID2 | T7 | T6 | T5 | T4 | T3 | T2 | T1 | T0 | REV7 | REV6 | REV5 | REV4 | REV3 | REV2 | REV1 | REV0 |

In compliance with the AC '97 rev. 2.1 specification, all reserved or non-implemented register bits, non-implemented addresses, odd register addresses return 0 when read. Vendor specific registers 5Ah - 7Ah are reserved and should not be written for regular operation, unless otherwise specified.

## Register Description

**Reset Register  (Index 00h)**

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|---------|
| –   | SE4 | SE3 | SE2 | SE1 | SE0 | ID9 | ID8 | ID7 | ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 | 6D50h   |

The Reset register is used to configure the hardware to a known state or to read the ID code of the part. A code was assigned to IC Ensemble (27 = 11011h) for 3D Stereo Enhancement reflected in SE[4:0]. ID8 and ID6 are set to 1b to report that the ADC and DAC are 18-bit resolution respectively. The ICE1232 supports an alternate line level out with independent volume control as reflected by ID4=1b. Writing data to this register will set all the mixer registers to their default values. For description of the bits set to 0b, refer to AC'97 Rev. 2.1 spec.

**Stereo Output Control Register  (Index 02h)**

| D15  | D14 | D13 | D12 | D11 | D10 | D9  | D8  | D7 | D6 | D5 | D4  | D3  | D2  | D1  | D0  | Default |
|------|-----|-----|-----|-----|-----|-----|-----|----|----|----|-----|-----|-----|-----|-----|---------|
| Mute | –   | –   | ML4 | ML3 | ML2 | ML1 | ML0 | –  | –  | –  | MR4 | MR3 | MR2 | MR1 | MR0 | 8000h   |

**Mute**                     **Stereo Output Mute Control**

"1" :     Mute enabled

"0" :     Mute disabled

**ML[4:0]**                  **Master Output (Left Channel) Volume Control**

These five bits select the level of attenuation applied to the Left channel of the Stereo Output signal. The level of attenuation is programmable from 0dB to -46.5dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 17** on page 16 for details.

**MR[4:0]**                  **Master Output (Right Channel) Volume Control**

These five bits select the level of attenuation applied to the Right channel of the Stereo Output signal. The level of attenuation is programmable from 0dB to -46.5dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 17** on page 16 for details.

**Alternate Line Output Control Register  (Index 04h)**

| D15  | D14 | D13 | D12 | D11 | D10 | D9  | D8  | D7 | D6 | D5 | D4  | D3  | D2  | D1  | D0  | Default |
|------|-----|-----|-----|-----|-----|-----|-----|----|----|----|-----|-----|-----|-----|-----|---------|
| Mute | –   | –   | ML4 | ML3 | ML2 | ML1 | ML0 | –  | –  | –  | MR4 | MR3 | MR2 | MR1 | MR0 | 8000h   |

**Mute**                     **Stereo Output Mute Control**

"1" :     Mute enabled

"0" :     Mute disabled

**ML[4:0]**                  **Alternate Line Output (Left Channel) Volume Control**

These six bits select the level of attenuation applied to the Left channel of the Stereo Output signal. The level of attenuation is programmable from 0dB to -46.5dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 17** on page 16 for details.

**MR[4:0]**                  **Alternate Line Output (Right Channel) Volume Control**

These five bits select the level of attenuation applied to the Right channel of the Stereo Output signal. The level of attenuation is programmable from 0dB to -46.5dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 17** on page 16 for details.

**Mono Output Control Register  (Index 06h)**

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|---------|
| Mute | – | – | – | – | – | – | – | – | – | – | MM4 | MM3 | MM2 | MM1 | MM0 | 8000h |

**Mute**　　　　　　**Mono Output Mute Control**

"1" :　　Mute enabled

"0" :　　Mute disabled

**MM[4:0]**　　　　**Mono Output Volume Control**

These five bits select the level of attenuation applied to the Mono Output signal. The level of attenuation is programmable from 0dB to -46.5dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 17** on page 16 for details.

**Table 17.  Stereo and Mono Output Attenuation**

|    | M4 | M3 | M2 | M1 | M0 | Level (dB) |
|----|----|----|----|----|----|-----------|
| 0  | 0  | 0  | 0  | 0  | 0  | 0.0 |
| 1  | 0  | 0  | 0  | 0  | 1  | -1.5 |
| 2  | 0  | 0  | 0  | 1  | 0  | -3.0 |
| 3  | 0  | 0  | 0  | 1  | 1  | -4.5 |
| 4  | 0  | 0  | 1  | 0  | 0  | -6.0 |
| 5  | 0  | 0  | 1  | 0  | 1  | -7.5 |
| .. | .. | .. | .. | .. | .. | .. |
| .. | .. | .. | .. | .. | .. | .. |
| 28 | 1  | 1  | 1  | 0  | 0  | -42.0 |
| 29 | 1  | 1  | 1  | 0  | 1  | -43.5 |
| 30 | 1  | 1  | 1  | 1  | 0  | -45.0 |
| 31 | 1  | 1  | 1  | 1  | 1  | -46.5 |

**PC Beep Input Volume Control Register  (Index 0Ah)**

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|---------|
| Mute | – | – | – | – | – | – | – | – | – | – | PV3 | PV2 | PV1 | PV0 | – | 8000h |

**Mute**　　　　　　**PC Beep Input Mute Control**

"1" :　　Mute enabled

"0" :　　Mute disabled

**PV[3:0]**　　　　**PC Beep Input Volume Control**

These four bits select the level of attenuation applied to the PC beep input signal. The level of attenuation is programmable from 0dB to -45dB in 3dB increments, providing a total of 16 programmable levels. The beep gain is set at 0dB when PV[3:0] = 0h. Even though the default of the input volume control is mute, as long as RESET# is active, PC Beep will be passively routed to the line outputs.

**Phone Input Volume Control Register  (Index 0Ch)**

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|-----|-----|-----|-----|-----|-----|----|----|----|----|----|-----|-----|-----|-----|-----|---------|
| Mute | – | – | – | – | – | – | – | – | – | – | GN4 | GN3 | GN2 | GN1 | GN0 | 8008h |

**Mute**　　　　　　　**Phone Input Mute Control**

"1" :　　Mute enabled

"0" :　　Mute disabled

**GN[4:0]**　　　　　　**Phone Input Volume Control**

These five bits select the gain applied to the Phone Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 18** on page 20 for details.

**Mic Input Volume Control Register  (Index 0Eh)**

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|-----|-----|-----|-----|-----|-----|----|----|----|------|----|-----|-----|-----|-----|-----|---------|
| Mute | – | – | – | – | – | – | – | – | 20dB | – | GN4 | GN3 | GN2 | GN1 | GN0 | 8008h |

**Mute**　　　　　　　**Mic Input Mute Control**

"1" :　　Mute enabled

"0" :　　Mute disabled

**20dB**　　　　　　　**Mic Boost Control**

"1" :　　Fixed 20dB gain enabled

"0" :　　Fixed 20dB gain disabled

**GN[4:0]**　　　　　　**Mic Input Volume Control**

These five bits select the gain applied to the Mic Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 18** on page 20 for details.

**Line Input Control Register  (Index 10h)**

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|-----|-----|-----|-----|-----|-----|----|----|----|----|----|-----|-----|-----|-----|-----|---------|
| Mute | – | – | GL4 | GL3 | GL2 | GL1 | GL0 | – | – | – | GR4 | GR3 | GR2 | GR1 | GR0 | 8808h |

**Mute**　　　　　　　**Line Input Mute Control**

"1" :　　Mute enabled

"0" :　　Mute disabled

**GL[4:0]**　　　　　　**Left Channel Gain Control**

These five bits select the gain applied to the LEFT channel of the Line Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 18** on page 20 for details.

**GR[4:0]**　　　　　　**Right Channel Gain Control**

These five bits select the gain applied to the RIGHT channel of the Line Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 18** on page 20 for details.

**CD Input Control Register  (Index 12h)**

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|---------|
| Mute | – | – | GL4 | GL3 | GL2 | GL1 | GL0 | – | – | – | GR4 | GR3 | GR2 | GR1 | GR0 | 8808h |

**Mute**          **CD Input Mute Control**

"1" :     Mute enabled

"0" :     Mute disabled

**GL[4:0]**          **Left Channel Gain Control**

These five bits select the gain applied to the LEFT channel of the CD Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 18** on page 20 for details.

**GR[4:0]**          **Right Channel Gain Control**

These five bits select the gain applied to the RIGHT channel of the CD Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 18** on page 20 for details.

**Video Input Control Register  (Index 14h)**

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|---------|
| Mute | – | – | GL4 | GL3 | GL2 | GL1 | GL0 | – | – | – | GR4 | GR3 | GR2 | GR1 | GR0 | 8808h |

**Mute**          **Video Input Mute Control**

"1" :     Mute enabled

"0" :     Mute disabled

**GL[4:0]**          **Left Channel Gain Control**

These five bits select the gain applied to the LEFT channel of the Video Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 18** on page 20 for details.

**GR[4:0]**          **Right Channel Gain Control**

These five bits select the gain applied to the RIGHT channel of the Video Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 18** on page 20 for details.

**Auxiliary Input Control Register  (Index 16h)**

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|------|-----|-----|-----|-----|-----|-----|-----|----|----|----|-----|-----|-----|-----|-----|---------|
| Mute | – | – | GL4 | GL3 | GL2 | GL1 | GL0 | – | – | – | GR4 | GR3 | GR2 | GR1 | GR0 | 8808h |

**Mute**                    **Auxiliary Input Mute Control**

"1" :     Mute enabled

"0" :     Mute disabled

**GL[4:0]**                 **Left Channel Gain Control**

These five bits select the gain applied to the LEFT channel of the Auxiliary Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 18** on page 20 for details.

**GR[4:0]**                 **Right Channel Gain Control**

These five bits select the gain applied to the RIGHT channel of the Auxiliary Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 18** on page 20 for details.

**PCM Output Control Register  (Index 18h)**

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|------|-----|-----|-----|-----|-----|-----|-----|----|----|----|-----|-----|-----|-----|-----|---------|
| Mute | – | – | GL4 | GL3 | GL2 | GL1 | GL0 | – | – | – | GR4 | GR3 | GR2 | GR1 | GR0 | 8808h |

**Mute**                    **PCM Output Mute Control**

"1" :     Mute enabled

"0" :     Mute disabled

**GL[4:0]**                 **Left Channel Gain Control**

These five bits select the gain applied to the LEFT channel of the PCM Output signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 18** on page 20 for details.

**GR[4:0]**                 **Right Channel Gain Control**

These five bits select the gain applied to the RIGHT channel of the PCM Output signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 18** on page 20 for details.

**Table 18.   Programmable Mixer Input Gain Levels**

|    | G4 | G3 | G2 | G1 | G0 | Level (dB) |
|----|----|----|----|----|----|------------|
| 0  | 0  | 0  | 0  | 0  | 0  | 12.0  |
| 1  | 0  | 0  | 0  | 0  | 1  | 10.5  |
| 2  | 0  | 0  | 0  | 1  | 0  | 9.0   |
| 3  | 0  | 0  | 0  | 1  | 1  | 7.5   |
| 4  | 0  | 0  | 1  | 0  | 0  | 6.0   |
| 5  | 0  | 0  | 1  | 0  | 1  | 4.5   |
| 6  | 0  | 0  | 1  | 1  | 0  | 3.0   |
| 7  | 0  | 0  | 1  | 1  | 1  | 1.5   |
| 8  | 0  | 1  | 0  | 0  | 0  | 0.0   |
| 9  | 0  | 1  | 0  | 0  | 1  | -1.5  |
| 10 | 0  | 1  | 0  | 1  | 0  | -3.0  |
| 11 | 0  | 1  | 0  | 1  | 1  | -4.5  |
| 12 | 0  | 1  | 1  | 0  | 0  | -6.0  |
| 13 | 0  | 1  | 1  | 0  | 1  | -7.5  |
| 14 | 0  | 1  | 1  | 1  | 0  | -9.0  |
| 15 | 0  | 1  | 1  | 1  | 1  | -10.5 |
| 16 | 1  | 0  | 0  | 0  | 0  | -12.0 |
| 17 | 1  | 0  | 0  | 0  | 1  | -13.5 |
| 18 | 1  | 0  | 0  | 1  | 0  | -15.0 |
| 19 | 1  | 0  | 0  | 1  | 1  | -16.5 |
| 20 | 1  | 0  | 1  | 0  | 0  | -18.0 |
| 21 | 1  | 0  | 1  | 0  | 1  | -19.5 |
| 22 | 1  | 0  | 1  | 1  | 0  | -21.0 |
| 23 | 1  | 0  | 1  | 1  | 1  | -22.5 |
| 24 | 1  | 1  | 0  | 0  | 0  | -24.0 |
| 25 | 1  | 1  | 0  | 0  | 1  | -25.5 |
| 26 | 1  | 1  | 0  | 1  | 0  | -27.0 |
| 27 | 1  | 1  | 0  | 1  | 1  | -28.5 |
| 28 | 1  | 1  | 1  | 0  | 0  | -30.0 |
| 29 | 1  | 1  | 1  | 0  | 1  | -31.5 |
| 30 | 1  | 1  | 1  | 1  | 0  | -33.0 |
| 31 | 1  | 1  | 1  | 1  | 1  | -34.5 |

**Record Select Register  (Index 1Ah)**

| D15 | D14 | D13 | D12 | D11 | D10 | D9  | D8  | D7 | D6 | D5 | D4 | D3 | D2  | D1  | D0  | Default |
|-----|-----|-----|-----|-----|-----|-----|-----|----|----|----|----|----|-----|-----|-----|---------|
| –   | –   | –   | –   | –   | SL2 | SL1 | SL0 | –  | –  | –  | –  | –  | SR2 | SR1 | SR0 | 0000h   |

**SL[2:0]**          **Record Source Select (Left Channel)**

These bits determine the record source for the left channel.

| SL2 | SL1 | SL0 | Left Record Source |
|-----|-----|-----|--------------------|
| 0 | 0 | 0 | Mic |
| 0 | 0 | 1 | CD (L) |
| 0 | 1 | 0 | Video In (L) |
| 0 | 1 | 1 | Aux In (L) |
| 1 | 0 | 0 | Line In (L) |
| 1 | 0 | 1 | Stereo Mix (L) |
| 1 | 1 | 0 | Mono Mix |
| 1 | 1 | 1 | Phone |

**SR[2:0]** **Record Source Select (Right Channel)**

These bits determine the record source for the right channel.

| SR2 | SR1 | SR0 | Right Record Source |
|-----|-----|-----|---------------------|
| 0 | 0 | 0 | Mic |
| 0 | 0 | 1 | CD (R) |
| 0 | 1 | 0 | Video In (R) |
| 0 | 1 | 1 | Aux In (R) |
| 1 | 0 | 0 | Line In (R) |
| 1 | 0 | 1 | Stereo Mix (R) |
| 1 | 1 | 0 | Mono Mix |
| 1 | 1 | 1 | Phone |

**Record Gain Control Register  (Index 1Ch)**

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|---------|
| Mute | – | – | – | GL3 | GL2 | GL1 | GL0 | – | – | – | – | GR3 | GR2 | GR1 | GR0 | 8000h |

**Mute** **Record Mute Control**

"1" :    Mute enabled

"0" :    Mute disabled

**GL[3:0]** **Record Gain Control (Left Channel)**

These four bits select the gain applied to the LEFT channel recording source. The gain is programmable from 0dB to 22.5dB in 1.5dB increments, providing a total of 16 programmable levels. The gain is set at 0dB when GL[3:0] = 0h.

**GR[3:0]** **Record Gain Control (Right Channel)**

These four bits select the gain applied to the RIGHT channel recording source. The gain is programmable from 0dB to 22.5dB in 1.5dB increments, providing a total of 16 programmable levels. The gain is set at 0dB when GR[3:0] = 0h.

**General Purpose Register  (Index 20h)**

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|---------|
| – | – | 3D | – | – | – | MIX | MS | LPBK | – | – | – | – | – | – | – | 0000h |

**3D** **3D Stereo Enhancement**

"1" :    Enable 3D

"0" :    Disable 3D

**MIX** **Mono Output Mode**

"1" :    Mic Output

"0" :    Mono mix output

**MS** **Microphone Select**

"1" :    Microphone 2

"0" :    Microphone 1

**LPBK** **Loopback Mode**

"1" :    DAC/ADC Loopback enabled

"0" :    DAC/ADC Loopback disabled

**3D Control Register  (Index 22h)**

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|-----|-----|-----|-----|---------|
| – | – | – | – | – | – | – | – | – | – | – | – | DP3 | DP2 | DP1 | DP0 | 0000h |

**DP[3:0]**　　　　**3D Depth Control**

These four bits control the linear depth control of the 3D stereo enhancement built into the codec. The gain is programmable from 0% to 100% in 6.67% increments, providing a total of 16 programmable levels. The default value corresponds to no stereo enhancement.

**Power Down and Status Register  (Index 26h)**

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|-----|-----|-----|-----|---------|
| EAPD | PR6 | PR5 | PR4 | PR3 | PR2 | PR1 | PR0 | – | – | – | – | REF | ANL | DAC | ADC | 0000h |

**EAPD**　　　　**Enable Amplifier Power Down**

"1" :　　Powerdown External Power Amplifier

"0" :　　External Power Amplifier active

The signal polarity at pin 47, EAPD is identical to bit description.

**PR[5:0]**　　　　**Power Down Mode Bits**

These read/write bits are used to control the power down states of the ICE1232. Each power down function bit is enabled by setting the respective bit high. The power down modes controlled by each bit is described in the table below:

| Bit | Function |
|-----|----------|
| PR0 | ADC and Mux Powerdown |
| PR1 | DAC Powerdown |
| PR2 | Mixer Powerdown (VREF on) |
| PR3 | Mixer Powerdown (VREF off) |
| PR4 | AC Link Powerdown (BIT_CLK off) |
| PR5 | Internal Clock Disabled |
| PR6 | Alternate Line Out Powerdown |

**Status (READ Only) bits**

These bits are used to monitor the readiness of some sections of the ICE1232. Reading a "1" from any of these bits would be an indication of a "ready" state.

| Bit | Status Bit |
|-----|-----------|
| REF | VREF at nominal level |
| ANL | Mixer, Mux and Volume Controls ready |
| DAC | DAC ready to accept data |
| ADC | ADC ready to transmit data |

**Extended Audio ID Register (Index 28h)**

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|-----|-----|-----|-----|-----|-----|------|----|----|----|----|----|----|----|----|-----|---------|
| ID1 | ID0 | – | – | – | – | AMAP | – | – | – | – | – | – | – | – | VRA | 0201h |

The Extended Audio ID is a read only register.

**ID[1:0]**　　　　**(See Table below)**

One primary and a maximum of three secondary codecs may be supported as an option.

**Table 19.  Multiple Codec Mode Status Bits**

| ID1 | ID0 | Codec Mode |
|-----|-----|------------|
| 0 | 0 | Primary Codec (default) |
| 0 | 1 | Secondary Codec 1 |
| 1 | 0 | Secondary Codec 2 |
| 1 | 1 | Secondary Codec 3 |

**Note:**    The state of the ID pins is reported in reverse polarity on register 28h, bits D15 and D14. If you use Table 16 to configure the codec via pins 45 and 46, use the inverse values. Please, refer to **Figure 11** on page 25. Digital Controllers may support up to four DATA_IN pins to support one primary and three secondary codecs. BIT_CLK is an output for the primary codec and an input pin for the controller and secondary codecs. ID[1:0] pins with internal pull-up resistors defaults codec as primary codec.

**AMAP**            **Slot/DAC mapping based on Codec ID**

"1" :     Feature implemented in compliance to AC '97 2.1 Appendix D

**VRA**            **Variable Sampling Rate PCM Audio**

"1" :     Feature implemented in compliance to AC '97 2.1 Appendix A

**Extended Audio Status/Control  Register(Index 2Ah)**

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|---------|
| – | – | – | – | – | – | – | – | – | – | – | – | – | – | – | VRA | 0000h |

**VRA**            **Variable Sampling Rate Mode control**

"1" :     Enable VSR
"0" :     Fixed 48kHz sampling rate

**PCM DAC Sample Rate Register  (Index 2Ch)**

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|---------|
| SR15 | SR14 | SR13 | SR12 | SR11 | SR10 | SR9 | SR8 | SR7 | SR6 | SR5 | SR4 | SR3 | SR2 | SR1 | SR0 | BB80h |

**SR[15:0]**            **DAC Sample Rate (in Hz)**

16-bit unsigned value representing the sample rate in 1Hz resolution. The default value is 48kHz (48000 = BB80h).

**PCM ADC Sample Rate Register  (Index 32h)**

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|---------|
| SR15 | SR14 | SR13 | SR12 | SR11 | SR10 | SR9 | SR8 | SR7 | SR6 | SR5 | SR4 | SR3 | SR2 | SR1 | SR0 | BB80h |

**SR[15:0]**            **ADC Sample Rate (in Hz)**

16-bit unsigned value representing the sample rate in 1Hz resolution. The default value is 48kHz (48000 = BB80h).

**Vendor Reserved Register  (Index 5Ah)**

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|-----|-----|-----|-----|-----|-----|-----|-----|------|------|------|------|-----|-----|-----|------|---------|
| – | – | – | – | – | – | – | – | Res. | Res. | Res. | Res. | IB1 | IB0 | – | Res. | 0021h |

**Res.**  **Reserved**

These read/write bits are used for testing the digital modes of the audio codec. Do not access them during Normal operation.

**IB[1:0]**  **Analog Current Setting Bits**

Normally these bits should be left at default when analog operating at 5V supply. The four possible settings adjust the power consumption of the analog section. The power-up default 00b sets the codec for the best analog performance at 5V. At 3.3V analog supply, 10b should be set for the best analog performance instead of default 00b. Setting to 11b puts the codec in its most aggressive low power consumption mode during normal operation. This mode is desirable for system designs with limited power budget such as battery operated portable devices. Intermediate steps 01b and 10b set the analog bias current to 40% and 50% of maximum respectively. However it does not translate linearly to the total analog power consumption current.

**Vendor Identification Register  (Index 7Ch)**

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|---------|
| F7 | F6 | F5 | F4 | F3 | F2 | F1 | F0 | S7 | S6 | S5 | S4 | S3 | S2 | S1 | S0 | 4943h |

The upper and lower byte of this register (index 7Ch), in conjunction with the upper byte of index register 7Eh, make up the vendor identification code for the ICE1232. The Vendor ID Code (in ASCII format) is equal to ICE, where:

**F[7:0]**  **Upper Byte (Index 7Ch) D[15:8] = I**

**S[7:0]**  **Lower Byte (Index 7Ch) D[7:0]  = C**

**T[15:8]**  **Upper Byte (Index 7Eh) D[15:8] = E**

**Revision Identification Register  (Index 7Eh)**

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|-----|-----|-----|-----|-----|-----|-----|-----|------|------|------|------|------|------|------|------|---------|
| T7 | T6 | T5 | T4 | T3 | T2 | T1 | T0 | REV7 | REV6 | REV5 | REV4 | REV3 | REV2 | REV1 | REV0 | 4511h |

The upper byte of this register is used in conjuction with index register 7Ch to make up the Vendor ID code for the ICE1232. The lower byte identifies ICE1232 and its revision code.

**T[15:8]**  **See description in Vendor Identification Register.**

**REV[7:0]**  **Revision ID**

"11":  Revision Number

**Note:** As a reference, other valid IDs associated with ICE AC'97 products are:  "01" for ICE1230.

## Multiple Codec Example

One primary codec and three secondary codecs, with tag bits ID[1:0] defining which codec is primary and the order of the secondary codecs. Note that the ID[1:0] pins are internally pulled up; therefore, it is necessary to pull the ID[1:0] pins low to set the codec as secondary. Notice that the state of the ID[1:0] pins are reflected in reverse polarity as shown on **Table 19** on page 23.
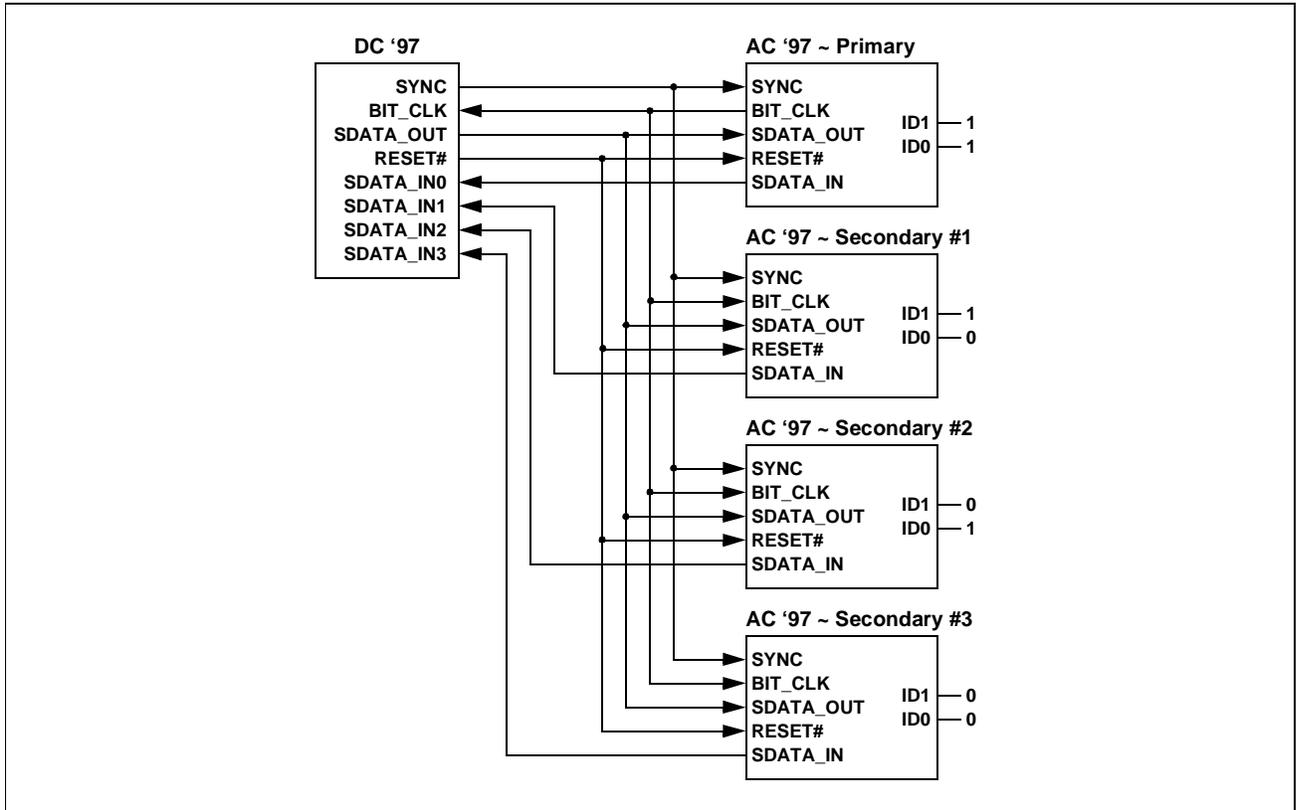


**Figure 11.  Multiple Codec Example**

## Power Management

The ICE1232 may be placed in several power down states using the power down control bits located in index register 26h. **Table 20** lists the power down states accessible through this register.

**Table 20.  Power Down Mode Bits**

| Bit | Function |
| --- | --- |
| PR0 | ADC and Mux Powerdown |
| PR1 | DAC Powerdown |
| PR2 | Mixer Powerdown (VREF on) |
| PR3 | Mixer Powerdown (VREF off) |
| PR4 | AC Link Powerdown (BIT_CLK off) |
| PR5 | Internal Clock Disabled |
| PR6 | Alternate Line Out Powerdown |

**Note:**  Registers maintain values in sleep mode (PR4 write) and wake up with a warm reset (register values) or a cold reset (default values).  Power Down and Status register (index 26h) read action verifies stability before power down write action occurs.
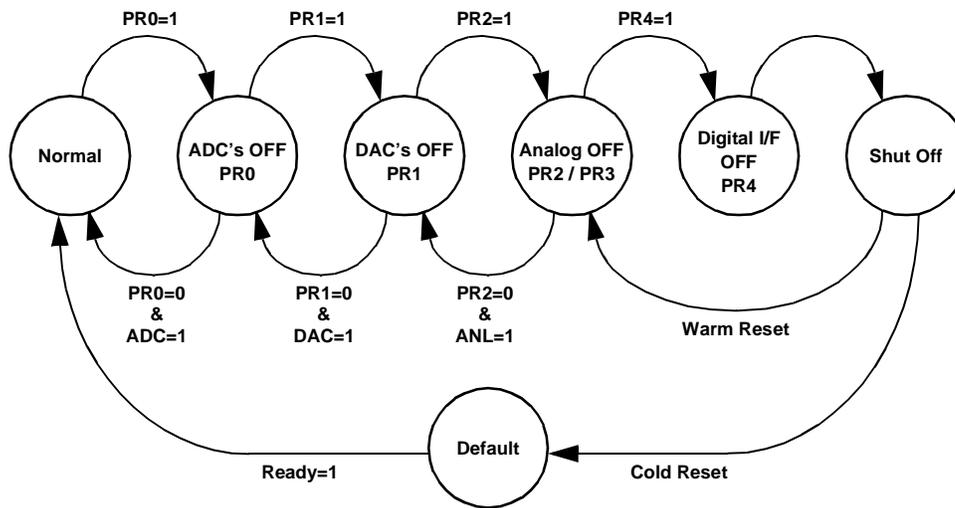


Note:  In this example, the Analog Mixer has been disabled, but VREF is still on.

**Figure 12.  AC'97 Power Down / Power Up Procedure**

Complete power down of the AC '97 device is achieved by sequential writes to the Power Down and Status Control Register (Index 26h) as follows:

| | |
| --- | --- |
| Normal Operations: | PR[6:0] = 00h |
| ADC's and Input Mux: | PR0 = 1 (write) |
| DAC's: | PR1 = 1 (write) |
| Analog Mixer: | PR2 = 1 (write) |
| VREFOUT: | PR3 = 1 (write) |
| AC-link: | PR4 = 1 (write) |
| Internal Clocks: | PR5 = 1 (write) |
| Alt. Line Out: | PR6 = 1 (write) |

## Power Management  (*continued...*)
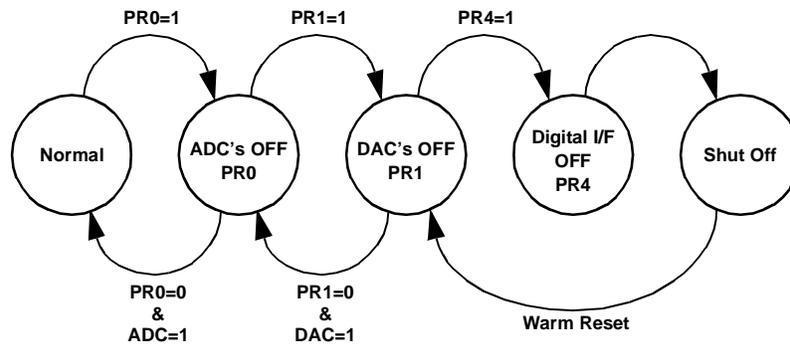


Note:  To power up the codec, a warm reset is required; PR4 is reset to zero upon either reset.

**Figure 13.  AC'97 Power Down Procedure with Analog Section Still Active**

## Test Mode Operation

### ATE Test Mode:  (PCB in-circuit Testing of the ICE1232)

ATE Test mode is entered when the SDATA_OUT signal is sampled at the rising edge of the RESET# signal. In this mode, the SDATA_IN and BIT_CLK pins are placed in a high impedance (Hi-Z) state. This mode of operation doesn't occur under normal operating conditions.

### Vendor Test Mode:

Vendor Test mode is entered when the SYNC signal is sampled during the rising edge of the RESET# signal. This mode of operation doesn't occur under normal operating conditions.

## Package Dimensions
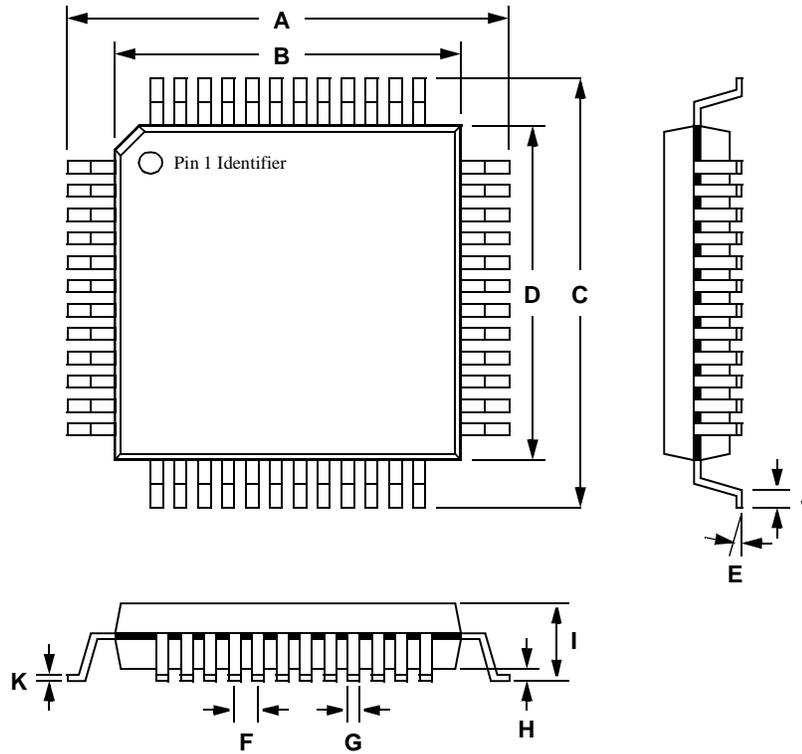


## Mechanical Dimensions (millimeters, unless otherwise stated)

| Symbol | A | B | C | D | E | F | G | H | I | J | K |
|--------|---|---|---|---|---|---|---|---|---|---|---|
| **48-pin (7x7) TQFP** | | | | | | | | | | | |
| minimum | 8.6 | 6.9 | 8.6 | 6.9 | 0° | 0.5 | 0.17 | 0.05 | 1.0 | 0.45 | 0.100 |
| maximum | 9.4 | 7.1 | 9.4 | 7.1 | 10° | | 0.27 | 0.15 | | 0.75 | 0.175 |
| **48-pin (7x7) LQFP** | | | | | | | | | | | |
| minimum | 8.6 | 6.9 | 8.6 | 6.9 | 0° | 0.5 | 0.13 | 0.05 | – | 0.3 | 0.100 |
| maximum | 9.4 | 7.1 | 9.4 | 7.1 | 10° | | 0.28 | 0.15 | 1.7 | 0.7 | 0.175 |