# Aladdin V

## M1541/M1543C

*Product Brief*

*Core Logic for Pentium$^{TM}$ /M1/M2/K5/K6 based Business and Multimedia PCs*

**INTRODUCTION**

Aladdin-V is the fifth generation 586 chipset from AcerLabs.  It maintains the best system architecture (2-chip solution) to achieve the best system performance with the lowest system cost (TTL-free).  Aladdin-V consists of two BGA chips to give the 586-class system a complete solution with most up-to-date features and architecture for the most engaging multimedia/ multithreading OS and software applications.  It utilizes the modern BGA package to improve the AC characterization, resolves system bottleneck and make the system manufacturing easier.

The M1541 includes the higher CPU bus frequency (up to 100 MHz) interface for all socket 7 compatible processors, PBSRAM and Memory Cache L2 controller, internal MESI tag bits (16K*2) and Tag RAM (under tests) to reduce cost and enhance performance, high performance FPM/EDO/SDRAM DRAM controller, PCI 2.1 compliant bus interface, smart deep buffer design for CPU-to-DRAM, CPU-to-PCI, and PCI-to-DRAM to achieve the best system performance, and also the highly efficient PCI fair arbiter.  The M1541 also provides the most flexible 64-bit memory bus interface for the best DRAM upgradeability and ECC/Parity design to enhance the system reliability.

With the AGP interface design, the dedicated PCI_66 AGP interface can be concurrent with CPU and PCI interface.  The deep buffer of the read and write buffer design makes the utilization of memory bandwidth more efficient.  The interface supports AGP specification V1.0.  Supports up to 128 entries table look aside buffer for Graphic Address Remapping Table (GART).  The interface not only supports the AGP 66MHz PCI protocol, but also the AGP 1X and 2X sideband address function.

With the concurrent bus design, PCI-to-PCI access can run concurrently with CPU-to-L2 and CPU-to-DRAM access, PCI-to-DRAM access can run concurrently with CPU-to-L2 access.  The M1541 also supports the snoop ahead feature to achieve the PCI master full bandwidth access (133Mbytes).  The M1541 also provides the enhanced power management features including ACPI support, suspend DRAM refresh, and internal chip power control to support Microsoft's On Now technology OS.

The M1543C provides the best desktop system solution.  The M1543C integrates ACPI support, green function, 2-channel dedicated Ultra-33 IDE Master controller, 2-port USB controller, SMBus controller, PS/2 Keyboard/Mouse controller, the Super I/O (Floppy Disk Controller, 2 serial port/1 parallel port) support and Fast IR.

The built-in I/O in M1543C is an advanced Super I/O controller solution to the basic IBM PC, XT, AT and notebook peripherals.  It incorporates two full function universal asynchronous receiver/ transmitters (UARTs), a flexible high performance internal data separator with send/receive 16 byte FIFOs.  It is suitable for notebook computers since it has Fast Infra Red for wireless communications with other devices.  It can swap your drives A & B.  It features basic functions such as standard mode, enhanced mode, high speed mode.  It supports SPP, PS/2, EPP and ECP parallel port.  It also has a programmable baud rate generator.  It has high performance power management for FDC, UART and parallel port.

Furthermore, Aladdin V is designed to meet the requirements of all socket 7 processors including business, multimedia and high performance CPU file servers.

## M1541 (AGP, CPU-to-PCI Bridge, Memory Cache & Buffer Controller)

■ **Supports all socket 7 processors.** Host bus at *100MHz*, 83.3MHz, 75MHz, 66 MHz, 60 MHz and 50MHz at 3.3V/2.5V.
   - Supports linear wrap mode for Cyrix M1 & M2
   - Supports Write Allocation feature for AMD K6
   - Supports Pseudo Synchronous PCI bus access
  (CPU bus 75MHz - PCI bus 30Mhz,
   CPU bus 83.3MHz - PCI bus 33Mhz,
   CPU bus 100MHz - PCI bus 33Mhz)

■ **Supports Pipelined-Burst SRAM/Memory Cache**
   - Direct mapped, 256KB/512KB/1MB
   - Write-Back/Dynamic-Write-Back cache policy
   - *Built-in 16K\*2 bit SRAM for MESI* protocol to reduce cost and enhance performance
   - *Built-in 16K\*10 bit SRAM for TAG* data to reduce cost and enhance performance (under tests)
   - Cacheable memory up to 512MB with 10-bit Tag SRAM when using 512KB L2 cache, 1GB when using 256KB L2 cache
   - 3-1-1-1-1-1-1-1 for Pipelined Burst SRAM/ Memory Cache at back-to-back burst read and write cycles.
   - Supports 3.3V/5V SRAMs for Tag Address.
   - Supports CPU Single Read Cycle L2 Allocation.

■ **Supports FPM/EDO/SDRAM DRAMs**
   - 8 RAS Lines up to 1GByte support
   - 64-bit data path to Memory
   - Symmetrical/Asymmetrical DRAMs
   - 3.3V or 5V DRAMs
   - No buffer needed for RASJ and CASJ and MA
   - CBR and RAS-only refresh for FPM
   - CBR and RAS-only refresh and Extended refresh and self refresh for EDO
   - CBR and Self refresh for SDRAM
   - 32 QWORD deep merging buffer for 3-1-1-1-1-1-1-1 posted write cycle to enhance high speed CPU burst access
   - 6-3-3-3-3-3-3-3 for back-to-back FPM read page hit
    5-2-2-2-2-2-2-2 for back-to-back EDO read page hit
    6-1-1-1-2-1-1-1 for back-to-back SDRAM read page hit
    x-2-2-2 for retired data for posted write on FPM and EDO page-hit
    x-1-1-1 for retired data for posted write SDRAM page-hit
   - Enhanced DRAM page miss performance
   - Supports 64Mbit (16M\*4, 8M\*8, 4M\*16) technology of DRAMs

   - Supports programmable-strength RAS/CAS/ MWEJ/MA buffers.
   - Supports Error Checking & Correction (ECC) and Parity for DRAM
   - Supports 4 single-sided DIMMs based on x4 DRAMs
   - Supports 4 single and double-sided DIMMs based on x8 and x16 DRAMs

■ **Synchronous/Pseudo Synchronous 25/30/33MHz 3.3V/5V tolerance PCI interface**
   - Concurrent PCI architecture
   - PCI bus arbiter: Five PCI masters and M1533/ M1543/M1553 (ISA Bridge) and AGP Master supported
   - 6 DWORDs for CPU-to-PCI Memory write posted buffers
   - Converts back-to-back CPU to PCI memory write to PCI burst cycle
   - 48/22 DWORDs for PCI-to-DRAM Write-posted/ Read-prefetching buffers
   - PCI-to-DRAM up to 133 MB/sec bandwidth (even when L1/L2 write back)
   - L1/L2 pipelined snoop ahead for PCI-to-DRAM cycle
   - Supports PCI mechanism #1 only
   - PCI spec. 2.1 support. (N(32/16/8)+8 rule, passive release, fair arbitration)
   - Enhanced performance for Memory-Read-Line and Memory-Read-Multiple and Memory-write-Invalidate PCI commands.

■ **Enhanced Power Management**
   - ACPI support
   - Supports PCI bus CLKRUN function
   - Supports Dynamic Clock Stop
   - Supports Power On Suspend
   - Supports Suspend to Disk
   - Supports Suspend to DRAM
   - Self Refresh during Suspend

■ **Accelerated Graphics Port (AGP) Interface**
   - *Supports AGP specification V1.0*
   - Supports up to 128 entries table look aside buffer for Graphic Address Remapping Table (GART)
   - AGP 66MHz PCI protocol
   - *AGP 1X and 2X sideband* address function
   - 32 entries Request queue
   - 32 QWORDs Read buffer
   - 16 QWORDs Write buffer

■ **35x35 mm 456-pin BGA package**

## M1543C (PCI-to-ISA Bus Bridge with Super I/O and Fast IR)

■ **Provides a highly integrated bridge (with Super I/O & Fast IR) between PCI and ISA bus for both Pentium and Pentium II systems**

■ **PCI 3.3V/5V Tolerance Interface**
- Supports PCI Master and Slave Interface
- Supports PCI Master and Slave Initiated Termination
- Concurrent PCI Architecture
- PCI spec. 2.1 Compliant (Delayed Transaction & Passive Release Support)

■ **Buffers Control**
- 8-byte Bi-directional Line Buffers for DMA/ISA Memory Read/Write Cycles to PCI Bus
- 32-bit Posted Write Buffer for PCI Memory Write and I/O Data Write (for Sound Card) to ISA Bus

■ **Provides Steerable PCI Interrupts for PCI device Plug-and-Play**
- Up to 8 PCI Interrupts Routing
- Level to Edge Trigger Transfer

■ **Enhanced DMA Controller**
- Provides 7 Programmable Channels, 4 for 8-bit Data Size, 3 for 16-bit Data Size
- 32-bit Addressability
- Provides Compatible DMA Transfers
- Provides Type F Transfers

■ **Interrupt Controller**
- Provides 14 Interrupt Channels
- Independent Programmable Level/Edge Triggered Channels

■ **Counter/Timers**
- Provides 8254 Compatible Timers for System Timer, Refresh Request, Speaker Output Use

■ **Supports Distributed DMA**
- 7 DMA Channels can be Arbitrarily Programmed as Distributed Channels

■ **Supports Serialized IRQ**
- Quiet/Continuous Mode
- Programmable (Default 21) IRQ/DATA Frames
- Programmable START Frame Pulse Width

■ **Supports Plug-and-Play**
- 1 Programmable Chip Select
- 2 Steerable Interrupt Request Lines

■ **Built-in Keyboard Controller**
- Built-in PS2/AT Keyboard and PS2 Mouse Controller

■ **Supports up to 256 KB ROM Size Decoding**

■ **Supports Positive/Subtractive Decode for ISA Device**

■ **PMU Features**
- Full Support for ACPI and OS Directed Power Management
- CPU SMM Legacy Mode and SMI Feature Supported
- Supports Programmable STPCLKJ: Throttle/CKONSTP/CKOFFSTP Control
- Supports I/O Trap for I/O Restart Feature
- PMU Operation States:
  -- ON
  -- Standby
  -- Sleep (Power On Suspend)
  -- Suspend (Suspend to DRAM)
  -- Suspend to HDD
  -- Soft-Off
  -- Mechanical Off
- APM State Detection and Control Logic Supported
- Global and Local Device Power Control Logic
- 3 Programmable Timers: Standby/ APMA/ Global_Display
- Provides System Activity and Display Activity Monitoring, including
  -- Video
  -- Audio
  -- Hard Disk
  -- Floppy Disk
  -- Serial Ports
  -- Parallel Port
  -- Keyboard
  -- 1 Programmable I/O Group
  -- 1 Programmable Memory Space
- Provides Hot Plugging Events Detection
  -- Docking Insert
- Multiple External Wakeup Events of Standby Mode
  -- Power Button (Hotkey)
  -- Modem Ring
  -- RTC Alarm
  -- DRQ2

- Suspend Wakeup Detected
  - -- Modem Ring
  - -- RTC Alarm
  - -- Docking Insert
  - -- Power Button **(**Hotkey**)**
  - -- USB Events
  - -- IRQ
  - -- ACPWR
- Thermal Alarm Supported
- Clock Generator Control Logic Supported
  - -- CPUCLK Stop Control
  - -- PCICLK Stop Control
- L2 Cache Power Down Control Logic Supported
- 6 General Purpose Input Signals, 10 General Purpose Output Signals
- <u>16 Extended General Purpose Input Signals and 16 Extended General Purpose Output Signals</u>
- All Registers Readable/Restorable for Proper Resume from Suspend State

■ **Built-in PCI IDE Controller**
- Supports Ultra 33 DMA Mode Transfers up to Mode 2 Timing (33 Mbytes/sec)
- Supports PIO Modes up to Mode 4 Timings, and Multiword DMA Mode 0,1,2 with Independent Timing of up to 4 Drives
- Integrated <u>16 x 32-bit</u> Read Ahead & Posted Write Buffers for each channel (Total: <u>32 DWords</u>)
- Dedicated pins of ATA Interface for each channel
- Supports tri-state IDE signals for Swap Bay

■ **USB Interface**
- One Root Hub with <u>three</u> USB ports based on OpenHCI 1.0a specification
- Supports FS (12Mbits/sec) and LS (1.5Mbits/sec) Serial Transfer
- Supports Legacy Keyboard and Mouse Software with USB-based Keyboard and Mouse

■ **Super I/O Interface**
- Supports Windows 95 Plug-and-Play
- Supports 2 Serial/ 1 Parallel/ FDC/ 1 IR Functions
- <u>Supports 16-bit Address Decoder</u>
- 2.88 MB (Formatted) Floppy Disk Controller
  - -- Software Compatible with 82077 and Supports 16-byte Data FIFOs
  - -- High Performance Internal Data Separator
  - -- Supports Standard 1 Mbps/ 500 Kbps/ 300 Kbps/ 250 Kbps Data Transfer Rate
  - -- Supports 3 modes of 3.5" FDD (720K/1.2M/ 1.44MB)
  - -- Swappable Drives A and B

- Various modes of Parallel Port
  - -- Supports ECP/ EPP / PS/2 / SPP and 1284 Compliance
  - -- Standard Mode
  - -- <u>Multiplexing of FDC signals through Parallel Port pins</u>
  - -- <u>12 IRQ Channel Options</u>
  - -- <u>4 8-bit DMA Channel Options</u>
  - -- IBM PC/XT, PC/AT and PS/2 Compatible Bi-directional Parallel Port
  - -- Enhanced Mode
    - - Enhanced Parallel Port (EPP) Compatible
    - - <u>EPP Is Compatible with EPP1.9 (IEEE 1284 Compliant ), also supports EPP1.7 of Xircom specification</u>
  - -- High Speed Mode
    - - Microsoft and Hewlett Packard Extended Capabilities Port (ECP) Compatible
    - - <u>IEEE 1284 Compatible ECP</u>
    - - Includes protection circuit against damage caused when printer is powered up, or operated at higher voltages
- Serial Ports
  - -- Two high performance 16550 compatible UARTs with Send/Receive 16-byte FIFOs
  - -- Programmable Baud Rate Generator
  - -- MIDI (Musical Instrument Digital Interface) Compatible
  - -- Option between 12 IRQs for each device

- <u>Wireless Communications</u>
  - -- <u>Dedicated pins and COM Port for Infrared Transmission</u>
  - -- <u>Supports IrDA 1.0 (SIR) and IrDA 1.1 (MIR and FIR)</u>
  - -- <u>Supports Sharp-IR</u>
  - -- Option between 12 IRQs for each device

- High Performance Power Management for FDC, UART And Parallel Port

■ **SMBus Interface**
- System Management Bus Interface meets the V1.0 specification

■ **Hotkey for Power on Button function through Keyboard**

Underlined features means difference with M1543

■ **328-pin (27mmx27mm) BGA package**