Advance Information

This document contains information on a product under development.
The parametric information contains target parameters that are subject to change.

Bt832

CMOS Camera Video Processor

The Bt832 CMOS Camera Video Processor chip connects a QuartzSight™ CMOS color digital camera directly to video capture devices via an 8-bit, 4:2:2 YUV or YCrCb video interface. It is designed to connect to capture devices such as the Bt878 Single-Chip Video and Broadcast Audio Decoder for the PCI Bus. Additionally, it connects to several popular graphics controller devices. The RGB pixel data is received 4-bits at a time and undergoes several data processing steps such as defect correction, sharpness correction, color balance, and gamma correction before it is converted to 4:2:2 data. The chip is implemented in a 32-pin Thin Quad Flat Pack (TQFP) package and uses a 3.3 V and 5 V power supply.

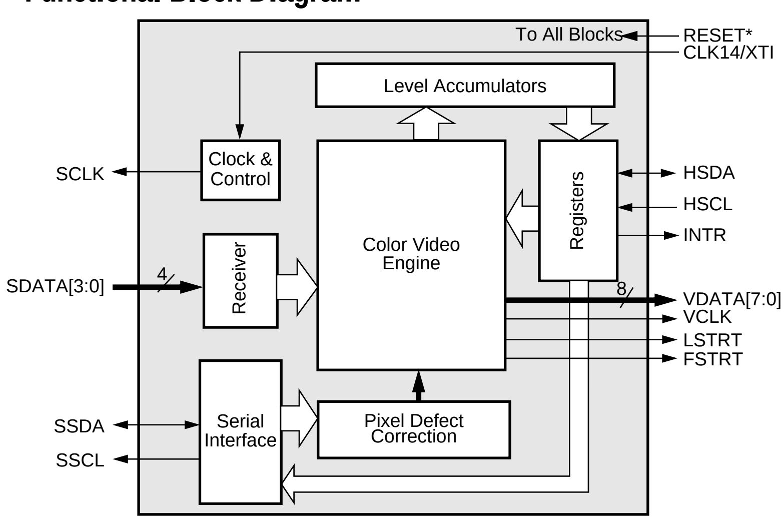
The video processor has logic which will automatically adjust the exposure time in the camera chip as well as adjust the color balance parameters in the video processor itself. If desired, the hardware control can be disabled and the exposure and color balance can be done in software.

The video processor corrects pixels which it determines to be defective based on a defect map. The defect map is stored in an EEPROM which comes with the camera module.

The 4:2:2 video data output to the capture device supports two types of interfaces. First, the horizontal and vertical timing information can be embedded as control codes in the 8-bit data stream. The codes are compatible with the CCIR656 standard. Second, the horizontal and vertical timing can be obtained from the LSTRT and FSTRT pins that are driven with the 8-bits of video data.

The video processor contains two distinct serial interfaces (I^2C). On one interface, the video processor is the master, and on the other it is a slave. It uses the master interface to program the camera sensor chip as well as to upload the camera's defect map. The slave interface is used by the CPU to program the video processors register. This is also how the host accesses the register in the QuartzSight camera sensor device.

Functional Block Diagram



Distinguishing Features

- 32-pin TQFP package
- 3.3 V and 5 V supply required
- Processes CIF image (352 * 288) at either 30 fps or 25 fps
- 4x4 color interpolation processor (4 line memories)
- 256 byte SRAM to allow correction of up to 128 defects
- RGB to video color space (YUV, YCrCb) matrix is programmable
- 4:2:2 data on 8-bit bus with CCIR656 compatible control codes
- Horizontal and vertical sync information on separate pins
- Registers are programmed through I^2C slave port
- Gamma correction
- Sharpness correction
- Bypass mode allows raw sensor data to be sent to capture device via an 8-bit port
- Automatic Exposure Control/Automatic Color Balance (AEC/ACB) logic included
- AEC/ACB logic can be disabled, allowing software to implement the functionality
- Interrupt pin provided to assist software handling of AEC/ACB

Applications

- Video e-mail
- Video conferencing
- Motion video capture
- Video editing
- Still-frame capture

Related Products

- QuartzSight Camera
- Bt878/879

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt832KTF	32-pin TQFP	0° C to +70° C

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1.0 Functional Description

1.1 Functional Overview

The Bt832 is a digital video processing module capable of outputting CIF-format 4:2:2-sampled digital video up to 30 frames per second. The module controls the 356 x 292 pixel color CMOS image sensor in the QuartzSight™ via a 9-wire interface. This interface incorporates the following functions:

- A 4-wire data bus (SDATA[3:0]) for receiving both video data and embedded timing references.
- A 2-wire serial interface (SSDA, SSCL) for controlling the camera.
- The clock for camera module (SCLK).
- VCC and GND power lines (7 to 12 V) regulated in the camera to give a +5 V. The Bt832 is not required to provide power directly to the camera. Camera power is derived from systems power supplies.

Each 8-bit pixel value is transmitted across the 4-wire data bus as a series pair of 4-bit nibbles, with the most significant nibble first. Along within the pixel data, codes representing the start and end frames and the start and end of lines are embedded within the video data stream to allow the receiver to synchronize with video data the camera module is generating.

The 2-wire camera serial interface provides complete control over how the sensor is setup and run. Exposure and gain values are programmed via this interface. A second 2-wire serial interface (the host serial I/F) is used to provide access to the Bt832 internal registers.

The video processing engine performs these basic functions on incoming data:

- Full color restoration at each pixel site from Bayer-patterned input data.
- Matrixing/gain on each color channel for color purity.
- Aperture correction for image clarity.
- Gamma correction.
- Color space conversion (including hue and saturation control) from RGB to YUV or YCbCr as required by H.320 image coders.

Level accumulators gather statistical data in assigned zones for processing by host software. This is the means by which end-of-frame housekeeping tasks such as exposure control and color balance are managed.

1.2 Pin Information

The Bt832 CMOS Camera Video Processor chip is packaged in a 32-pin TQFP package. Figure 1-1 illustrates the pinout diagram. Table 1-1 contains a description of the Bt832 pin functions.

Figure 1-1. Bt832 Pinout Diagram

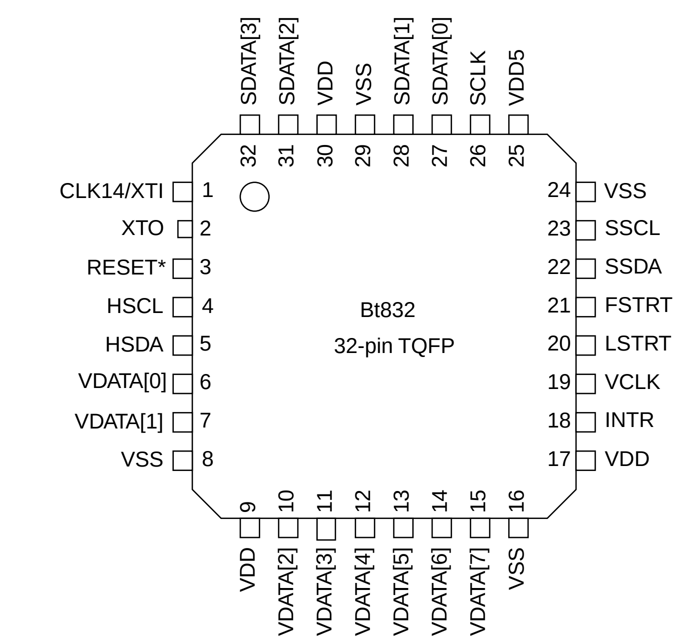


Table 1-1. Bt832 Pin List *(1 of 2)*

Signal Name	Pin Number	I/O[(1)]	Description
14.31818 MHz Master Clock			
CLK14/XTI	1	I	14.31818 MHz clock input. Connect single-ended oscillator source to this pin, or if using a crystal, connect one of it's terminals to this pin.
XTO	2	O	If using a crystal for the 14.31818 MHz clock, connect the other crystal terminal to this pin.
Camera Data Interface			
SDATA[3:0]	32, 31, 28, 27	I	RGB data from camera sensor module. Byte values are sent on this bus, 4 bits at a time.
SCLK	26	O	Clock to camera sensor module. Unlike the other outputs, this pin will swing 5 V to CMOS levels.

Table 1-1. Bt832 Pin List *(2 of 2)*

Signal Name	Pin Number	I/O(1)	Description
Serial Interfaces			
SSCL	23	O	Serial clock to sensor chip and camera defect EEPROM (I^2C).
SSDA	22	I/O	Serial data to sensor chip and camera defect EEPROM (I^2C).
HSCL	4	I	Serial clock from host device (I^2C).
HSDA	5	I/O	Serial data from host device (I^2C)
Output Interface to Video Capture Device			
VCLK	19	O	Video data clock to capture device.
VDATA[7:0]	15–10, 7–6	O	Output video data in 4:2:2 format to video capture device.
LSTRT	20	O	Line start for horizontal timing reference for video data.
FSTRT(2)	21	O	Frame start for vertical timing reference for video data. Also, the state of this pin (internal driver disabled) is sampled during reset to configure the serial address that the chip will respond to. An external pull-up resistor should be added to FSTRT to configure the device to respond to a host I^2C address of ad[7:1] = 1000101b rather than the default 1000100b.
INTR	18	O	Interrupt to host. The interrupt is generated on exception conditions as well as on frame boundaries.
Reset			
RESET*	3	I	Chip Reset. When driven low, resets all registers to default state and disables all of the chips output drivers.
Power and Ground			
VDD	9, 17, 30	P	3.3 V power supply.
VDD5	25	P	5 V power supply for SCLK output pad.
VSS	8, 16, 24, 29	P	Grounds.

Notes: (1). The I/O designation refers to the functionality of the signal pin only. The I/O buffers may have additional functionality for test or other purposes. The designations are as follows: I = Input, O = Output, I/O = Bidirectional, P = Power/Ground pin.
(2). Serial address configuration.

1.3 Receiver Interface

The purpose of the receiver is to decode digital data from the QuartzSight camera module, ensuring that camera and Bt832 remain in synchronization. Communication errors, should they occur, are flagged to the host.

1.3.1 Overview

The Bt832 block receiver (including clock generator) manages the detection of a QuartzSight camera device and the automatic selection of optimum input data-nibble sampling phase (or its override by the host system). The downstream Bt832 engine clock is generated according to this selection, along with certain key control signals.

After establishing nibble-synchronism with incoming data, the receiver then detects certain embedded codes to establish byte-synchronism and then parses the incoming data stream, stripping out control codes and passing pixel data on to the Bt832 engine along with qualifying signals. A list of possible errors is detected and flagged by the receiver.

1.3.2 Receiver Operational Modes

The Bt832 provides some user configurability of the receiver module, which includes controlling the frame rate through clock division.

Input Sampling Phase (*Phase[1:0]*)

A circuit automatically detects a sequence of alternating 1 and 0 data from the sensor during the start-up sequence. This resolves the uncertainty of the optimum sampling phase on incoming data. Using both edges of the system's fast clock, four candidate phases are evaluated and a polling circuit selects the optimal phase. The Bt832 status flag phase_error denotes successful phase selection, and if set and an error interrupt is generated. The host must override the clock phase selection.

Host Override of Input Sampling Phase (*Phase Override*)

In emergencies, for example when the Bt832 reports failure to phase lock via the Bt832 status flag phase_error, the host may set this bit and write a trial value into PHASE[1:0]. This is done after issuing a reset, before waking up the camera. The Bt832 will, in this instance, start-up using the external phase setting.

Frame Rates (*clkdiv[1:0]* and *Frame Rate Select*)

The sensor is capable of generating two frame rate classes: 30 fps and 25 fps.

The number of video lines in for each frame rate is the same (304). The slower frame rate is implemented by extending the line period from 393 pixel periods to 471 pixel periods. Sub-multiples of these rates can be generated by clock division, under control of the 2-bit parameter clkdiv (Table 1-2).

Table 1-2. Frame Rate Selection

Frame Rate Select (1)	Frame Timing (Pixels x Lines)	clkdiv	Frame Rate (fps)
0	471 x 304	0	25
		1	12.5
		2	6.25
		3	3.125
1	393 x 304	0	30
		1	15
		2	7.5
		3	3.75
Notes: (1). Bit 3 of register 57 (see Table 2-17).			

1.3.3 Hot Plug

The Bt832 supports the capability to both hot plug and hot unplug the camera. There are two relevant register bits that support this. A camera_present bit in the CAM_STATUS register shows in an absolute sense whether a camera is connected or not. A camera_x bit in the VP_STATUS register is set whenever there is a change in the camera_present status. The setting of the camera_x bit generates an interrupt. Thus, an interrupt is generated whenever a camera is connected or disconnected. The interrupt is only cleared when the camera_x register bit is reset to zero by a host register write.

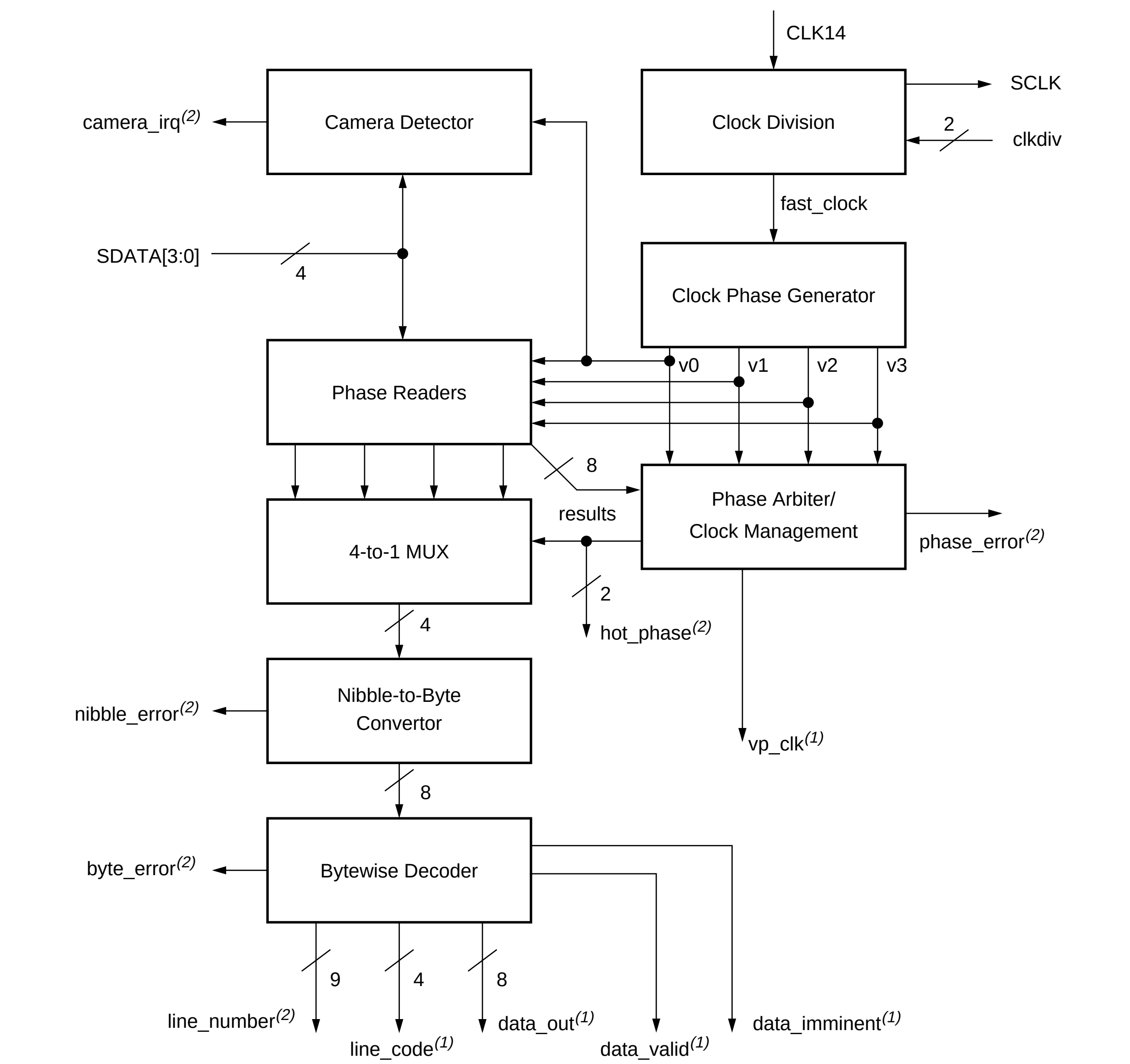
The camera_present bit is reset to one. However, after reset, this status is not guaranteed to valid until the low_power mode bit is cleared in the CAM_SETUP0 register, thereby waking up the receiver module. Therefore, software should ignore both the camera_present bit and camera_x interrupts until it clears the low-power bit in CAM_SETUP0 register.

After a plug or connect event has been detected, software should reset the Bt832 (through software control of the RESET* pin). This is necessary to upload the EEPROM defect map. After the reset, software can repeat its standard initialization routine.

1.3.4 Data Nibble Interface

The Bt832 receiver supplies the Camera Clock (SCLK) and uses embedded control sequences from the QuartzSight module to synchronize with the frame and line level timings. Thus the receiver and sensor synchronize to derivatives of the same fundamental clock (14.31818 MHz). During its power-up sequence the sensor outputs a 101010... sequence on each of its databus lines for the receiver to synchronize. This allows the receiver to determine the best sampling position of the video data.

Figure 1-2. Receiver Block Diagram



Notes: (1). These bits are connecting to the Video Engine.
(2). These are status indication only.
3. All lower-case signal names denote internal signals only.

The video data interface consists of a unidirectional, three-stateable 4-wire databus. 8-bit digital video data is transmitted as serial pairs of parallel 4-bit nibbles (most significant nibble first). Nibble transmission is synchronized to the rising edge of the system clock.

Control information, including both video timing references and sensor status/configuration data, is multiplexed with the sampled pixel data (see Table 1-3). Video timing reference information takes the form of field start characters, line start characters, end of line characters, and a line counter.

Table 1-3. Video Encoding Parameters

Form of Encoding	Uniformly Quantized, PCM, 8 Bits per Sample
Correspondence between video signal levels and quantization levels	225 quantization levels with the video black level corresponding to code 16 and the peak white level corresponding to code 240 (CCIR-601 levels). Internally, valid pixel data is clipped to ensure that 00_H and FF_H values do not occur when pixel data is being output on the data bus.

1.3.5 Detection of Camera Using Data Bus State

The Bt832 has internal pull-down terminations on the data bus. On power-up the sensor will pull all data lines high until a wake-up message is sent to the sensor via the serial interface. The Bt832 can detect the presence of a sensor on the interface on power-up, or the connection of a sensor to an already powered-up interface (a hot connection).

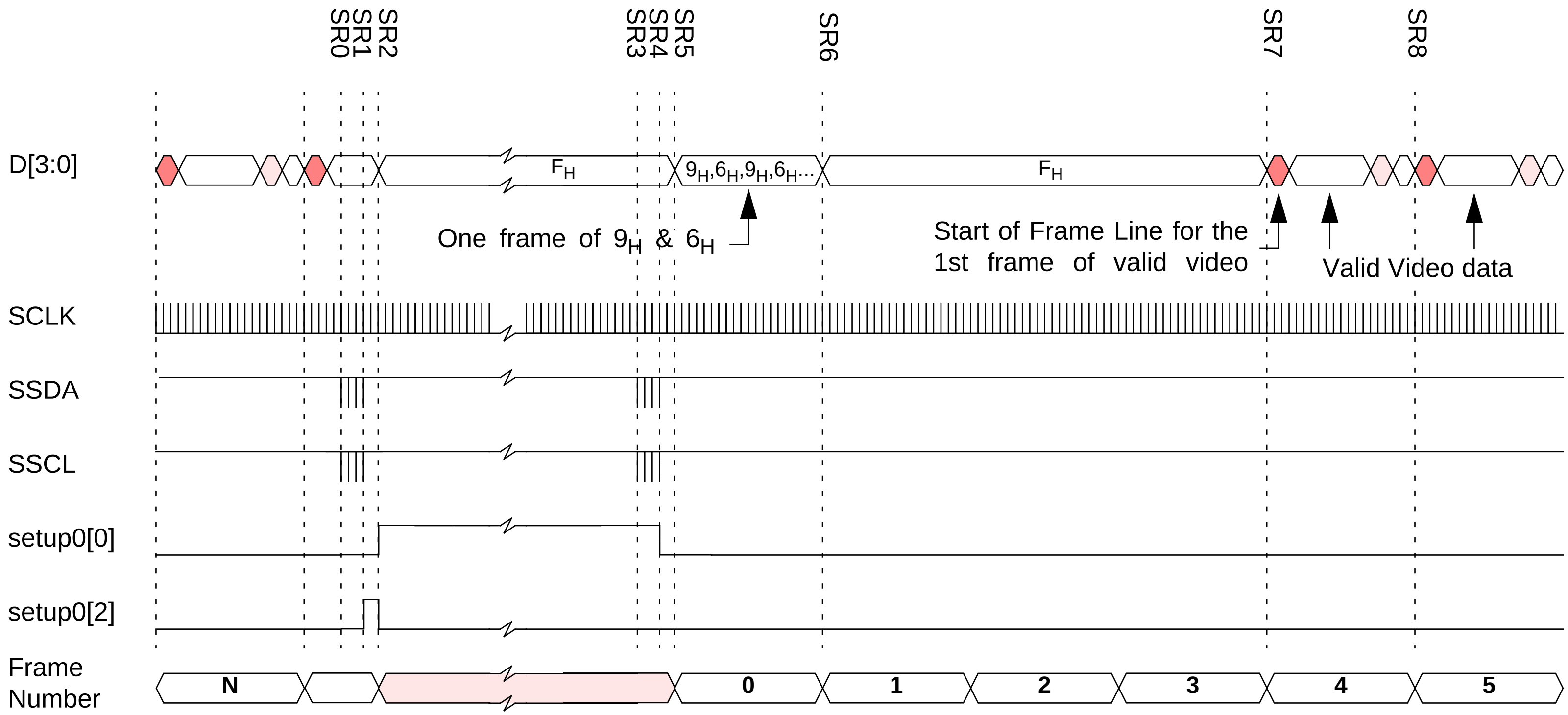
The absence of a camera is detected by the Bt832 upon seeing more than 32 consecutive nibbles of 0_H on the data bus. The presence of a sensor is detected by the Bt832 upon seeing more than 32 consecutive nibbles of F_H on the data bus.

The SCLK is always enabled.

1.3.6 Resetting the Camera Via the Serial Interface

Bit 2 of CAM_SETUP0 register (register 57) allows the QuartzSight sensor to be reset to its power-on state via the 2-wire serial interface. Setting this soft reset bit causes all of the serial interface registers including the soft reset bit to be reset to their default values. Soft reset leaves the sensor in low-power mode and thus an exit low-power mode command must be issued via the serial interface before the sensor will start to generate video data. Figure 1-3 illustrates a soft reset via the serial interface.

Figure 1-3. Resetting the QuartzSight Camera via the Serial Interface



SR0-SR1	Soft-reset command. At the end of the command the sensor is reset and enters low-power mode.
SR2	The sensor enters low-power mode.
SR3-SR4	Exit low-power mode command. Powers-up analog circuits and initiates the QuartzSight sensor’s 4-frame start-up sequence.
SR5-SR6	One Frame of alternating 9_H & 6_H data on D[3:0] for the Bt832 to determine the best sampling phase for the nibble data (D[3:0]).
SR7-SR8	Four Frames after the exit low-power mode command, the sensor starts outputting valid video data.

1.3.7 Power-Up, Low-Power and Sleep Modes

To clarify the state of the interface on power-up, including the case of a hot connection of the interface cable, the power-up state of the bus is defined in the following paragraphs.

Power-Up/Down

On power-up or hot-plug, all of the input databus lines will immediately go high (F_H) to indicate that the device is present. The device enters low-power mode.

When the Bt832 is reset, the following sequence is executed to ensure that the QuartzSight starts to generate video data. After the Bt832 has been released from reset, the camera clock is enabled immediately.

1. After waiting for 16 SCLK clock cycles, a soft reset command is issued to the camera. This ensures that the camera is brought into a known state. If the camera is not present, the serial interface communications by Bt832 will not be acknowledged.
2. If the serial CMOS E^2PROM containing the defectivity map for the camera is present, down-load the values.
3. To enable video data, the host software must clear the *low-power* mode bit. It should also clear the skip bit in *vp_control1*.

After the exit low-power mode command has been sent, the camera will output (for one frame) a continuous stream of alternating 9_H and 6_H values on SDATA[3:0]. By locking onto the resulting 0101/1010 patterns appearing on the data bus lines the Bt832 can determine the best sampling position for the nibble data. After the last 9_H 6_H pair has been output, the databus returns to F_H until the start of fifth frame after SCLK has been enabled when the first active frame is output. After the Bt832 has determined the correct sampling position for the data, it waits for the next Start of Frame line (SOF).

If the Bt832 detects 32 consecutive 0_H values on the data bus, then the camera has been removed. Table 1-4 displays the system power-up procedure.

Table 1-4. System Power-Up or Hot-Plugging Device Behavior

States	Description
1	System power-up or camera hot-plugged.
2	Camera internal-on reset triggers, the sensor enters low-power mode and SDATA[3:0] is set to F_H.
3	Bt832 released from reset, Bt832 enables the sensor clock.
4	At least 16 SCLK clock periods after SCLK has been enabled the Bt832 sends a soft-reset command to the sensor via the serial interface. This ensures that if a sensor is present, it is in low-power mode.
5	On detecting 32 consecutive F_H values on SDATA[3:0], the Bt832 sets camera_present high.
6	If present, upload the sensor defect map from E^2PROM into the Bt832.
7	Upon detecting completion of the defect map upload, the host triggers the Bt832 to send the exit low-power mode command to the sensor via the serial interface. This initiates the sensors 4 frame start sequence.
8	One frame of alternating 9_H and 6_H data on SDATA[3:0] for the Bt832 to determine the best sampling phase for the nibble data (SDATA[3:0]).
9	Four frames after the exit low-power mode is set through the serial interface, the sensor starts to output valid video data.

Low-Power Mode

Under the serial interface control, the sensor analog circuitry can be powered down and then powered-up. When the low-power bit (bit 0, register 57) is set via the I^2C serial interface, all the databus lines will go high at the end of the EOF line of the current frame. Then the analog circuits in the sensor will power down. The sensor clock remains active for the duration of low-power mode.

Only the analog circuits are powered down; the values of the serial interface registers, such as exposure and gain, are preserved. The sensor's internal frame timing is reset to the start of a video frame on exiting low-power mode.

In a similar manner, the second frame after the serial communications contains a continuous stream of alternating 9_H and 6_H to allow the Bt832 to re-confirm its sampling position. Three frames later the first start of frame line is generated.

NOTE: Exiting from low-power mode does not automatically trigger the optimum phase detection. Soft-reset should be used instead.

Sleep Mode

Sleep mode is similar to low-power mode, except that the sensor's analog circuitry remains powered. When the sleep bit (bit 1, register 57) is set via the I^2C serial interface, the pixel array is put into reset and the data lines will go high at the end of the current frame. Again the system clock remains active for the duration of sleep mode.

When sleep mode is disabled, the sensor's frame timing is reset to the start of a frame. During the first frame after exiting from sleep mode the databus will remain high while the exposure value propagates through the pixel array. At the start of the second frame the first SOF line will be generated.

System Clock Application During Camera Low-Power Modes

The Camera Clock (SCLK) remains active for the duration of low-power and sleep modes. The SCLK is active except when the reset pin is asserted.

1.3.8 Embedded Control Code Sequences

To distinguish the control data from the sampled video data, all control data is encapsulated in embedded control sequences. These are a minimum of six words long and include a combined escape/sync character, one control word (the command byte) and two words of supplementary data.

To minimize the susceptibility of the embedded control data to random bit errors, redundant coding techniques have been used to allow single bit errors in the embedded control words to be corrected. However, more serious corruption of control words or the corruption of escape/sync characters cannot be tolerated without loss of sync to the data stream. To ensure that a loss of sync is detected, a simple set of rules has been devised. The four exceptions to the rules are outlined below:

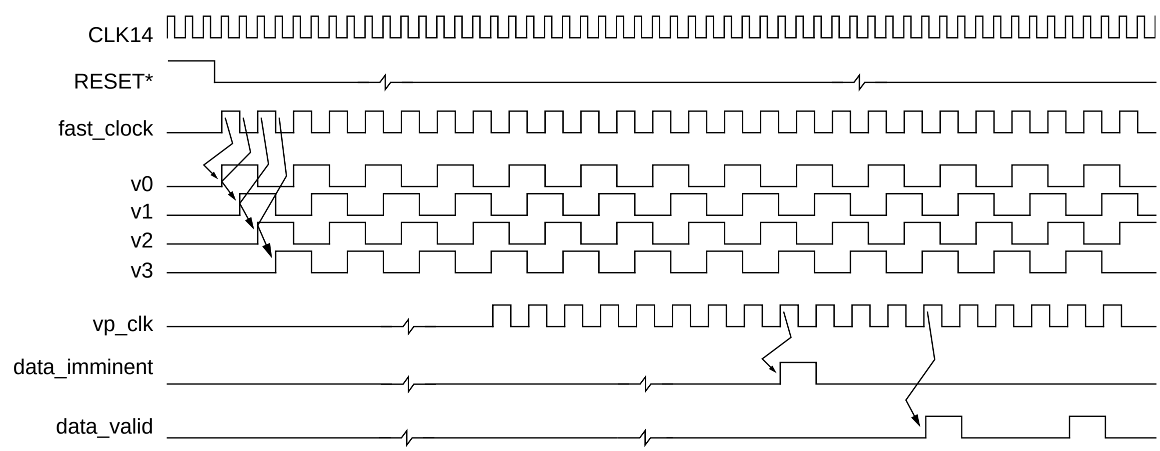
1. Data containing a command word that has two bit errors.
2. Data containing two end of line codes that are not separated by a start of line code.
3. Data preceding an end of frame code before a start of frame code has been received.
4. Data containing lines that do not have sequential line numbers (excluding the end of frame line).

If the receiver detects one of these violations, it raises the INTR pin, sets the data_corrupt flag in the VP_STATUS register, and abandons the current frame of video.

1.3.9 Clock and Control Generation

The receiver block generates the clocks for both the video engine and the sensor. Figure 1-4 shows the clock output for the case where clkdiv = 1 (for example, fast clock is half the 14.31818 MHz master frequency) and v3 is the selected phase. The sensor clock is always a gated version of v0. The vp_clk is either the fast_clock (hot_phase = 0 or 2) or an inverted copy (hot_phase = 1 or 3). The two controls shown are derived from the rising edge of this clock, as is the output data (see Figure 1-4 and Figure 1-13).

Figure 1-4. Clock and Control Generation



Note: All lower-case signal descriptions denote internal signals only.

1.3.10 Resets

The receiver is reset both by the RESET* pin and by setting the soft reset bit (bit 2 of register 57) in the camera setup register. The latter is detected by the Bt832 before the contents of the register are sent to the camera over the serial interface.

1.3.11 Error Conditions and Procedures

The receiver generates four error flags, under these conditions.

camera _present First task of the receiver module on power-up is to check for presence of a camera, denoted by 32 or more samples of F_H on SDATA. Thirty-two or more samples of 0_H indicate the absence of a camera. If no camera is detected, the camera_present bit in register 54 (Camera Status) is set and the receiver idles, while it is idling, it continues to test for the presence of a camera. Clock and control outputs to Bt832 are suppressed unless the self timing bit is set. An interrupt is also generated whenever there is a change in the camera_present bit. This type of interrupt sets the camera_x bit in the VP_STATUS register.

phase_error The next task of the receiver module in the power-up sequence is to select the optimum input sampling phase. To assist in this selection, the camera outputs an entire frame of $9_H6_H9_H6_H9_H6_H$.... data sequence. The receiver's phase detector and arbiter choose the optimum sampling phase, and output the chosen phase on the 2-bit status line hot_phase[1:0]. If phase selection should fail for any reason, the phase_error flag is set and the receiver reverts to the default phase (0, aligned with sensor clock). In this state, the receiver is susceptible to host override of the phase setting, and must continue operation with this setting. Whichever phase is chosen, incoming data is re-timed accordingly.

nibble_error Next task of the receiver module on power-up is to establish byte-synchronism, because nibble-pairs are inherently ambiguous. The camera outputs a transition (....$F_HF_H0_H0_H$....), as part of the Start of Active Video (SAV) sequence embedded in every line. This is decoded as contiguous bytes F_HF_H and 0_H0_H. Flywheel synchronism is maintained line-to-line, and upon loss of byte-synchronism (denoted by an unexpected F_H0_H transition) the nibble_error flag is set and the frame abandoned. The receiver module must re-synchronize to this incoming code, making the necessary adjustments to control signal generation in readiness for the next frame. The next start of frame line code clears the nibble_error flag.

byte_error The last and highest semantic level is contained in the byte-wide data, comprising null codes, control codes, supplementary data and video data. As video data is restricted to the decimal range 16-240, control codes can be easily stripped out. Some redundant coding is included for error detection and partial correction, but the receiver takes no action beyond this to recover from semantic errors. The byte_error flag (bit 2 of register 52) is set and the frame abandoned. The next SOF line code clears the byte_error flag. See QuartzSight datasheet for more comprehensive treatment of semantic errors.

1.3.12 Sampling Phase Optimization

Input data transitions are associated with the rising edge of SCLK. The delay between the receiver supplying a rising clock edge and the data on the databus becoming valid is a function of several indeterminate system parameters, such as the length of the cable between the sensor and the receiver. To allow the receiver to find the best sampling position for the data nibbles, the sensor can be forced to output 9_H, 6_H, 9_H, 6_H,.. values continuously.

The receiver contains a polling circuit to identify the best of four candidate sampling phases. In the unlikely event of selection failure, an interrupt is generated and the phase_error flag in the VP_STATUS register is set. In this case, the user must either issue a soft reset thereby restarting the process, or manually select a sampling phase.

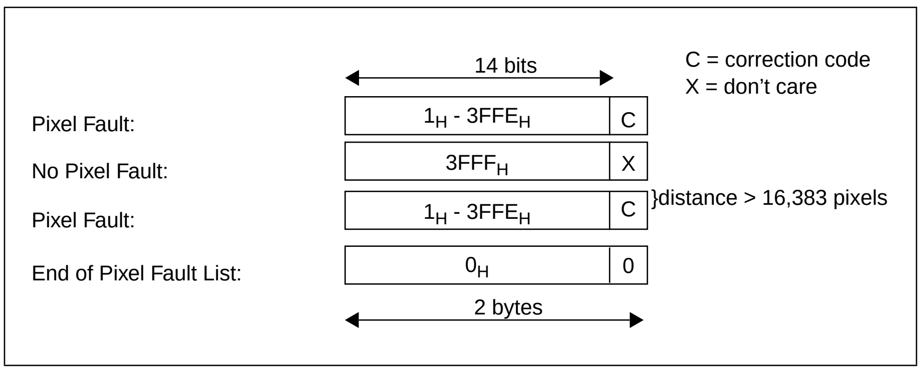
1.3.13 Pixel Defect Correction

To allow the receiver to correct single pixel defects in the sensor array, the QuartzSight module can be supplied with a 2-wire serial CMOS E^2PROM (Atmel AT24C Series) containing the defect map for each sensor. The defect map is programmed into the serial CMOS E^2PROM as part of the module test procedure.

As part of the startup sequence the receiver looks to see if the serial E^2PROM is present. If it is, the receiver downloads the defect map.

The receiver contains storage for up to 127 defects.

Figure 1-5. Pixel Defect Correction Codes for the Serial E^2PROM



The defect map takes the form of a variable length list of 2-byte (word) pixel faults. The end of the list has been marked with two all-zero words. The distance from the previous fault or the beginning of frame is encoded in unsigned binary, and if greater than 16,383 ($3FFF_H$), more than one word is used.

NOTE: The distance to the first pixel is one.

The two least significant bits of the word specify the type of correction applicable to the fault at the start of the distance associated with the code. A description of the codes is shown in Table 1-5.

Table 1-5. Defect Correction Codes

Length	Code	Function
$X<3FFF_H$	00	“Sombrero” correction algorithm.
$X<3FFF_H$	01	Insert bright pixel (Y=254).
$X<3FFF_H$	10	Copy from left pixel.
$X<3FFF_H$	11	Copy from right pixel.
0	X	Last (of two) entry of defect list.
$3FFF_H$	0	No fault, distance greater that 2^{14}.

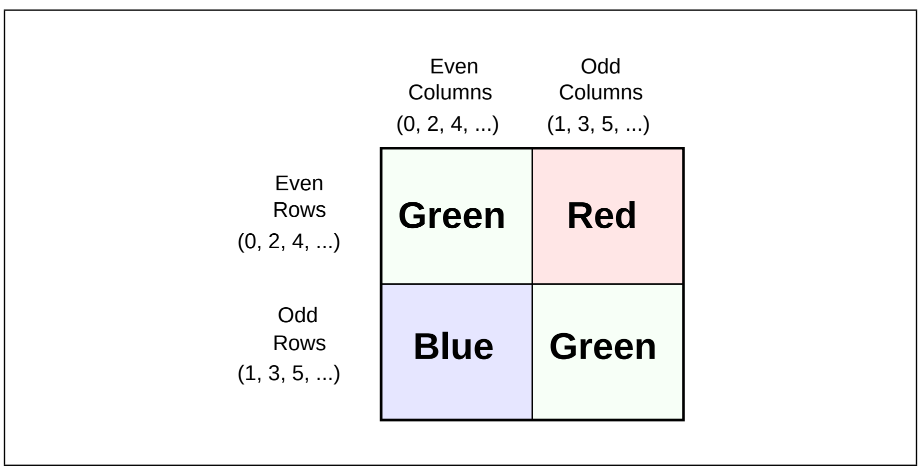
1.4 Video Engine

1.4.1 Bayer Pattern Overview

Before describing the Bt832 Video Engine, it is worthwhile to describe the Bayer Pattern. The Bayer Pattern is the expected colorization pattern of Bt832 input data. Instead of providing a trichromatic sample at each pixel site, the Bayer Pattern provides a single colorized sample. This simplifies sensor layout, reduces transmission bandwidths, and increases relative light-gathering area, at the cost of reduced resolution. This reduction in resolution is not equally distributed over the three-color channels: one channel is chosen as ‘luminance representative’, and is rendered as a checkerboard pattern, sub-sampled at 50 percent. The other two channels, each sub-sampled at 25 percent, fill in the spaces in the checker-board, alternating in rows and columns. The QuartzSight uses green as the luminance representative, and red and blue as the other colors. Figure 1-6 shows the fundamental tiling element of the Bayer Pattern.

Note that the manufacturing processes may result in consistently different responses in odd and even-row greens. If any correction applies, the Bayer output should have 4 channels, each sub-sampled at 25 percent. To minimize time-domain interference between transmitted samples, the sensor unshuffles each Bayer row into two groups of contiguous constituent colors. By transmitting in this color-bunched fashion, the sensor can eliminate cross-talk between the color channels that can exist in the analog domain within the camera.

Figure 1-6. Bayer Colorization Pattern



1.4.2 Function and Architecture

The Bt832 Video Engine converts data from a bayer input pattern format, into YUV/YCrCb 4:2:2. It is highly programmable, although fixed in terms of gross function. The parameter set resides in a shadow register bank, accessible to the serial interface. While most parameters are set by the host application on power-up, some are updated regularly by the host application. These dynamic parameters can be further categorized as user-parameters (adjustable on user request) and application parameters (adjusted automatically by the application, transparently to the user). Figure 1-7 illustrates the Block Diagram of Video Engine.

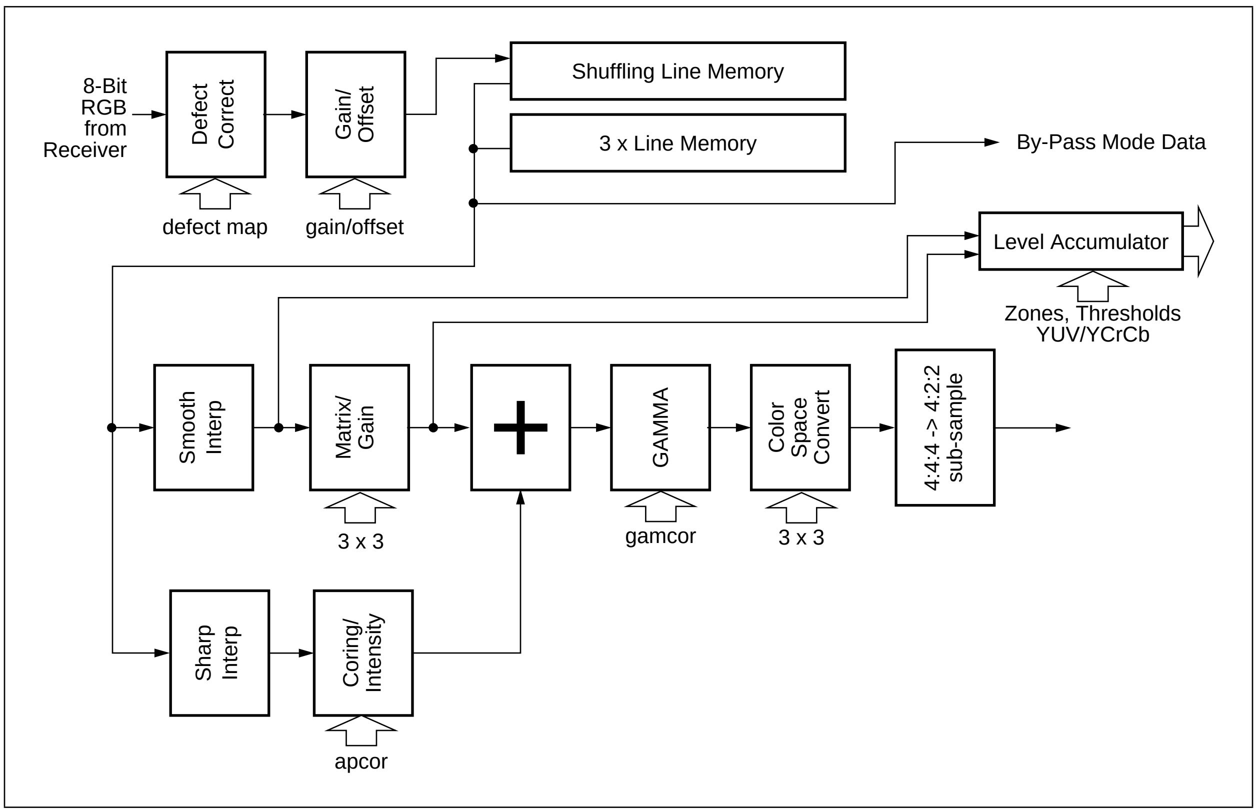
Input Processor

The dataflow (Figure 1-7) begins with an input processor, which corrects defective pixels by horizontal interpolation according to a list downloaded via the receiver. The input processor is also capable of applying a fixed offset, and four gains (one per Bayer channel). If the Bayer gain is denoted as c’, then each effective gain can be calculated by the equation:

$$c' = 2 * (1 + c/128)$$

where c is the value programmed into the input gain register. The value c is an 8-bit 2’s complement variable (–128 to 127). All four default values are 0xC9 (hex), or c = –55 and c’ = 1.141. This default assumes a sensor output range of 16 to 240.

Figure 1-7. Block Diagram of Video Engine



Line Memories

A 4-line memory lies between the input and main processors, capable of re-shuffling input data to its original spatial distribution. Access to line-history allows the spatial neighborhood transforms (necessary for interpolation back to 100 percent population) to be applied to incoming data.

Interpolation

The green channel (no longer containing responses of even and odd rows) is treated differently from red and blue. It is interpolated into two output representations, one sharper (containing more detail) than the other.

Unsharp Masking

Subtraction of these two green representations creates an unsharp mask, which can be further processed before returning to the main color flow.

Matrix/Gain

The main color flow results from a 3 x 3 matrix multiplication on the smooth RGB channels. They have two main roles to play: matrixing (mapping of Bayer pixel taking chromaticities onto nominal display chromaticities) and color balance (channel gains). The matrix is derived from values programmed in the M00 through M22 registers. The host must compute the values to program in these registers in one of two ways, depending on whether the coefficient is on-diagonal or not (diagonals are M00, M11, and M22). On-diagonal coefficients are calculated as:

$$c' = 2*(1+c/128)$$

where: c is the 8-bit 2's complement variable (–128 to 127) in the register. In contrast, off diagonal coefficients are calculated as:

$$c' = 2*c/128$$

The on-diagonal coefficients have a default of 0xC0 (c = 0.5, c' = 1).

Gamma Correction

A programmable gamma correction stage produces the non-linear distortion of data amplitudes required for various video communication standards. It also provides cosmetic enhancement of image detail under user control. The Bt832 provides 16 curves, all to 9-bit accuracy (see Figure 1-9), linear (GAMCOR = 0), SMPTE-240M (GAMCOR = 8, approximating a gamma of 2.2), an additional seven by interpolating between linear and SMPTE-240M, and a final seven by extrapolation beyond SMPTE-240M. See "GAMCOR [register 20]", page 38.

Color Space Conversion

Further cosmetic enhancement (of hue and saturation) is possible by reprogramming the color-space conversion matrix. The color space conversion matrix is derived from values programmed into the CSC00 to CSC22 registers.

Some interpretation of the color space matrix coefficients computed and transmitted by the host is performed in the Bt832. This is done to maximize the accuracy of multiplications in the color space conversion, while restricting coefficient sizes to 8 bits. The top row of the matrix, which computes luminance according to ITU-R-BT601, achieves this by multiplying gamma corrected values R'_{255}, G'_{255} and B'_{255} by:

$$c' = c/256 + 0.25,$$

where: c is the 8-bit 2's complement value in the programmable csc register and c' is the effective coefficient. The other two rows, which compute chrominances Cb and Cr, respectively (or U and V), multiply gamma corrected values R'_{255}, G'_{255}, and B'_{255} by:

$$c' = c/256,$$

where: c is the 8-bit 2's complement number programmed into the CSC register and c' is the effective coefficient. This supports wider number ranges for hue and saturation control from the host. The recommended conversion matrix for gamma-corrected RGB to YCrCb is shown in Figure 1-8.

Figure 1-8. Recommended Conversion Matrix

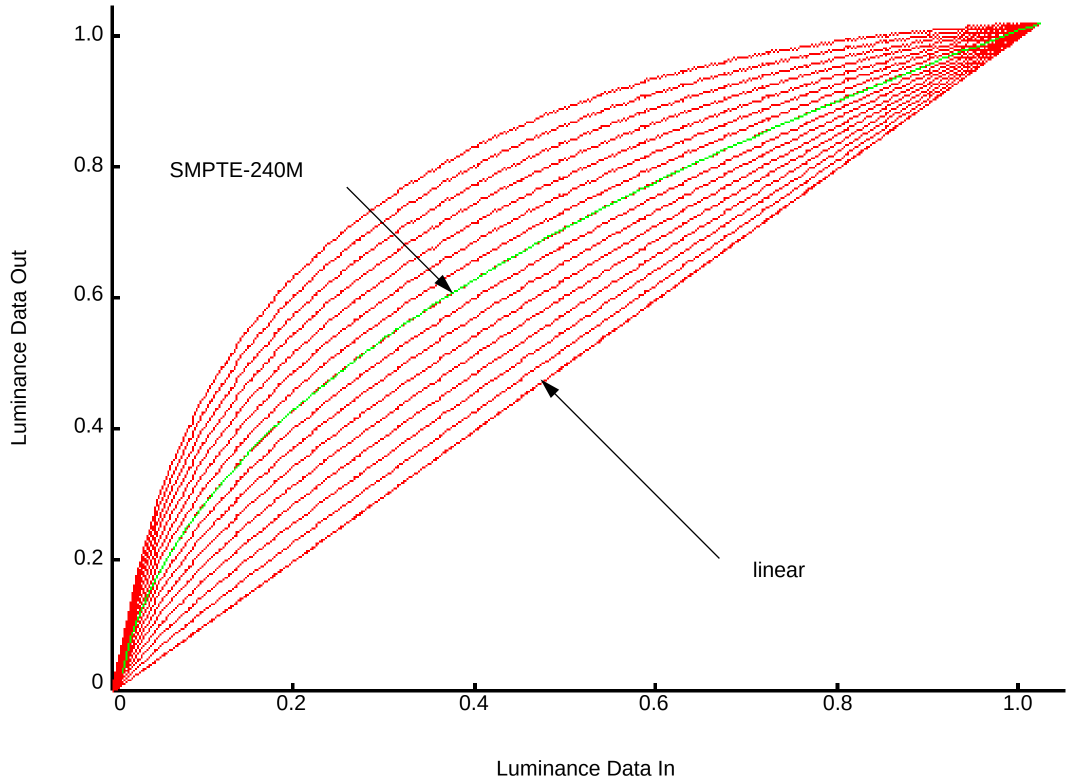
1) ITU-R-BT601 conversion equation

$$\begin{bmatrix} Y \\ Cb \\ Cr \end{bmatrix} = \begin{bmatrix} 16 \\ 128 \\ 128 \end{bmatrix} + \frac{1}{256} \underbrace{\begin{bmatrix} 66 & 129 & 25 \\ -38 & -74 & 112 \\ 112 & -94 & -18 \end{bmatrix}}_{c'} \bullet \begin{bmatrix} R'_{255} \\ G'_{255} \\ B'_{255} \end{bmatrix}$$

2) Recommended conversion matrix
(8-bit, 2's complement coding)

$$\underbrace{\begin{bmatrix} 0x02 & 0x41 & 0xD9 \\ 0xED & 0xDB & 0x38 \\ 0x38 & 0xD1 & 0xF7 \end{bmatrix}}_{c}$$

Figure 1-9. Video Processor's 16 Selectable Gamma-Correction Curves



Note: Luminance data normalized for maximum white = 1.00.

1.4.3 Level Accumulator

The level accumulator stores the luma samples, represented by the raw (pre-matrix) green channel. This sum is weighted according to the zone value ZONECODE[3:0] set for each of the 16 zones in the image, and scaled/rounded/windowed according to ACCSCALE. The result is found in register EXP_ACC.

The level accumulator is also programmed to gather statistics on the three smooth color channels, post-matrix. These statistics, named RACC, GACC, and BACC, consist of accumulations of signal samples over a set threshold THRESH and find use in color balance control.

A third level accumulator function, used to support software-based flicker-reduction mode, gathers line accumulations over 8 lines. They are spaced apart by the LINESPACE bits in register VP_CONTROL2. These accumulations reside in registers LACC0, etc.

Finally the black lines are monitored and their average stored in BLACK_ACC.

1.4.4 Line Output Format

The sub-sampled 4:2:2 output associates a chrominance pair (Cb/Cr) with every other luminance sample, as shown in Figure 1-10. The chrominance pair is sub-sampled only horizontally. No line memory is required for computing of chrominance values. Chrominance sub-sampling is achieved by averaging the two original samples co-sited with the previous and next luminance samples, then further averaging with the current co-sited chrominance sample.

Indices in Figure 1-11 refer to the horizontal dimension of the appropriate output image size. After 4:2:2 sub-sampling, Y-image dimensions are twice those of Cb and Cr.

Figure 1-10. 4:2:2 Sampling

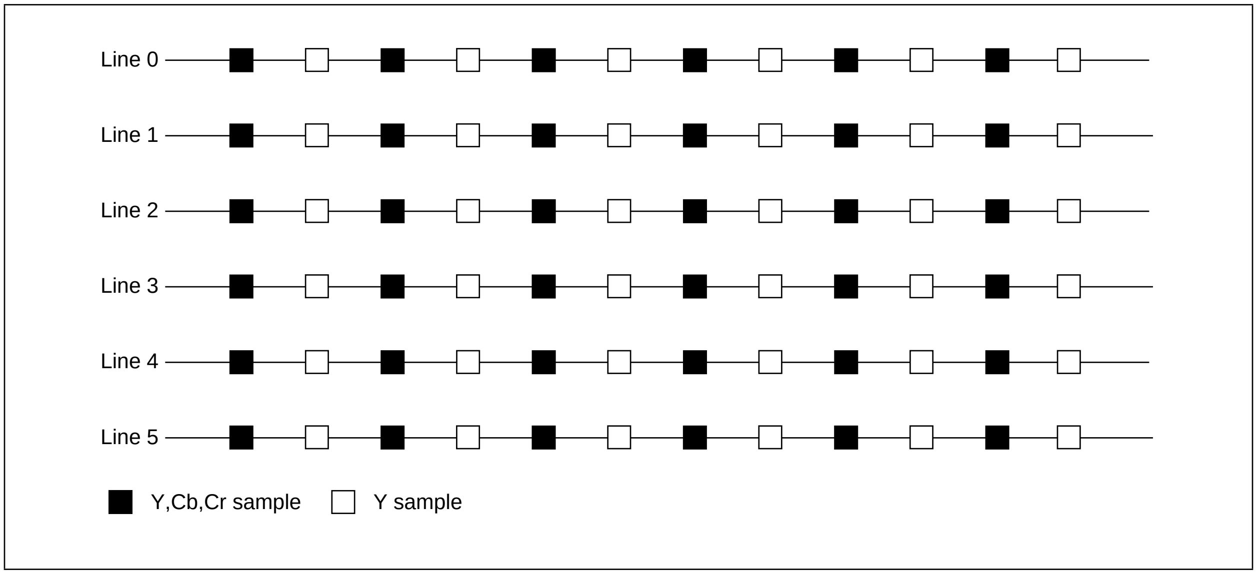
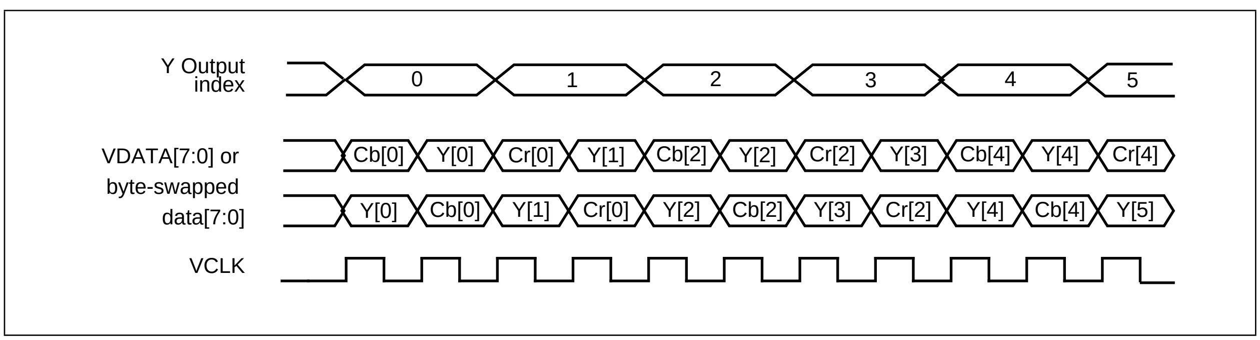


Figure 1-11. Bt832 Line Output



1.4.5 Operational Modes

The Bt832 has several distinct, operating modes, programmable via the registers VP_CONTROL0 and VP_CONTROL1.

Image Size (*QCIF*) The output image format can be CIF or QCIF, as shown in Table 1-6. In both cases, output images are derived by interpolation from an input 356 x 292 bayer-patterned image. The extra pixels in the input image are required to form a border for interpolation, and input lines are delivered in color-bunched (shuffled) form to manage signals in the time domain.

Table 1-6. Output Image Format Selection

QCIF	Y Image Size (col x row)	Cb,Cr Image Size (col x row)
0	352 x 288	176 x 144
1	176 x 144	88 x 72

Matrix Coefficient Interpretation (RGBmatrix) To save on device registers, two sets of matrix coefficients (9 registers) share the same address space: M00 etc. One set is applied for color correction and color balance, the other for color space conversion and control of hue and saturation. The RGBmatrix flag is the means by which the host ensures the correct destination for matrix coefficient sets (Bit 1 of register 40, see Table 2-6).

Bayer Pattern Interpretation Controls (HJOG, VJOG and EVENFIRST) Some flexibility is provided for the interpretation of Bayer channels. Any Bayer channel as depicted in Figure 1-6 can represent the origin for purposes of interpretation. The QuartzSight and the Bt832 default use 0,0 (even, green) as origin. If HJOG is set, the interpretation origin moves horizontally by one pixel. If VJOG is set, the interpretation origin moves vertically. If EVENFIRST is set, the first half-color group in any line is processed as even-indexed, if EVENFIRST is not (default), as odd-indexed.

Spacing of Line Accumulations (LINESPACE) The Bt832 is capable of flicker-reduction, given suitable exposure and gain parameters from the host. To allow the host to estimate flicker, eight spaced single-line accumulations are provided by the Bt832 on registers LACC0, etc. The spacing of these accumulations along the vertical dimension of the image is controlled by the 4-bit LINESPACE parameter, which scans the range 1 to 16, as coded with an increment.

Automatic Exposure Control The Bt832 has two automatic control mechanisms to adjust the picture brightness and white color balance, according to lighting conditions. It computes a set of accumulations of the pixel values and modifies the settings of exposure values (coarse, fine and gain on the camera) and the RGB matrix. The user may choose to disable these adjustments and overwrite the values either after reading the same set of accumulations or by calculations over the image data.

The exposure algorithm reads the EXP_ACC register, which is the average of all luma (Y) samples. The luma (Y) are read before color space conversion and weighted, using the zone codes *(*ZONE *0–3)*. The total is divided by a power of two (2^n), which is determined by the ACCSCALE in VP_CONTROL2 (register 21). See also "Mono Accumulation [register 30]", page 39.

The average is then compared against two programmable thresholds (AEC_TH and AEC_TL) and changes the exposure by a small percentage, until a certain average value is reached (AEC_TC). The exposure control algorithm is activated again when the average is outside these thresholds.

The exposure is increased or decreased by a programmable percentage of it’s current value ("Auto-Exposure Configuration [register 48]", page 43), if it lies outside the threshold zone, and by 1/64 inside the zone, before crossing the target value.

Analog gain is used as part of the exposure control, but it is always equal to or less than the gain limit in AEC_CONFIG [register 48]. It can be disabled and removed from the algorithm.

The Automatic Exposure Control (AEC) can be disabled by resetting bit 00 and bit 1 of the AEC register. The user can then overwrite the exposure/gain values. If AEC is not disabled, it will overwrite the programmed exposure values at the next odd frame boundary.

Automatic (White) Color Balance

The objective of color balance is to make white objects in the scene appear white, regardless of any color cast in the ambient scene lighting.The Automatic Color Balance (ACB) algorithm is based on altering the RGB matrix in such a way as to balance the amount of energy being collected by the three over-threshold color accumulators RACC, GACC, and BACC. Access to the RGB matrix involves use of bit 1 of VP_CONTROL1 (RGB).

The performance of ACB is controlled by a number of parameters (see "Color Balance Registers [register 44 –46]", page 42). Like exposure control, the algorithm reads the color accumulators, but these are affected by the THRESH (register 41) value. Zone weighting does not apply to these accumulations.

ACB_GNBASE [register 45] defines the target level at which the algorithm tries to keep the minimum of the three channel gains. The position of this target has an effect on both the overall brightness of the image and how much gain headroom the color balance algorithm has to work with. The higher the target the brighter the image but with less headroom. The actual value of the gain base is ((1+gnbase)/8). ACB_MU (register 46) is a time constant that effects the speed of the color balance algorithm (ACB_MU = 0 is the fastest, ACB_MU = 7 the slowest).

The user may either disable the ACB algorithm and overwrite the RGB matrix, or just freeze the current set of values. The ACB algorithm can be disabled by resetting bit 0 of ACB configuration. To freeze the values, leave bit 0 set and set bit 1 to one. See the description of ACB_CONFIG (register 44), in "Color Balance Registers [register 44 –46]", page 42.

By-Pass Mode

In by-pass mode, the Bt832 can be configured (VP_DMCODE[7] - register 45) to supply the Bayer Pattern video data directly after defect correction, gain/offset, and unshuffle operations (see Figure 1-10). The data stream is available using the frame-grabber signals (FSTRT, LSTRT and VCLK).

1.4.6 Interrupts Generated

While routine Bt832-host communication is accomplished via the I^2C interface, an interrupt line requests attention for more important events. The signal stays active (high) until the host clears the appropriate bit of the VP_STATUS register, by writing a zero (writing one does not change the state of the bit).

Video Data Error This is an error condition in the video data stream. There are three different types of error. The details are described in Error Conditions and Procedures. The error type is stored in VP_STATUS register.

Camera Attached/Disconnected Change in camera-present status detected. The condition of the connection is reported in the CAM_STATUS register.

Serial Communication Error Bt832 serial interface master failed to get an acknowledge while attempting to write to the camera module.

1.5 Video Output Timing

There are two physical output interfaces to connect the processor to a video decoder. Video data is always 8-bit YUV/YCrCb-4:2:2 and the image is always non-interlaced. There are two synchronization options for marking HSYNC and VSYNC video events:

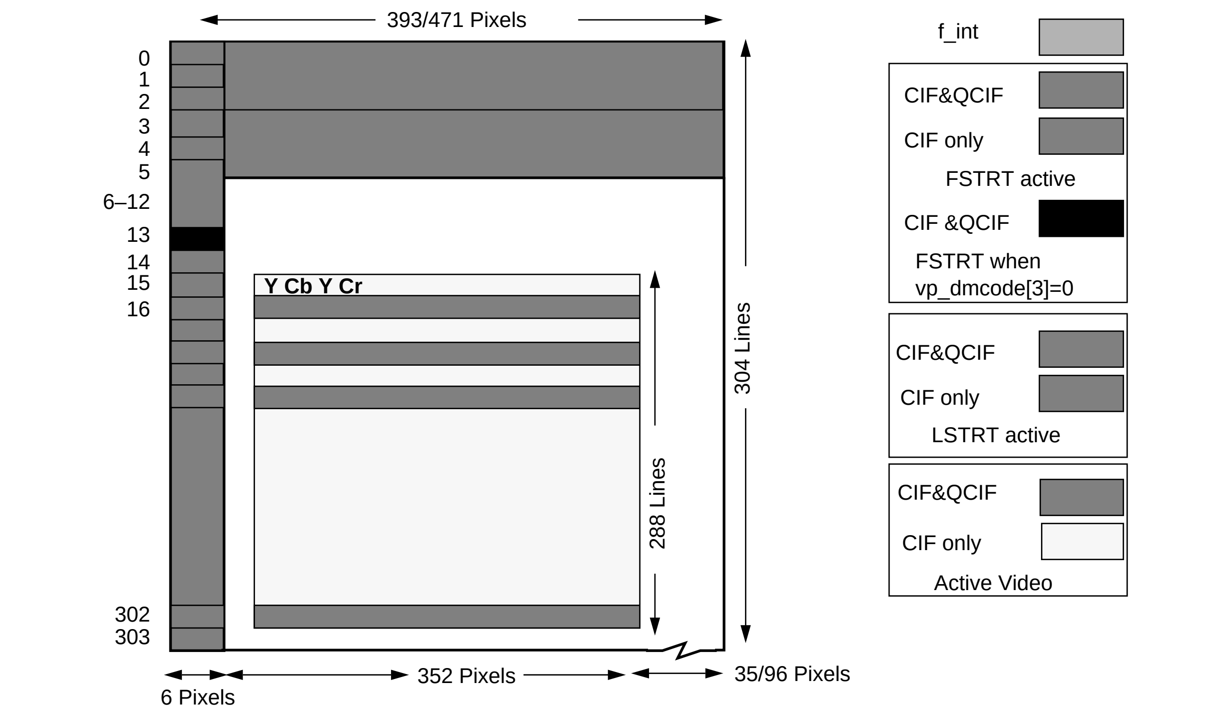
- Frame grabber signals (FSTRT, LSTRT and VCLK)
- Embedded sequences (CCIR-656 control codes) and qualifying clock

1.5.1 Frame Grabber Signals

These modes have a number of parameters programmable via the VP_DMCODE (register 43). Although these modes are not mutually exclusive (signals always pulse and embedded codes always appear on the data stream) it is best to use only one option, because there is no one-to-one correspondence between the features of the two options.

The structure of the frame grabber signals is presented in Figure 1-12. The term “pixel” refers to one period of the sensor clock divided by two. In Figure 1-12, the horizontal axis represents time for a given clock (VCLK) division. The Bt832 video output is pairs of 8-bit samples in YUV/YCrCb-4:2:2 format. Optionally, the bytes of a pair can be swapped (YUYV - as shown in Figures 1-12, 1-13, and 1-14, and Table 1-7). See the VP_DMCODE register, bit 0. VCLK falling edge should be used to sample each output byte.

Figure 1-12. Embedded Code Video Output Structure



Note: The line numbering is not the same as in previous figures. Line numbers shown here are the ones encoded in the SAV/EAV embedded sequences.

Figure 1-13. VCLK Relationship to System Clock

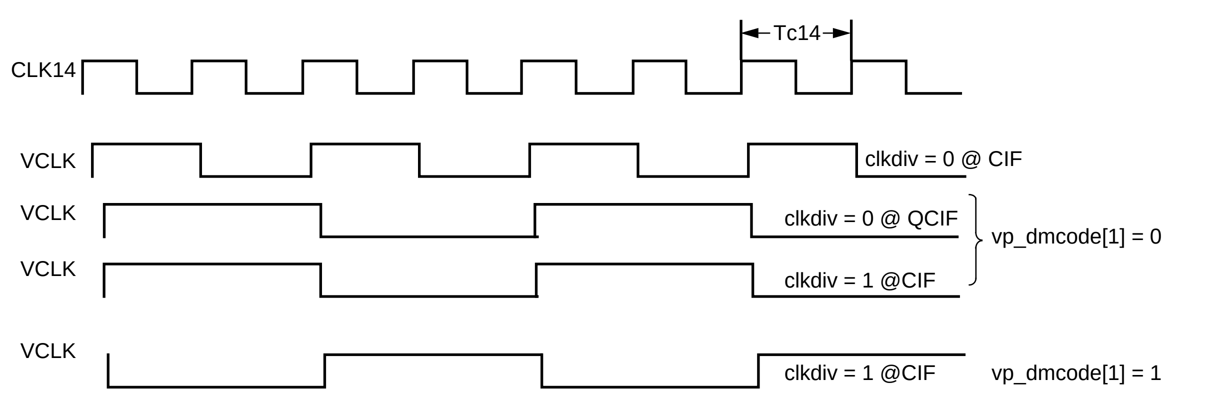
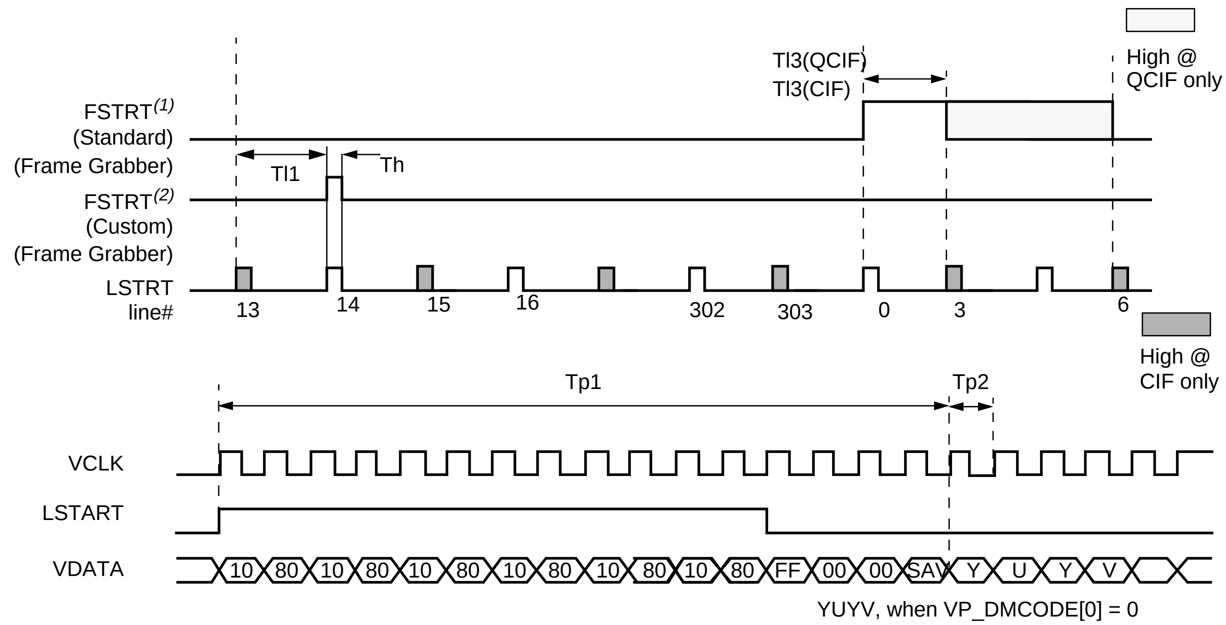
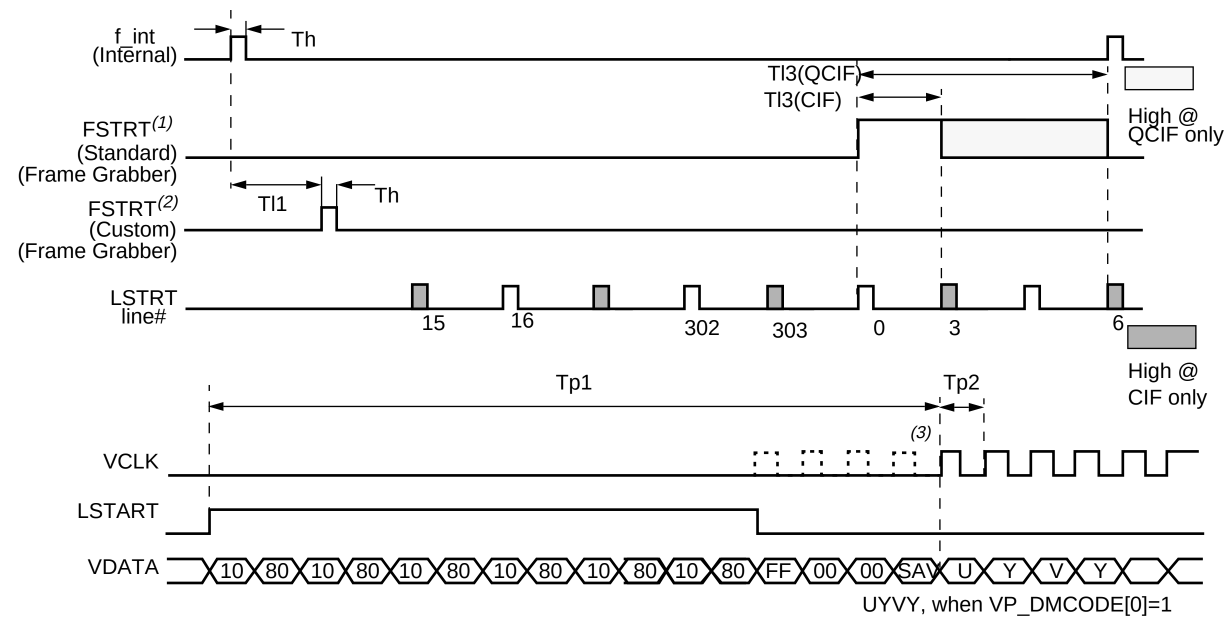


Figure 1-14. Frame Grabber Signals (LSTRT/VCLK Free Running)



Notes: (1). VP_DMCODE[2]=1.
(2). VP_DMCODE[2]=0.

Figure 1-15. Frame Grabber Signals (LSTRT/VCLK Only on Active Video)



Notes: (1). VP_DMCODE[2]=1.
(2). Custom frame grabber, VP_DMCODE[2]=0.
(3). Low when VP_DMCODE[2]=0.

Table 1-7. Video Timing Parameters

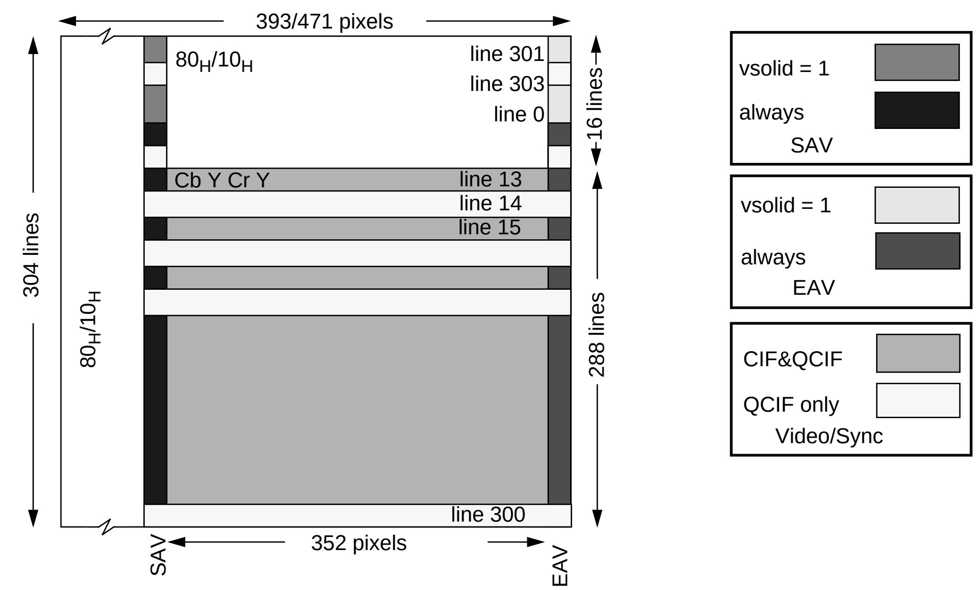
Symbol	Duration	Description
Th	12*Tp2	High period of the LSTRT.
Tl1	2*N*Tp2	One line period (N=393 @ 60 Hz, 471 @ 50 Hz).
Tl3	3*Tl1	High period of FSTRT (when VP_DMCODE[2]=1).
Tp1	16*Tp2	LSTRT to first active video sample.
Tp2	D*Tc14	Sample period, D=2 @ CIF & clkdiv = 0 (see Figure 1-13).
Tc14	69.84128 ns	Period of system clock (14.31818 MHz).

1.5.2 Embedded Code Sequences

Video events are also marked using CCIR656-like embedded codes (SAV/EAV) as shown in Figure 1-15.

Field ID in the embedded codes may be constant (zero-even) or toggling every field/frame (see VP_TEST_CONTROL0 register in the Programmers Model). In both cases, the video output is non-interlaced.

Figure 1-16. Embedded Code Video Output Structure



Note: The line numbering is not the same as in previous figures. Line numbers shown here are the ones encoded in the SAV/EAV embedded sequences.

1.6 Host Serial Control Bus

1.6.1 General Description

Writing configuration information to the video processor and reading processor status and configuration information is performed via the 2-wire host I^2C serial interface.

Communication using the serial bus centers around a number of registers internal to the video processor. These registers store status, set-up, exposure, and system information. Most of the registers are read/write allowing the host to change their contents. Others (such as the chip ID) are read only.

The main features of the serial interface include:

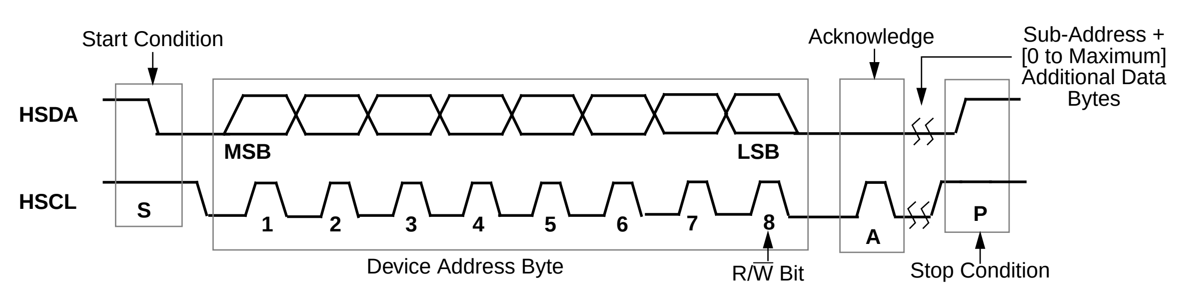
- Variable length read/write messages
- Indexed addressing of information source or destination within the sensor
- Automatic update of the index after a read or write message
- Message abort with not acknowledge (NACK) from the master
- Byte-oriented messages
- Pin programmable slave address

In order to use the serial interface, the system clock must be running.

1.6.2 Serial Communication Protocol

The host must perform the role of a communications master. The Bt832 acts as either a slave receiver or transmitter. The communications take the form of 8-bit data with a maximum serial clock frequency of 400 kHz. The serial clock (HSCL) is generated by the host, which determines the data transfer rate. The 7-bit default I^2C address for the Bt832 is 1000100b, or a transmitted byte of 0x88 for writes and 0x89 for reads. An alternate serial address can be chosen by adding a pull-up resistor to the FSTRT pin. The pin is read during reset before the output driver is enabled. By overriding the internal pull-down with an external pull-up resistor (25 k for 5 V pull-up, or 10 k for 3.3 V pull-up), one can select a serial address of 10001010b, or a transmitted byte of 0x8A for writes and 0x8B for reads. The serial protocol for the I^2C bus is shown in Figure 1-17.

Figure 1-17. Serial Interface Data Transfer Protocol



Note: For more information, request Rockwell's "I^2C Reference Guide".

1.6.3 Data Format

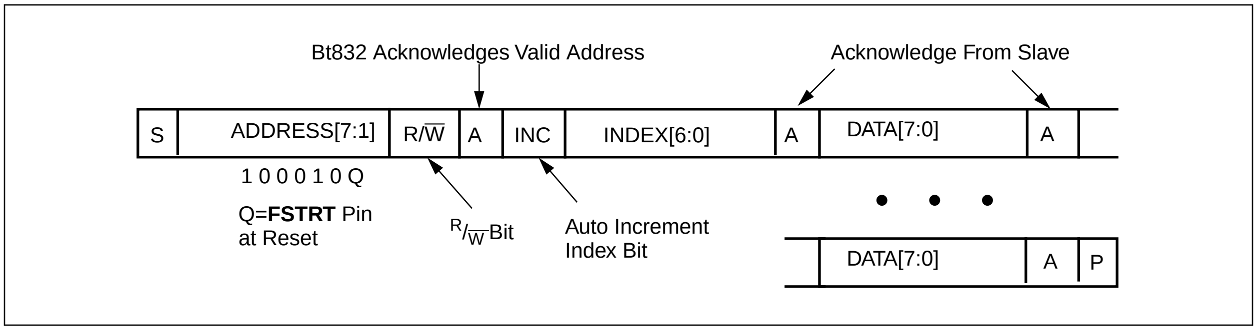
Information is packed in 8-bit packets (bytes) always followed by an acknowledge (ACK). The internal data is produced by sampling HSDA at a rising edge of HSCL. The external data must be stable during the high period of HSCL. The exceptions to this are start (S) or stop (P) conditions when HSDA falls or rises respectively, while HSCL is high.

A message contains at least two bytes preceded by a start condition, and followed by either a stop or repeated start (Sr), followed by another message.

The first byte contains the device address byte which includes the data direction (R$\overline{\text{W}}$) bit. The LSB of the address byte indicates the direction of the message. If the LSB is set high, then the master will read data from the slave. If the LSB is reset low, then the master will write data to the slave. After the R/$\overline{\text{W}}$ bit is sampled, the data direction cannot be changed, until the next address byte when a new R/$\overline{\text{W}}$ bit is received.

The byte following the address byte contains the address of the first data byte (also referred to as the INDEX). The serial interface can address up to 128 byte registers. If the MSB of the second byte is set, the automatic increment feature of the address index is selected.

Figure 1-18. Serial Interface Data Format



1.6.4 Message Interpretation

All serial interface communications with the Bt832 must begin with a start condition. If the start condition is followed by a valid address byte, then further communications can take place. The Bt832 acknowledges the receipt of a valid address by pulling it's HSDA line low. The state of the READ/$\overline{\text{WRITE}}$ bit (LSB of the address byte) is stored and the next byte of data, sampled by HSDA, can be interpreted.

During a write sequence, the second byte received is an address index and is used to point to one of the internal registers. The most-significant bit of the following byte is the index_auto_increment flag. If this flag is set then the serial interface will automatically increment the index address by one location after each slave acknowledge. The master can therefore send data bytes continuously to the slave until the slave fails to provide an acknowledge, or the master terminates the write communication with a stop condition or sends a repeated start (Sr). If the auto increment feature is used, the master does *not* have to send indices to accompany the data bytes.

As data is received by the slave it is written bit by bit to a serial/parallel register. After each data byte has been received by the slave, an acknowledge is generated. The data is then stored in the internal register addressed by the current index.

During a read message, the current index is read out in the byte following the device address byte. The next byte read from the slave device are the contents of the register addressed by the current index. The contents of this register are then parallel loaded into the serial/parallel register and clocked out of the device by HSCL.

At the end of each byte, in both read and write message sequences, an acknowledge is issued by the receiving device. Although the Bt832 is always a slave device, it acts as a transmitter when the bus master requests a read.

At the end of a sequence of incremental reads or writes, the final index value in the register will be one greater than the last location read from or written to. A subsequent read will use this index to begin retrieving data from that internal register.

A message can only be terminated by the bus master, either by issuing a stop condition, a repeated start condition, or by not acknowledging (NACK) after reading a complete byte during a read operation.

1.7 Camera Serial Control Bus

The Bt832 communicates to the QuartzSight camera and optional E^2PROM, which contains the sensor's defect map over a 2-wire I^2C serial interface. The Bt832 takes the role of bus master, overseeing serial communication. Only the QuartzSight camera, E^2PROM, and Bt832 can reside on the sensor I^2C bus (SSCL and SSDA). The data protocol is identical to the Host Serial Interface.

1.7.1 Usage of the Camera Registers with Auto Exposure Enabled

With Auto Exposure Control (AEC) enabled, there is a periodic camera serial interface message generated every two image frames. This message is seven bytes long (slave address, internal index, and five data bytes) and is initiated at the end of the appropriate frame. The message finishes before the frame interrupt signal is generated and the host may attempt to write any of the camera registers (except those in Bunch 0) a short time after INTR rises. "A short time" is defined as fast enough so that both the host and the camera serial interface messages complete before the last video line is output.

In this case both the camera register and AEC exposure register updates can take place in an interleaved manner.

If the host cannot guarantee absence of update activity towards the end of odd frames, the AEC should be turned off, the desired registers updated, and AEC turned on again. See "Note" on page 43.

2.0 Control Registers

2.1 The Programmers Model

There are 64 8-bit registers within the Bt832, accessible by the host via the serial interface. The primary categories are listed below:

- Status registers (read only)
- Setup registers with bit significant functions
- Exposure parameters that influence output image brightness
- System functions and analog test bit significant registers

Any internal register that can be written to can also be read from. There are a number of read only registers that contain device status information (for example, CAM_DEVICEH, register 54). There is also another type of register, where the bits can only be cleared as they are set by the hardware (VP_STATUS, register 52).

A detailed description of each register follows. The address indices are shown as binary numbers in brackets.

As a general rule, unused bits are located at the most-significant end of any byte.

2.2 Parameter Bunches and Parameter Cache

Some parameters (in particular the exposure and gain parameters) must be transferred in a block for continuous correct system operation. To avoid situations where a parameter transfer is overtaken by the onset of a new video frame, a mechanism exists whereby the host can write bunches to a 10-byte temporary store (the parameter cache). The host may indicate completion of parameter transfer by writing data of 255 and address of 63 to the Bt832, at which time the cache flushes, and the last *n* parameters written (where 0 <= *n* <= 10) are queued for distribution. If more than 10 values are written, the tenth value is overridden by the last value.

The Bunch column of Table 2-1 shows which parameters should be grouped.

***Table 2-1. Device Registers** (1 of 3)*

	Decimal Addr	Hex Addr	Bunch	Name	Bits	R/W	Default (in Hex)	Description
Input Processor	0	00		OFFSET	8	R/W	10	Video level offset
	1	01	0	RCOMP	8	R/W	C9	R input compensation gain
	2	02		G1COMP	8	R/W	C9	G (in R row) compensation gain
	3	03		G2COMP	8	R/W	C9	G (in B row) compensation gain
	4	04		BCOMP	8	R/W	C9	B input compensation gain
Exposure	5	05		FINEH	1	R/W	00	9-bit fine exposure; max value 360 (30Hz mode) or 438 (25Hz mode)
	6	06		FINEL	8	R/W	00	
	7	07		COARSEH	1	R/W	00	9-bit coarse exposure; max value 302
	8	08		COARSEL	8	R/W	00	
	9	09		CAM GAIN	3	R/W	00	External gain; effectively 1 + x where x is setting coded as a 3-bit unsigned integer

Table 2-1. Device Registers *(2 of 3)*

	Decimal Addr	Hex Addr	Bunch	Name	Bits	R/W	Default (in Hex)	Description
Main Processor	10	0A	1	M00/CSC00	8	R/W	C0/02	mxy:-row x col y matrix component
	11	0B		M01/CSC01	8	R/W	00/41	See VP_CONTROL1, bit [1] for RGB/YUV/YCrCb matrix selection. Default value R/C:- RGB component initialized to R YUV/YCrCb initialized to C DUAL–Purpose register set
	12	0C		M02/CSC02	8	R/W	00/D9	
	13	0D		M10/CSC10	8	R/W	00/ED	
	14	0E		M11CSC11	8	R/W	C0/DB	
	15	0F		M12/CSC12	8	R/W	00/38	
	16	10		M20/CSC20	8	R/W	00/38	
	17	11		M21/CSC21	8	R/W	00/D1	
	18	12		M22/CSC22	8	R/W	C0/F7	
	19	13		APCOR	8	R/W	14	Aperture Correction parameters
	20	14		GAMCOR	4	R/W	08	Gamma Correction parameters
Accumulator Inputs	21	15		VP_CONTROL2	8	R/W	14	Line accumulation spacing and scaling
	22	16	2	ZONECODE0	8	R/W	00	Zone weights
	23	17		ZONECODE1	8	R/W	28	
	24	18		ZONECODE2	8	R/W	28	
	25	19		ZONECODE3	8	R/W	00	
Accumulator Outputs	26	1A		RACC	8	RO		R channel accumulation
	27	1B		GACC	8	RO		G channel accumulation
	28	1C		BACC	8	RO		B channel accumulation
	29	1D		BLACK_ACC/ ACB00	8	RO		Black level accumulation
	30	1E		EXP_ACC	8	RO		mono (pre-matrix) accumulation
	31	1F		LACC0/ACB01	8	RO		Line accumulations 0 - 7 or Auto. Color Balance calculated RGB matrix
	32	20		LACC1/ACB02	8	RO		
	33	21		LACC2/ACB10	8	RO		
	34	22		LACC3/ACB11	8	RO		
	35	23		LACC4/ACB12	8	RO		
	36	24		LACC5/ACB20	8	RO		
	37	25		LACC6/ACB21	8	RO		
	38	26		LACC7/ACB22	8	RO		

Table 2-1. Device Registers *(3 of 3)*

	Decimal Addr	Hex Addr	Bunch	Name	Bits	R/W	Default (in Hex)	Description
System	39	27		VP CONTROL0	8	R/W	01	Processor mode settings
	40	28		VP_CONTROL1	8	R/W	27	
	41	29		THRESH	8	R/W	E0	RGB accumulation threshold
	42	2A		VP_TESTCONTROL0	8	R/W	0	Test modes
	43	2B		VP_DMCODE	8	R/W	1C	Video output configuration
	44	2C		ACB_CONFIG	8	R/W	01	Auto. color balance configuration and parameters
	45	2D		ACB_GNBASE	8	R/W	08	
	46	2E		ACB_MU	8	R/W	04	
	47	2F		CAM TEST0	8	R/W	00	Camera system test
	48	30		AEC_CONFIG	8	R/W	17	AEC configuration bits
	49	31		AEC_TL	8	R/W	50	Lower average threshold
	50	32		AEC_TC	8	R/W	64	Target average value
	51	33		AEC_TH	8	R/W	78	Upper average threshold
Status	52	34		VP_STATUS	8	R/W	02	Processor status
	53	35		VP_LINECOUNT	8	RO		Top 8 bits of 9-bit current processor line count (lowest bit is in vp_status)
	54	36		CAM_DEVICEL	8	RO		Camera identification number including revision counter
	55	37		CAM_DEVICEH	8	RO		
	56	38		CAM_STATUS	8	RO		Camera status
Camera Setups	57	39		CAM_SETUP0	8	R/W	09	Low-power & mains freq. setup
	58	3A		CAM_SETUP1	8	R/W	C1	Diagnostics setup
	59	3B		Reserved	8	R/W	08	Do not write this register
	60	3C		Reserved	8	R/W	00	Do not write this register
System	61	3D		DEFCOR	8	R/W	08	Defect correction
	62	3E		Reserved	1	R/W	00	Do not write this register
	63	3F		DEVICE ID	8	R/W	31	See also parameter bunches

2.3 Key Registers in Detail

Some of the 64 registers require further detailed explanation, which follows.

Offset [register 0]

Digital control of input offset. The QuartzSight camera outputs digital video with a nominal black level of 16. The value of OFFSET, coded as an 8-bit two's complement integer between –128 and +127, is subtracted from the input value by the camera. Nominally 16, *offset* may be adjusted by the host for flare correction or for digital black-level compensation (see register 29).

Bayer Gains [registers 1–4]

Digital control of input Bayer channel gains. Can be altered relative to each other to equalize channel responses (color-dependent gain) or in ensemble fashion (color-independent gain). See "1.4.1 Bayer Pattern Overview" on page 16 for more information.

NOTE: At least one gain value should be written to the exposure bunch (registers 5–9) because camera exposure and gain values are not stored in the parameter cache.

Camera Exposure & Gain [registers 5–9]

Along with the Bayer gains (registers 1 through 4), this set of programmable registers controls the effective sensitivity of the sensor. These registers comprise Bunch 0 along with the Bayer Gain registers (1–4). The exposure registers are as follows:

1. Fine exposure time
2. Coarse exposure time
3. Camera gain

The final parameter does not affect the integration period. It amplifies the video signal at the output stage of the sensor core.

NOTE: At the camera, the exposure (coarse, fine, and gain) values do not take effect immediately. They are written via the camera serial interface, but they will be applied later. The exposure is updated on the next even frame and the gain is applied one frame after the exposure. If the user reads an exposure value via the host serial interface the value reported will be the previous exposure data read from the sensor, at the beginning of each frame.

Between writing the exposure data and the point at which the data is consumed by the exposure logic, bit 0 of the CAM_STATUS register is set. The gain value is updated a frame later than the coarse and fine parameters. The reason for this is because the gain is applied directly at the video output stage and does not require the long set up time of the coarse and fine exposure (see "Note" on page 43).

To eliminate the possibility of the sensor array seeing only part of the new exposure and gain setting, these values are stored temporarily in the camera serial cache and transferred to their final destination at frame boundaries, as described above.

The range of some parameter values is limited and any value programmed outside this range will be clipped to the maximum allowed values.

MATRIX/CSC [registers 10–18]

Two different sets of registers can be accessed depending on the state of bit{1} of VP_CONTROL1. The values in registers 10–18 are all 8-bit, 2's complement format. [M00–M22] are used to convert RGB data after the smooth interpolation stage into an RGB output which is now adjusted to imperfections in the camera response to different lighting conditions.

APCOR [register 19]

APCOR is an acronym for aperture correction, the Bt832's means of enhancing edge detail in images. This is achieved by deriving an unsharp mask, which is the difference between two interpolated green signals, one of which contains more high-frequency detail than the other. First, the unsharp mask is cored, (values below a programmable threshold are set to zero and values above the threshold have the threshold subtracted in an absolute sense). Next, it is amplified by a programmable intensity factor. Coring is a simple means of noise reduction.

Table 2-2. Apcor [register 19]

Bits	Function	Default	Description
3:0	Apcor Intensity	0100	4-bit gain factor applied to cored unsharp mask signal, spans the range 0 to 15 in steps of 1.
7:4	Apcor Threshold	0001	4-bit coring threshold, spans the range 0 to 3.75 in steps of 0.25 relative to RGB signal values.

GAMCOR [register 20]

GAMCOR is an acronym for gamma correction, the inverse-exponential distortion of signal amplitudes. Some video standards require a gamma of 2.2, corresponding to $f(x) = x^{0.45}$. A recent subtle modification (SMPTE-240M) specifies $f(x) = 4x$ ($x <= .0228$), else $f(x) = 1.1115\ x^{0.45} - 0.1115$, and Bt832 provides this curve as a basic function. Gamma correction has further use for cosmetic image enhancement. For this purpose, we provide 16 curves of increasing gamma , ranging from 0 (linear) through 8 (SMPTE-240M) to 15. Only Gamcor values of 0 and 8 produce legal gamma curves; others are derived by interpolation and correspond to a broad linear span of effective gamma curves.

Table 2-3. Gamcor [register 20]

Bits	Function	Default	Description
3:0	Gamcor	1000	4-bit gamma code. Gamma = 2.2 for Gamcor = 1000.
7:4	Unused		

ZONECODE 0,1,2,3 [register 22–25]

For exposure monitoring purposes, the sensor area can be divided into 16 zones. These zones are arranged in a 4 x 4 pattern, as shown in Table 2-4, referenced to the displayed image. Each zone carries a 2-bit weight, interpreted as follows: 00 = 0, 01 = 1, 10 = 2, 11 = 4. This facilitates center-weighted exposure control.

Table 2-4. Zonecode 0,1,2,3 [register 22-25]

zonecode0[1:0]	zonecode0[3:2]	zonecode0[5:4]	zonecode0[7:6]
zonecode1[1:0]	zonecode1[3:2]	zonecode1[5:4]	zonecode1[7:6]
zonecode2[1:0]	zonecode2[3:2]	zonecode2[5:4]	zonecode2[7:6]
zonecode3[1:0]	zonecode3[3:2]	zonecode3[5:4]	zonecode3[7:6]

RGB Accumulation [registers 26–28] and Threshold [register 41]

To assist in the external control of color balance, the Bt832 accumulates energy in the 3 main color channels. The parameter THRESH (register 41) acts as a threshold for accumulation, and signal values below this threshold are not accumulated. Note that these accumulations are not zoned.

Black Level Accumulation [register 29]

To control black level without interfering with sensor operation, the Bt832 outputs the average input black level over two lines transmitted prior to the main image frame. Two extra bits below the binary point is transmitted, so that if the nominal value of 16 is measured, the BLACK_ACC (register 29) parameter returned will be 64. The host may adjust OFFSET (register 0) to compensate for imperfect black calibration. See also "Color Balance Effective RGB Matrix [registers 29 & 31-38]", page 39.

Mono Accumulation [register 30]

To assist in the external control of exposure and front-end gain, the Bt832 accumulates energy in the raw (pre-matrix, post-interpolation) color channel, weighted according to ZONECODE settings. Accumulation is to 22-bit precision. The input is up-shifted by ACCSCALE bits (register 21), then downshifted 4 bits. The EXP_ACC (register 30) provides the 8 most-significant bits of a 22-bit accumulator. For example, with zone weights of 1 throughout, and ACCSCALE=1, full-scale input (i.e. all pixels at the maximum value - 0xFF) gives an internal accumulation of 255 * (((352 * 288) * 1 * 2) / 16) = 3231360, resulting in EXP_ACC = 197, as the eight most-significant bits.

Line Accumulations 0–7 [registers 31-38]

To facilitate the computation of optimal exposure values in flicker-reduction mode, the Bt832 returns eight accumulations of line energies, spaced LINESPACE (bits [3:0] of VP_CONTROL2) lines apart. This forms a series of eight scaled samples of flicker pattern in the image, and host must analyze current and past series to minimize flicker pattern crawl.

Color Balance Effective RGB Matrix [registers 29 & 31-38]

The ACB algorithm calculates a set of values that is applied internally on the video processing engine. The user may wish to read these values which are in locations shared with BLACK_ACC, LACC0–7, and AEC_CONFIG[3] to select which of the two sets are read in these locations. In order to override the internal RGB matrix, the ACB has to be turned off, using ACB_CONFIG[0].

VP_CONTROL0 [register 39], VP_CONTROL1 [register 40], and VP_CONTROL2 [register 21]

The processor has several different operating modes. These operating modes are independent.

Table 2-5. VP_CONTROL0 [register 39]

Bits	Function	Default	Description
1:0	clkdiv[1:0]	01	Frame Rate Division, used for selecting frame rates lower than 30/25 Hz. 00: divide frame rate by 1 01: divide frame rate by 2 10: divide frame rate by 4 11: divide frame rate by 8
3:2	Phase[1:0]	00	Phase of processor clock with regards to incoming data.
4	Phase_Override	0	Phase of processor clock externally set to value in Phase[1:0] register.
5	hjog	0	Bayer pattern horizontal jog.
6	vjog	0	Bayer pattern vertical jog.
7	evenfirst	0	Bayer pattern group interpretation.

Table 2-6. VP_CONTROL1 [register 40]

Bits	Function	Default	Description
0	Unused	1	
1	RGBmatrix	1	1: Processor interprets matrix data as matrix/gain 0: Processor interprets matrix as color space conversion
2	QCIF	1	1: QCIF mode 0: CIF mode
3	zoom mode	0	When in QCIF mode, the QCIF image comes from cropping the image to display just the center of the frame, rather than scaling the entire image down. Warning: This mode produces non-standard timing on the video output bus.
4	YUVNOT	0	YUV/YCrCb conversion from 24-bit RGB data is disabled.
6:5	Camera clock pin drive strength	01	00: three-state both drivers 01: enable 120 Ω driver 10: enable 240 Ω driver 11: enable both drivers, ~ 80 Ω drive
7	Three-state video output	0	VDATA[7:0], FSTRT, LSTRT, VCLK are three-stated if this bit = 1.

Table 2-7. VP_CONTROL2 [register 21]

Bits	Function	Default	Description
3:0	Linespace	1000	Spacing of the eight lines used in line accumulation for flicker-reduction.
6:4	Accscale	001	3-bit code controlling accumulator scaling.
7	f_int mask	0	When set, disables (or masks) the internal frame interrupt (f_int) from causing an interrupt on the INTR pin.

VP_TEST_CONTROL0 [register 42]

The processor has several different test modes.

Self-timing is required if the camera is not attached or put into low-power modes. Selftiming is also required four frames after exiting low-power mode or reset.

Speed-up serial master will increase the serial interface speed above 100kHz, but the camera head is not guaranteed to respond, unless connected via an ideal wire (no noise or skew).

If bit 6 is set to one, the SSDA and SSCL signals can be driven zero or left free to be pulled up by the pad resistors. Reading from these bits reports the actual state of the wires, which are possibly driven by the camera head.

Table 2-8. VP_TEST_CONTROL0 [register 42]

Bits	Function	Default	Description
0	color_bars	0	Generates NTSC System 'M' bars.
1	self_timing	0	Generates frame timing internally.
2	Mask receiver errors	0	For test purposes.
3	Speed-up serial master	0	For test purposes.
5:4	SSCL, SSDA	00	Bit5=SSDA, bit6=SSCL.
6	Access SSDA,SSCL signals	0	If this flag is set (= 1), software control of sensor I^2C can occur through [6:5].
7	Unused	0	

VP_DMCODE [register 43]

Video output has various programmable features to allow compatibility with a number of video capture devices.

If bit 4 is zero, the qualified output samples are dependent on bit 2 and bit 3 (STANDARD and VSOLID).

Table 2-9. VP_DMCODE [register 43]

Bits	Function	Default	Description
0	UYVY	0	Default is YUYV.
1	CCIR-656 clock edge	0	Data change at positive edge of VCLK, if zero.
2	Standard mode	1	Custom frame grabber spec, if zero.
3	Vsolid	1	Only one blank line (with SAV/EAV), if zero.
4	Free-running VCLK	1	Only active video + codes qualified, if zero.
5	Pairs always	0	Skip every other output sample if set.
6	Toggling field ID	0	If zero, the field ID is always 0 (i.e., even).
7	Enable by-pass	0	Raw Bayer data output, if set.

Color Balance Registers [register 44 –46]

The automatic color balance is configured by these registers. ACB_CONFIG is a bit-significant register and the function of each bit is described in Table 2-10.

The other two registers (ACB_GNBASE & ACB_MU) define the basic gain and the rate of update of the internal balance values. The calculated RGB matrix may be read by host registers 29 and 31-38, when bit 3 of this register is set (=1).

Table 2-10. Automatic Color Balance Configuration [register 44]

Bits	Function	Default	Description
0	ACB	1	Zero disables ACB.
1	Freeze values	0	Suspends CB algorithm.
2	Pregain	0	If set, gray-preserving RGB matrix enabled.
3	Access calculated RGB matrix values	0	Registers 29 and 31–38 are read-only if set.
7:4	Unused	0000	

Camera System Test [register 47]

The sensor has several different test modes. These test modes detect faults in the sensor pixel array and the supporting analog circuitry. Only one test mode can be enabled at a time.

NOTE: These features are exclusively for use during design development and are not intended to be used either by production test or an end user.

Table 2-11. Camera System Test [register 47]

Bits	Function	Default	Description
0	Bitline test	0	0 will be read from this register.
1	Black image test	0	0 will be read from this register.
2	White image test	0	0 will be read from this register.
3	Linear Test	0	0 will be read from this register.
4	Short frame enable	0	Short video frames (only one blank line).
5	57 lines per frame	0	Default is 13 lines per frame.
7:6	Unused	00	

Auto-Exposure Configuration [register 48]

This register is bit-significant and the bit functions are described in Table 2-12.

Table 2-12. Auto-Exposure Configuration [register 48]

Bits	Function	Default	Description
0	Enable auto-exposure control	1	Turns on AEC if set to one.
1	Enable use of gain	1	Allows AEC hardware to modify gain in addition to exposure time.
3:2	Step size	01	00 : 1/8 01 : 1/16 10 : 1/32 11 : 1/64
5:4	Gain upper limit	01	Limits the maximum gain value that the hardware can write.
7:6	Unused	00	

NOTE: Bit 1 of the Auto-Exposure Configuration register does not properly control the update of the gain register. In order to modify the CAM_GAIN register through the I^2C port, the AEC enable bit (bit 0) must be enabled while the AGC enable bit (bit 1) is left off. In cases where software is implementing the full auto-exposure control algorithm, it will have to be careful that it does not allows the hardware to modify the exposure registers by setting the AEC bit in order to modify the CAM_GAIN register.

Auto-Exposure Thresholds [registers 49–51]

These thresholds define the region in which the automatic exposure algorithm will try to drive the picture average value (calculated in EXP_ACC, register 30). They must be ordered as AEC_TL < AEC_TC < AEC_TH and maintaining adequate distance between them will prevent instability on some types of scenes (example: flat gray).

VP_STATUS [register 52]

An error condition generates an interrupt to the host and sets the appropriate bit in this register. The host can clear the bit by writing to this register location a binary value with zero at the corresponding position.

The phase_error flag indicates communication problems encountered on start-up. This situation may arise under unusual circumstances, such as the use of a faulty camera cable.

The data_corrupt and byte_error flags indicate loss of synchronization with the camera, possibly because of noise on the camera cable.

The serial_error flag (bit 3) indicates communication problems encountered between the camera and Bt832 at run-time. This situation may arise after a device reset, when a camera is not connected, when there is no defect list EEPROM or finally, from a faulty camera cable.

The odd_line flag is required by the host to interpret processor output. This bit is set for odd-indexed lines which contain both luminance and chrominance, while it is reset for even-indexed lines which contain luminance data only. Odd_line will not generate an interrupt. See "Line Output Format", page 21.

The effective phase may be different from the one programmed in VP_CONTROL1, if the Phase_Override (bit 4 of VP_CONTROL0 register) bit is zero.

Table 2-13. VP_STATUS [register 52]

Bits	Function	Default	Description
0	phase_error (generates interrupt/INTR = 1)	0	Sampling phase selection failed.
1	nibble_error (generates interrupt/INTR = 1)	0	Line sync error between the camera and Bt832 detected.
2	byte_error (generates interrupt/INTR = 1)	0	Illegal value from the sensor received by Bt832.
3	serial_error	0	Serial communications error between the camera and Bt832 detected.
4	camera_x	0	Camera head connection changed.
5	odd_line	0	Current output line is odd-indexed.
7:6	effective phase [1:0]	00	The value used by the receiver. See “Receiver Operational Mode” section for more detail.

Camera DeviceH [register 54] and DeviceL [register 55]

These registers provide read only information that identifies the sensor type that has been coded as a 12-bit number and a 4-bit mask set revision identifier. The initial mask revision identifier is 0 i.e. 0000_2. The device identification number for QuartzSight camera is 0x194.

Table 2-14. Camera DeviceH [register 54]

Bits	Function	Default	Description
7:0	Device type identifier	0001 1001_2	Most-significant 8 bits of 12 bit code identifying the chip type.

Table 2-15. Camera DeviceL [register 55]

Bits	Function	Default	Description
3:0	Mask set revision identifier	0000_2	Specifies mask revision number.
7:4	Device type identifier	0100_2	Least significant 4 bits of 12 bit code identifying the chip type.

Camera Status [register 56]

See Table 2-16 for camera status.

Table 2-16. Camera Status [register 56]

Bits	Function	Default	Description
0	Exposure value update pending	0	Exposure value sent but not yet consumed by the exposure controller.
1	Gain value update pending	0	Gain value sent but not yet consumed by the exposure controller.
2	Clock divisor update pending	0	Not used by Bt832.
3	BCAL in progress	0	Black calibration of custom DACs in progress.
4	Odd frame	0	This flag will toggle state on alternate frames. 1 denotes odd frame.
5	camera_present	1	A camera is present by the Bt832 if 1.
6	VP_busy	1	Bt832 is busy writing to the camera.
7	Unused	0	

Camera Setup0 and 1 [registers 57–58]

See Table 2-17 and 2-18 for pertinent camera setup information.

Table 2-17. Camera Setup0 [register 57]

Bits	Function	Default	Description
0	Low-Power Mode: Off/**On**	1	Powers down the sensor array. The output databus goes to FF_H .(1)
1	Sleep Mode: **Off**/On	0	Puts the sensor array into reset. The output databus goes to FF_H .
2	Soft Reset: **Off**/On	0	Setting this bit resets the sensor to its power-up defaults. This bit is also reset.
3	Frame Rate select: 25 fps or **30 fps**	1	Setting this bit chooses 30 frames/second.
4	Three-state camera output	0	Default value (= 0) means camera output (SDATA[3:0]) is not three-stated.
7:5	Unused		
Notes: (1). After a reset, the camera is in low-power mode.			

Table 2-18. Camera Setup1 [register 58]

Bits	Function	Default	Description
0	Automatic black calibration: Off/**On**	1	Enables or disables automatic black level calibration. Current black DAC values are frozen when disabled.
1	Force black calibration: **Off**/On	0	When set (= 1), the sensor is forced to repeatedly re-calibrate the black level.
3:2	Reserved		
4	Enable immediate gain update: **Off**/On	0	Allow manual change of gain to be applied immediately.
5	Reserved		
6	Border rows and columns: Masked or **Output**	1	When set (=1), pixels in the border rows and columns are output by camera over SDATA[3:0].
7	Pixel readout order: Unshuffled or **Shuffled**	1	Must be set to 1 for normal operation.

DEFCOR [register 61]

DEFCOR is an acronym for defect correction, the Bt832's method of eliminating pixel defects if present. The mechanism used is a 4-tap predictive filter on the Bt832 input which computes the function $[(1+m)N_1 - mN_2]$, where N_1 is the sum of the immediate left and right neighbors of a tagged defect pixel, N_2 is the sum of the next-nearest left and right neighbors, and m is a 5-bit coefficient defcor_coef [bit 4:0] spanning the range 0 to 0.96875 in steps of 0.03125. When m = 0, prediction is a simple linear interpolation. Values of m > 0 provide bi-directional, low-pass filtering to exploit the properties of inherently band-limited signals.

Table 2-19. DEFCOR [register 61]

Bits	Function	Default	Description
4:0	defcor_coef	01000	Coefficient m. Default value is 0.25.
7:5	Unused		

3.0 PC Board Layout Considerations

3.1 Layout Considerations

The PC board layout should be optimized for lowest noise on the Bt832 power and ground lines. Route digital traces away from analog traces. All shields must be connected to the ground plane with low impedance connection. Use shielded connectors.

3.1.1 Capacitors

From the following pins to ground, place bypass capacitors as close to the Bt832 as possible (using 0.1µF ceramic capacitors):

VDD	pin 9
VDD	pin 17
VDD	pin 30
VDD5	pin 25

Whenever possible, place traces from all power pins to a bypass capacitor on the component side, in addition to any feedthrough. Finally, place traces from all ground pins to a bypass capacitor on the component side, in addition to any feedthrough, when possible.

3.1.2 Ground Plane

Ensure that there is ample ground plane under the Bt832. Make wide paths of copper under and around the Bt832 if possible. Avoid creating a cut in the plane with feed-throughs: instead, disperse them. Also ensure that there is ample power plane under the Bt832. Make wide paths of copper under and around the Bt832 if possible. Avoid creating a cut in the plane with feed-throughs: instead, disperse them.

To fill:

- Copper fill ground on the component side of two-layer boards.
- Power fill on the circuit side of two-layer boards.
- Ground fill on both sides of 4-or-more-layer boards.

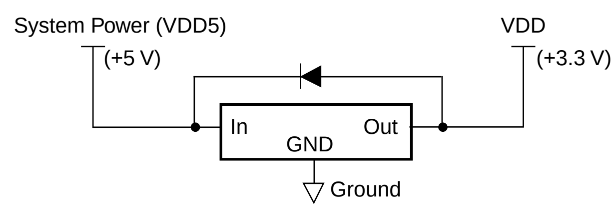
3.2 Latchup Avoidance

Latchup is possible with all CMOS devices. It is triggered when any signal pin exceeds the voltage on the power pins associated with that pin by more than 0.5 V, or falling below the ground pins associated with that pin by more than 0.5 V. Latchup can occur if the voltage on any power pin exceeds the voltage on any other power pin by more than 0.5 V.

To avoid latchup of the Bt832, follow these precautions:

- Apply power to the device before or at the same time as you apply power to the interface circuit.
- Connect all VDD pins together through a low impedance plane.
- Connect all VSS pins together through a low impedance plane.
- If a voltage regulator is used on the digital power plane, a protection diode must be used. Refer to Figure 3-1.

Figure 3-1. Optional Regulator Circuitry



Suggested part numbers:
Regulator Micrel MIC5201-3.3BM

3.3 Camera Interface

To provide the best emissions and susceptibility profile, the following camera connection guidelines are provided:

- Attach the connector shield to chassis ground.
- Make the connections from the Bt832 as short as possible.
- Keep the traces on the circuit side until the trace connects to the first component.
- Provide ample grounding as described in Section 3.1.

3.4 Bt832 Crystal Circuit

Crystals are specified as follows:

- 20 pF load capacitance
- Frequency temp char 30 ppm @ 25° C
- Shunt capacitance max 7 pF
- Series resistance 60 Ω max
- Fundamental cut
- 14.31818 MHz
- 20 ppm
- Parallel resonant

Figure 3-2 shows the clock options. Recommended crystals for use with the Bt832 are listed in Table 3-1.

Figure 3-2. Bt832 Clock Options

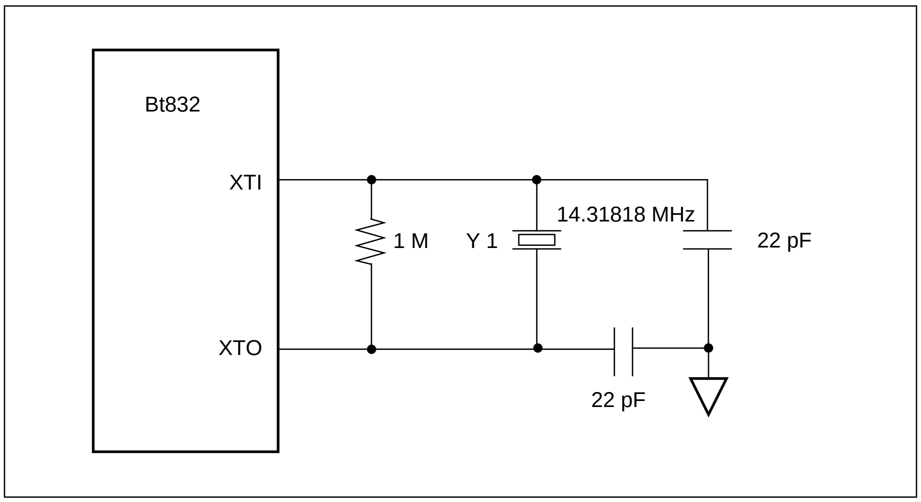


Table 3-1. Recommended Crystals

Manufacturer	Part Number
Horray Electronics Inc.	H1431–20
Raltron	AS–14.31818–20

3.4.1 Sample Schematics

Figures 3-3a through 3-3d are example schematics which detail the interface of the Bt832 to the Bt878.

Figure 3-3a. Sample Schematic (Bt878)

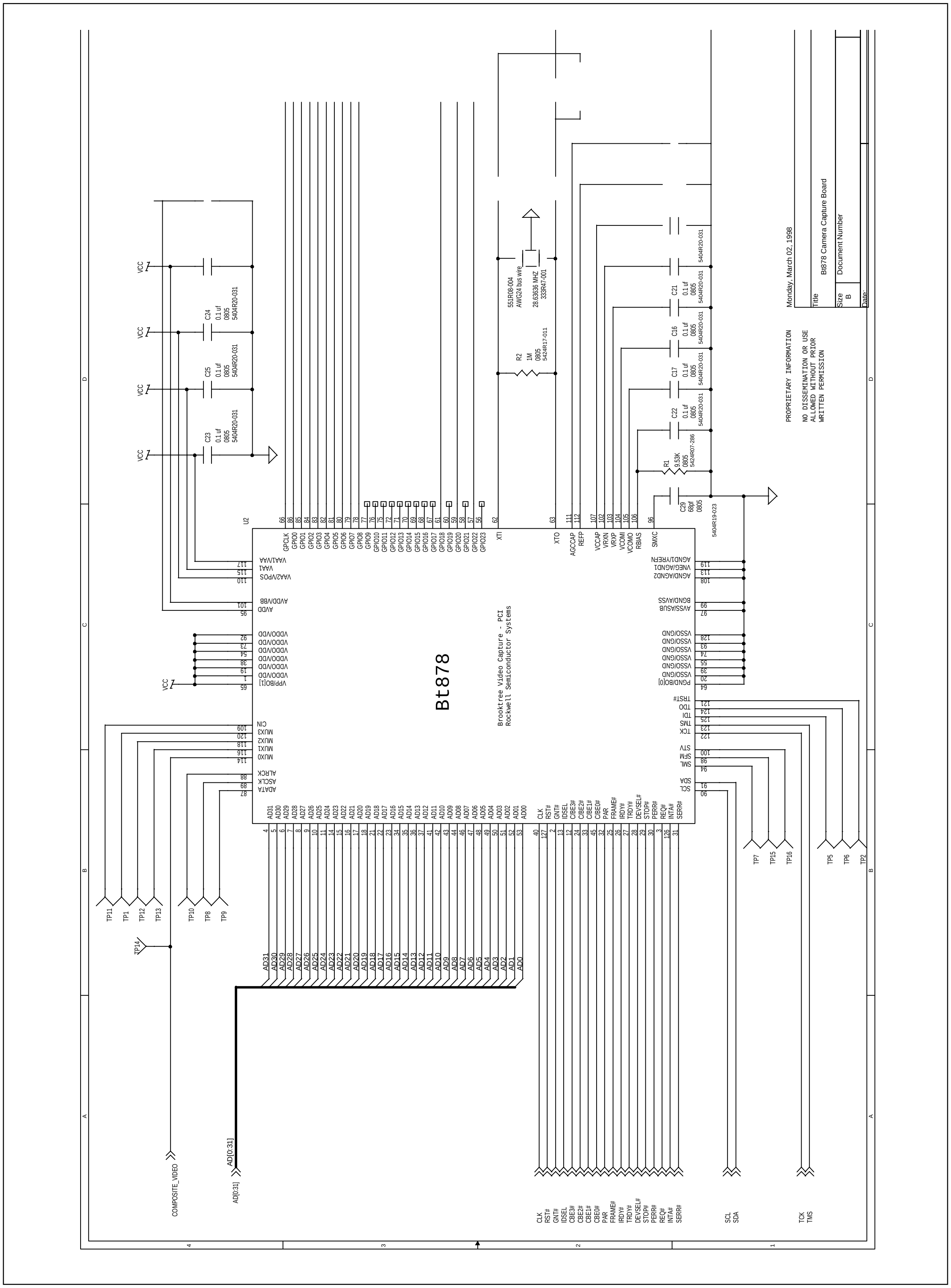


Figure 3-3b. Sample Schematic (Bt832)

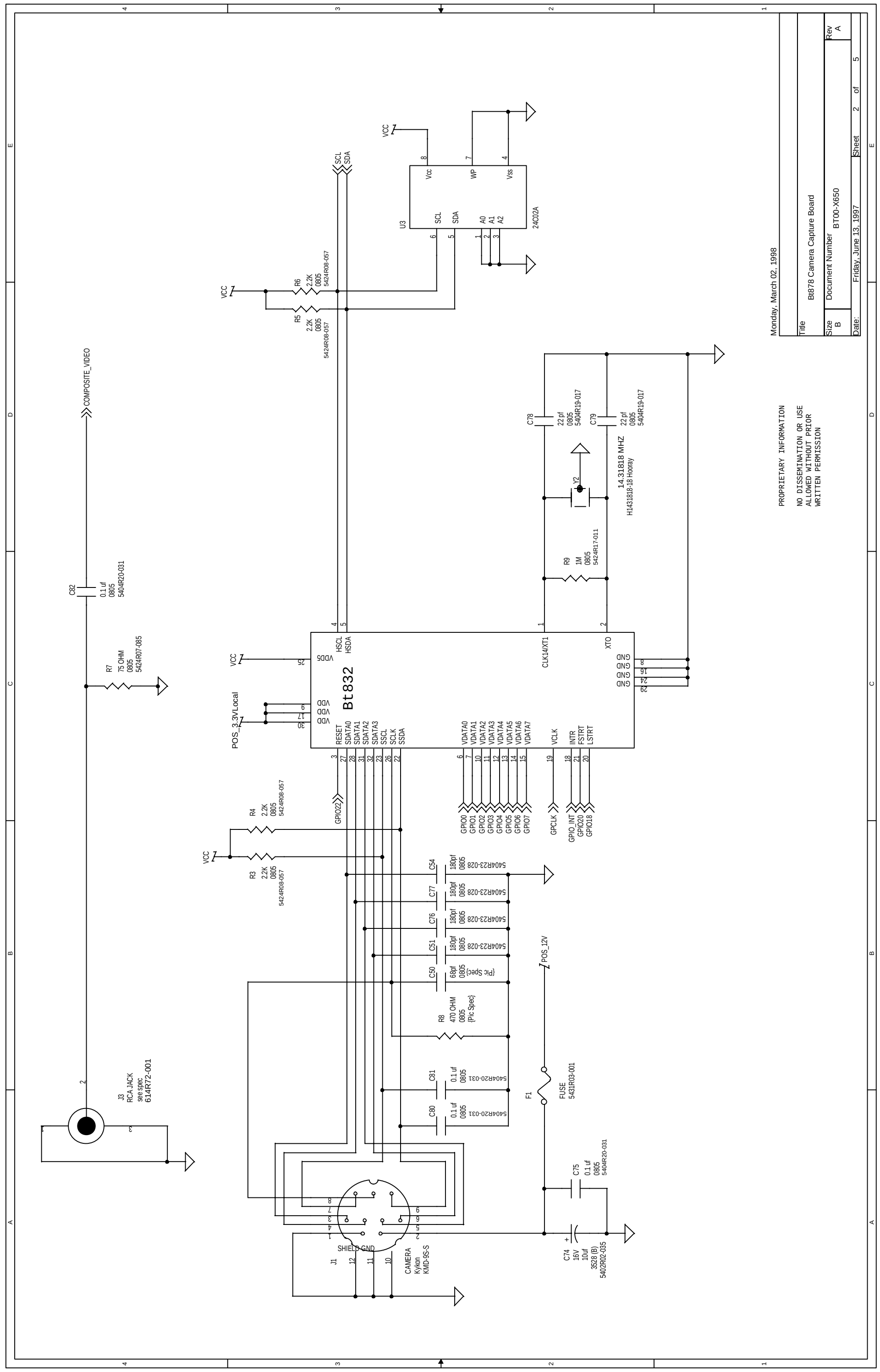


Figure 3-3c. Sample Schematic (PCI Connector)

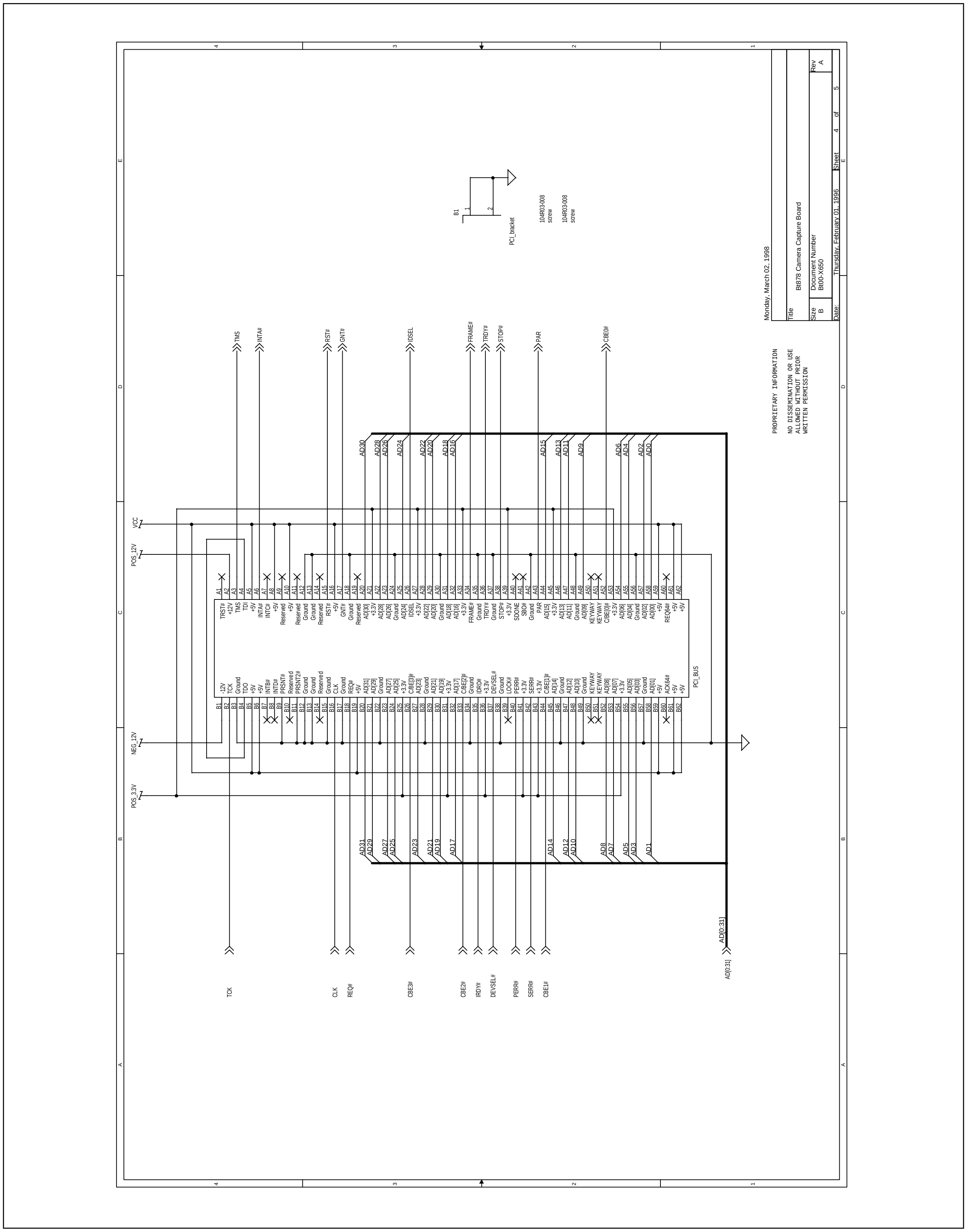
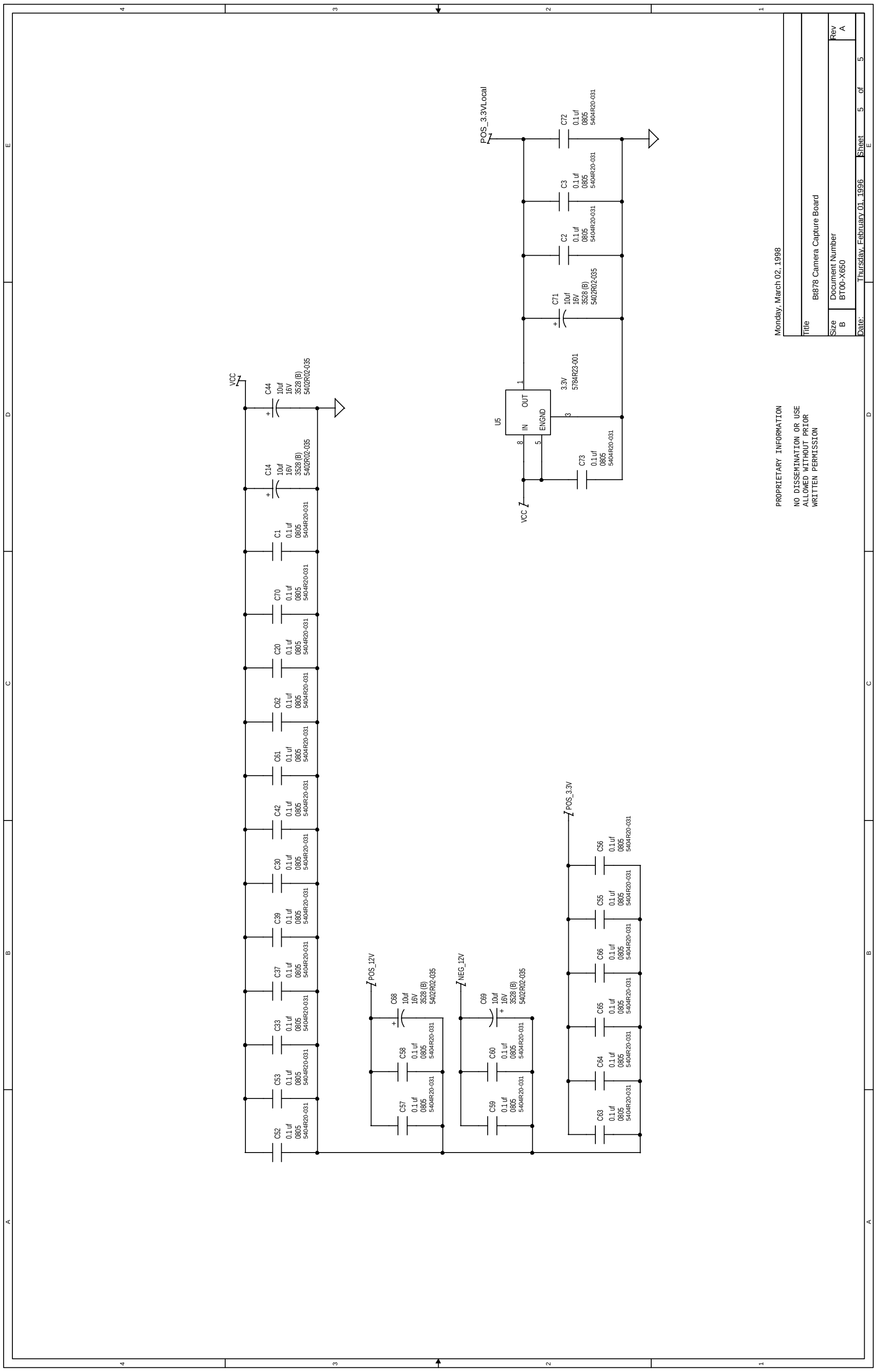


Figure 3-3d. Sample Schematic (Power)



4.0 Parametric Information

Table 4-1. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply, 5 V—Output, pin 25	VDD5	4.75	5.0	5.25	V
Power Supply—3.3 V CMOS	VDD	3.0	3.3	3.6	V
Ambient Operating Temperature	T_A	0	+25	+70	˚C

Table 4-2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
VDD5	VDD5		5.25	V
V_{DD}	VDD		3.6	V
Voltage on any signal pin(1)		GND –0.5	VDD5 +0.5	V
Ambient Operating Temperature	T_A	0	+70	˚C
Storage Temperature	T_S	0	+60	˚C
Junction Temperature	T_J		+150	˚C
Vapor Phase Soldering (15 Seconds)	T_{VSOL}		+210	˚C

Notes: (1). This device employs high-impedance CMOS devices on all signal pins. It must be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V or drops below ground by more than 0.5 V can induce destructive latchup.

2. Stresses above those listed may cause permanent damage to the device. This is a stress rating only, and functional operation at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4.1 DC Characteristics

Table 4-3. DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
5 V-tolerant TTL Inputs, all except SDATA[3:0]					
Input Leakage Low	IIL			–10	µA
Input Leakage High	IIH			10	µA
Input High Voltage	VIH	2.0		VDD5 + 0.5	V
Input Low Voltage	VIL	–0.5		0.8	V
5 V-tolerant Inputs with Hysteresis, SDATA[3:0]					
Input Leakage Low	IIL			-10	µA
Input Leakage High	IIH			10	µA
Input High Voltage	VIH	0.7 * VDD		VDD5 + 0.5	V
Input Low Voltage	VIL	–0.5		0.3 * VDD	V
Input Capacitance (V = 1 MHz, Vin = 2.4 V)			10		pF
3.3 V outputs, all but SCLK, XTO, FSTRT					
Output High Voltage (IOH = 4 mA)	VOH	2.4 V			V
Output Low Voltage (IOL = -4 mA)	VOL			0.4	V
3.3 V outputs, XTO and FSTRT					
Output High Voltage (IOH = 1.5 mA)	VOH	2.4 V			V
Output Low Voltage (IOL = 1.5 mA)	VOL			0.4	V
5 V output, SCLK					
Output High Voltage (IOH = 1.5 ma)	VOH	VDD5 –0.4			V
Output Low Voltage (IOL = -1.5 ma)	VOL			0.4	V

4.2 AC Characteristics

Table 4-4. AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
XTAL Frequency (± 50 ppm)	f_{xtal}		14.31818		MHz
VCLK Cycle time	t_{vcyc}		139.68		ns
VCLK Duty cycle	t_{vduty}	45	50	55	%
VCLK (edge programmable) to VDATA, FSTRT, LSTRT, INTR (CL = 50 pf)	td			30	ns
I^2C Timing	Consult I^2C Bus Reference Guide				

Table 4-5. Power Supply Current Parameters

Parameter	Symbol	Min	Typ	Max	Units
Supply Current	I				
VDD			TBD	TBD	mA
VDD5			TBD	TBD	mA

4.2.1 Processor Latency

The sensor and processor, while working synchronously at clock level, do not start and stop output image generation simultaneously. This is due to processor latency: the time difference between the appearance of the first input pixel of a frame and the appearance of the first output pixel.

Processor latency has several components:

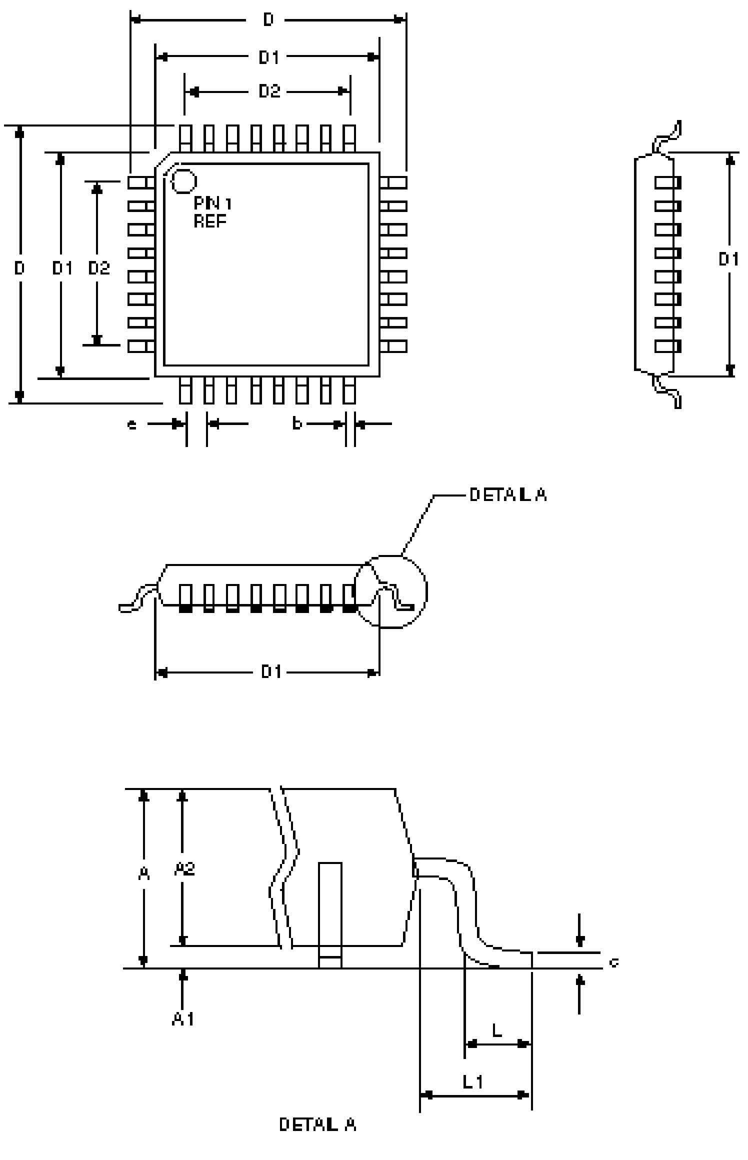
- Four lines of image data to provide line history for vertical filtering.
- One half-line of image data for the unshuffling operation.
- Several clock cycles to account for pipeline latency of the processor itself.

Before the processor commences output, a time duration no less than the processor latency must have elapsed since the sensor consumes any parameter updates.

4.3 Package Information

Figure 4-6 illustrates the 32-pin TQFP mechanical specifications of the Bt832.

Table 4-6. 32-Pin TQFP Mechanical Specifications



Dim.	Millimeters Min.	Millimeters Max.	Inches* Min.	Inches* Max.
A	1.6 MAX		0.0630 MAX	
A1	0.05	0.15	0.0020	0.0059
A2	1.4 REF		0.0551 REF	
D	8.75	9.25	0.3445	0.3642
D1	7.0 REF		0.2756 REF	
D2	5.6 REF		0.2205 REF	
L	0.5	0.75	0.0197	0.0295
L1	1.0 REF		0.0394 REF	
e	0.80 BSC		0.0315 BSC	
b	0.30	0.40	0.0118	0.0157
c	0.13	0.19	0.0051	0.0075
Coplanarity	0.10 MAX		0.004 MAX	

Ref: 32-PIN TQFP (GP00-D262)

* Metric values (millimeters) should be used for PCB layout. English values (inches) are converted from metric values and may include round-off errors.

FD-TQFP-32 (04/03/95)

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