



# Intel<sup>®</sup> 845GE/845PE Chipset

## Specification Update

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*Intel<sup>®</sup> 82845GE Graphics and Memory Controller Hub (GMCH) /  
Intel<sup>®</sup> 82845PE Memory Controller Hub (MCH)*

*June 2003*

**Notice:** The Intel<sup>®</sup> 82845GE GMCH/82845PE MCH may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

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The Intel® 82845GE GMCH / 82845PE MCH may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

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## Revision History

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Rev.	Draft/Changes	Date
-001	Initial Release.	October 2002
-002	(1) Added a new Q-Spec number to the Component Marking Information Table (2) Modified the Summary Table of Changes to allow differentiation of Specification Update Items to the specific 82845GE or 82845PE chipset (3) Added Specification Clarification #A1,B1, The Use of 400 MHz PSB and DDR333 Is Not Supported (4) Added Erratum #A1, GMBUS Protocol	December 2002
-003	(1) Added Documentation Change #A1, Remove Note in Graphics Control Register (Device 0), Bit [3] (2) Added Erratum #A2, VGA Panning (3) Added Erratum #A3, VGA Timing	June 2003

## Preface

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This public document is an update to the specifications contained in the documents listed in the following Affected Documents/Related Documents table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this update document and are no longer published in other documents.

### Affected Documents/Related Documents

Document Title	Document Number
<i>Intel® 845GE/845PE Chipset Datasheet: Intel® 82845GE Graphics and Memory Controller Hub (GMCH) / Intel® 82845PE Memory Controller Hub (GMCH)</i>	251924-001

## Nomenclature

**Specification Changes** are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

**Errata** are design defects or errors. Errata may cause the behavior of the Intel 82845GE GMCH / 82845PE MCH to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

**Specification Clarifications** describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

**Documentation Changes** include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

## Component Identification via Programming Interface

The Intel 82845GE GMCH / 82845PE MCH may be identified by the following register contents:

Stepping	Vendor ID <sup>1</sup>	Device ID <sup>2</sup>	Revision Number <sup>3</sup>
B0	8086h	2560h	02h
B1	8086h	2560h	03h

**NOTES:**

1. The Vendor ID corresponds to bits 15:0 of the Vendor ID Register located at offset 00–01h in the PCI function 0 configuration space.
2. The Device ID corresponds to bits 15:0 of the Device ID Register located at offset 02–03h in the PCI function 0 configuration space.
3. The Revision Number corresponds to bits 7:0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space.

## Component Marking Information

The 82845GE GMCH / 82845PE MCH may be identified by the following component markings:

Stepping	Q-Spec	S-Spec	Top Marking	Notes
B0	QD53	SL6H5	RG82845PE	82845PE Desktop
B1	QD74	SL6PS	RG82845GE	82845GE Desktop
B1	QD75	SL6Q3	RG82845PE	82845PE Desktop



## Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes that apply to the listed Intel 82845GE GMCH / 82845PE MCH steppings. Intel may intend to fix some of the errata in a future stepping of the component and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

### Codes Used in Summary Table

- X: Errata that applies to this stepping.
- Doc: Document change or update that will be implemented.
- PlanFix: This erratum may be fixed in a future stepping of the product.
- Fixed: This erratum has been previously fixed.
- NoFix: There are no plans to fix this erratum.
- (No mark) or (Blank Box): This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Shaded: This item is either new or modified from the previous version of the document

**Note:** Each Specification Update item is prefaced with a capital letter to distinguish the product. The key below details the letters that are used in this Intel® 845GE/845PE Chipset Specification Update.

A = Intel® 82845GE Graphics and Memory Controller Hub (GMCH)

B = Intel® 82845PE Memory Controller Hub (MCH)

NO.	SPECIFICATION CHANGES
	There are no specification changes in this Specification Update revision.

NO.	A1	B1	PLANS	ERRATA
A1	X	X	NoFix	GMBUS Protocol
A2	X	X	NoFix	VGA Panning
A3	X	X	NoFix	VGA Timing

NO.	SPECIFICATION CLARIFICATIONS
A1,B1	The Use of 400 MHz PSB and DDR333 Is Not Supported.

NO.	DOCUMENTATION CHANGES
A1	Remove Note in Graphics Control Register (Device 0) (Intel® 82845GE only), Bit [3]

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## ***Specification Changes***

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There are no specification changes in this Specification Update revision.

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## Errata

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### A1. GMBUS Protocol

**Problem:** Under certain environmental conditions, there are design sensitivities in asynchronous clock crossing logic in the 82845GE GMBUS implementation. As a result, the 82845GE may not correctly complete the protocol transactions to the DVI device.

**Implication:** A platform will boot normally but there is no display when using non-VGA display devices such as televisions, local non-removable digital flat panels and external user-removable DVI displays.

**Workaround:** A Video BIOS workaround is available in 82845GE VBIOS version 11.4.1 (build #2759).

**Status:** There are no plans to fix this erratum in silicon.

### A2 VGA Panning

**Problem:** VGA text mode diagnostic and stress test applications that use pixel panning can experience temporary visual anomalies under certain memory configurations. The memory configurations affected are 64-MB technology products that use 2-KB and 4-KB page sizes.

1. Test applications using a single VGA font table with a 32-KB font buffer range could fail. This failure was seen in a diagnostic utility.
2. Test applications using multiple VGA font tables could fail if the first two fonts are from different tables. This failing condition can occur in any memory configuration. This failure was seen in a stress test utility.

**Implication:** Entire scanlines will appear to flicker in some VGA diagnostic and stress test applications. However, there are no known customer sightings of this erratum. No known end user applications fail for this erratum.

**Workaround:** No workaround exists.

**Status:** This will not be fixed in future steppings

### **A3**      **VGA Timing**

**Problem:** Some VGA applications, running in 40-column modes, that use a non-black border color, may experience color/visual issues on systems configured with certain monitors.

**Implication:** 40-column VGA modes may experience visual color anomalies on some CRT monitors. This was observed using VGA focused Intel test software. With certain monitors, colors in active areas may change as the border color changes. As observed while using the test software, visual color anomalies can range from a slight color change difference to a completely blank screen. Based on the lack of customer or end user reported issues related to this erratum, the number of VGA applications that run in 40-column modes and also use non-black border colors is unknown, but is low. Based on Intel's validation and compatibility testing, the number of CRT monitors that exhibit the this color corruption anomaly is also low.

**Workaround:** No workaround exists.

**Status:** This will not be fixed in future steppings

## Specification Clarifications

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### A1,B1. The Combination of 400 MHz PSB and DDR333 Is Not Supported

Reference the *Intel® 845GE/845PE Chipset Datasheet*, Document Number 251924-001, dated October 2002, Section 1.4.1, *Host Interface*. Inset the following sentence between the first and second paragraphs:

“The use of a 400 MHz Processor System Bus together with DDR333 memory modules is a non-supported platform configuration.”

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## Documentation Changes

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**A1      Remove Note in Graphics Control Register (Device 0), (Intel® 82845GE only)  
Bit [3]**

Reference the *Intel® 845GE/845PE Chipset Datasheet*, document number 251924-001, paragraph 3.5.1.15, “GC – Graphics Control Register (Device 0)” (Intel® 82845GE only), at address offset 52h.

The Note in the description of bit [3] in this register is not correct. Remove the Note.